A Novel Asymmetric Half-Bridge Inverter for Capacitive Wireless Power Transfer

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***Abstract*—Capacitive wireless power transfer (CPT) is becoming a promising alternative to the inductive power transfer (IPT) due to the low cost and simplicity of the coupler link. However, if the configuration of the conventional IPT system is directly applied to the CPT, it increases the cost of the system. The paper proposes a topology to make CPT system more simple with the high voltage gain and the wide zero voltage switching (ZVS) feature. The target system is a low power system with the universal input voltage and wide load range applications (110V-340V, 6W-60W). The design and analysis procedures are presented, and the circuit is simulated in PSIM to verify the performance of the proposed topology.**

***Keywords*—Zero voltage switching, capacitive wireless power transfer, asymmetric half-bridge.**

I. Introduction

Nowadays, wireless power transfer is widely applied in electric vehicles, internet of thing devices, light-emitting diode, and biomedical application [1]. The inductive wireless power transfer (IPT) has been accepted with successful implementations. Recently, the capacitive wireless power transfer (CPT) has been proposed as the solution to replace the IPT systems as shown in Fig. 1(a). It uses electric fields instead of magnetic fields, to transfer energy through metal barriers without significant power losses. The advantage of CPT is the reduction of the cost and weight of energy coupler structure. Among various topology available in CPT systems [2], [3], [4], phase-shift full-bridge is usually regarded as the most suitable topology, because it can control the magnitude and frequency of the primary voltage. However, it requires four power switches and gate drivers, which makes the system complex and expensive. On the other hand, to achieve ZVS, the operating frequency should be tied to the inductive region which is placed above the resonant frequency. So, the gain curve is heavily dependent on the load, which makes the control difficult. Furthermore, it only steps down the voltage gain and thus cannot cover the wide input voltage variations.

To overcome these problems, a new half-bridge structure incorporating a buck-boost is proposed as shown in Fig. 2. The output voltage can be regulated by the duty ratio control that can achieve a wide input range. The proposed structure provides wide zero-voltage-switching (ZVS) by adding the parallel inductance, Lp, and operates in a resonant mode where the control becomes easy. Furthermore, the boost operation is possible. Thus, the dc-dc converter and high frequency inverter can be merged in the proposed topology as shown in Fig 1(b). In this paper, the operating principle is presented with operation mode and zero voltage switching analysis.

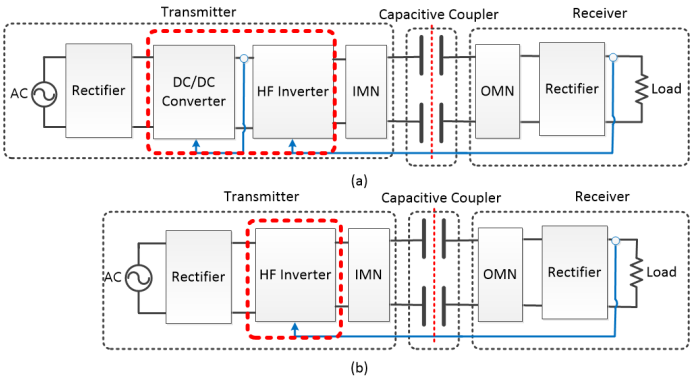

Fig. 1. (a) Conventional systems (b) Proposed systems.

II. Proposed Topology

Figure 2 shows the proposed topology, where two active switches, S_1 and S_2, are driven by asymmetrical pulse-width-modulated (APWM) gating pulses, and the floating capacitor, C_c, together with the parallel inductor, L_p, forms a buck-boost configuration [5]. Therefore, the average voltage of the capacitor and the peak-to-peak current in the parallel inductor can be derived as

$$V_{c_c} = \frac{D}{1-D} V_s \tag{1}$$

and

$$\Delta L_p = \frac{T_o D}{L_p} V_s \tag{2}$$

Because the proposed topology is controlled by a PWM gating signal at the resonant frequency, f_o, and mostly operated in the high quality factor of the resonance, the primary voltage waveform, v_{pri}(t), is expressed by the Fourier series, and only the fundamental component can be considered for simplicity. Thus, the magnitude of the fundamental voltage is well approximated by

$$v_{pri,f}\,(t) = \frac{2V_s}{\pi(1-D)} \sin(\pi D), \tag{3}$$

where

$$f_o = \frac{1}{2\pi\sqrt{L_r(C_{link1}||C_{link2})}} \tag{4}$$

and

$$C_{link} = C_{link1}||C_{link2}. \tag{5}$$

Since the buck-boost converter and the half-bridge [5] are merged, it is clear that the output voltage can be regulated directly by changing the duty ratio of S_1 and the dc voltage gain is given by

$$\frac{V_o}{V_s} = \frac{\sin(\pi D)}{2(1-D)} \leq \frac{\pi}{2}. \tag{6}$$

Figure 3 shows that the voltage gain of the proposed topology is wide in comparison with the conventional half-bridge and full bridge. However, since the switching voltage stress increases as the voltage gain increases, the maximum allowable duty should be limited.

III. Operation Analysis

The operation analysis for each time interval in Fig. 4 is shown as follows.

Stage 1 [$t_0 < t < t_1$]: The switch S_1 is turned ON while the switch S_2 is OFF. The current in L_p is charged as (7), the drain-to-source voltage of switch S_2 reaches its maximum value as (8), and the primary voltage, v_{pri}, becomes the same as the input voltage, V_s.

$$i_{L_p}(t) = \frac{V_s}{L_p}(t - t_0) + i_{L_p}(t_0) \tag{7}$$

$$V_{cds2}(t_0) = \frac{V_s}{1-D} \tag{8}$$

Stage 2 [$t_1 < t < t_2$]: It starts when the switch S_1 is turned OFF while the switch S_2 is still OFF. The energy stored in the inductors, L_p, and L_r, charge the parasitic output capacitor of S_2 while the output capacitor of S_1 is discharged, which makes the ZVS possible.

Stage 3 [$t_2 < t < t_3$]: It starts when the switch S_2 is turned ON while the switch S_1 is OFF. At $t = t_2$ the parasitic output capacitor of S_2 is fully discharged. Thus, S_2 turns ON in ZVS condition, the drain-to-source voltage of switch S_1 reaches its maximum value as in (9) and the current flowing in L_p, C_c, and L_r are summed to be zero as in (10).

$$v_{cds1}(t_3) = \frac{V_s}{1-D} \tag{9}$$

$$i_{L_p}(t) + i_{L_r}(t) + i_{cr}(t) = 0 \tag{10}$$

Stage 4 [$t_3 < t < t_4$]: It starts when the switch S_2 is turned OFF while S_1 is OFF. In this stage, the energy stored in the inductors L_p and L_r is used to charge the parasitic output capacitor of S_2 and discharge the output capacitor of S_1. Thus, the ZVS can be achieved.

IV. Zero Voltage Switching Condition

This section discusses the ZVS condition in the proposed method.

Figure 6 shows the switch voltage and current waveforms. Since the switch S_1 is turned on, the capacitor current C_c is equal to zero. Thus, the charge balance of capacitor C_c can be expressed in (11)

$$\int_{\pi D}^{2\pi - \pi D + \theta_d} i_{L_p}(\omega t) + i_{Lr}(\omega t) = 0 \tag{11}$$

where

$$\theta_d = \frac{2\pi}{T} t_d \tag{13}$$

and the minimum curent of the inductor, L_p, can be obtained by (11), which is given by (12).

This amount of charge needs to be displaced during the dead-time, t_d, to satisfy the ZVS. The maximum amount of charge is the total charge in L_p and L_r that can be expressed as follows

$$q_{L_r} = \frac{1}{\omega_0}\left(\frac{2\theta_d V_s}{R_e \pi (1-D)} \sin(\pi D) cos\left(-\pi D + \frac{\theta_d}{2}\right)\right). \tag{14}$$

Considering the total charge in C_{ds1} and C_{ds2}, which is given by the ZVS occurs while the parasitic output capacitor of the switch is initially at zero before the switch turns on [6]. In the analysis, the parasitic capacitor is assumed to be a linear capacitance [7], it can be calculated as

$$C_{eq} = \frac{Q}{V_s} = \frac{1}{V_s}\int_0^{V_s} C_{ds}\left(\frac{V_s}{1-D}\right) d\left(\frac{V_s}{1-D}\right) = 2C_{ds}, \tag{16}$$

$$q_{sw} = (C_{eq1} + C_{eq2})\frac{V_s}{1-D}, \tag{17}$$

where $C_{ds} = C_{ds1} = C_{ds2}$ is assumed. To satisfy ZVS, the condition should be met, and is given by

$$q_{L_p} + q_{L_r} \geq q_{sw}. \tag{18}$$

The value of the inductor, L_p,is expressed from (18) as shown in (19). Thus, ZVS range can be achieved by using the design 3D curve as shown in Fig. 7, the data is used to draw this curve as shown in Table I.

$$i_{L_p,n}(-\pi D) = V_s\left(\frac{2}{\pi^2 R_e (1-D)^2}\sin(\pi D)\sin(\pi(1-D)) - \frac{\pi D}{\omega L_p}\right). \tag{12}$$

$$q_{L_p} = \frac{\theta_d V_s}{2\omega_0(1-D)}\left(\frac{D}{\omega_0 L_p}(2\pi(1+D) - \theta_d) + \frac{4}{\pi^2 R_e(1-D)}\sin(\pi D)\sin(\pi(1-D))\right). \tag{15}$$

$$L_p \leq \frac{\theta_d D(2\pi(1+D) - \theta_d)}{4\omega_0\left(C_{eq}\omega_0 - \frac{\theta_d}{\pi R_e}\sin(\pi D)\left(\frac{1}{\pi(1-D)}\sin(\pi(1-D)) + cos\left(-\pi D + \frac{\theta_d}{2}\right)\right)\right)}. \tag{19}$$

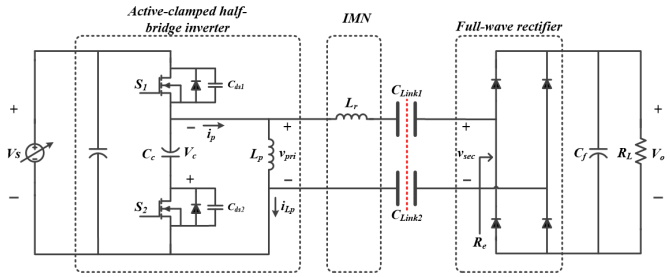

Fig. 2. The proposed topology.

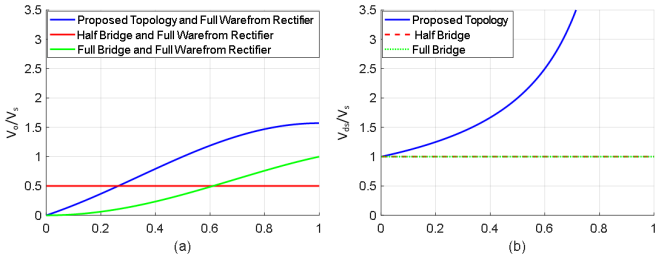

Fig. 3. (a) The voltage normalized gain (b) The switching voltage stress normalized by input voltage.

V. Design Procedure

This section describes the components design procedure and the simulation results to verify the performance of the proposed topology.

A. Target System Specification

To make universal input voltage and output power range, the specification of the system can be written as

$$V_{s,\min} \le V_s \le V_{s,\max}, \tag{20}$$

and

$$P_{o,\min} \le P_o \le P_{o,\max}. \tag{21}$$

The target voltage is fixed to V_o, so the value of the duty can be obtained switching duty-cycle by using (6) and the value of load resistor is expressed as follow

$$\frac{{V_o}^2}{P_{o\max}} \le R_L \le \frac{{V_o}^2}{P_{o\min}}. \tag{22}$$

B. Component Design Guideline

In this section, C_{link} is given by the energy link, the ω and t_d is assumed, and C_{eq} is given by datasheet of MOSFET to be used.

1) The Resonant Components, L_p and C_{link} : The peak tank inductor current and coupler link capacitor voltage peak magnitudes are both approximately proportional to the maximum load current, I_{omax}. Thus, the peak inductor current is written as

$$I_{Lr,p} = \frac{\pi}{2} I_{o,\max} = \frac{\pi}{2} \frac{P_{o\max}}{V_o}. \tag{23}$$

and the inductor value should be chosen by

$$L_r = \frac{1}{{\omega_0}^2 C_{link}}. \tag{24}$$

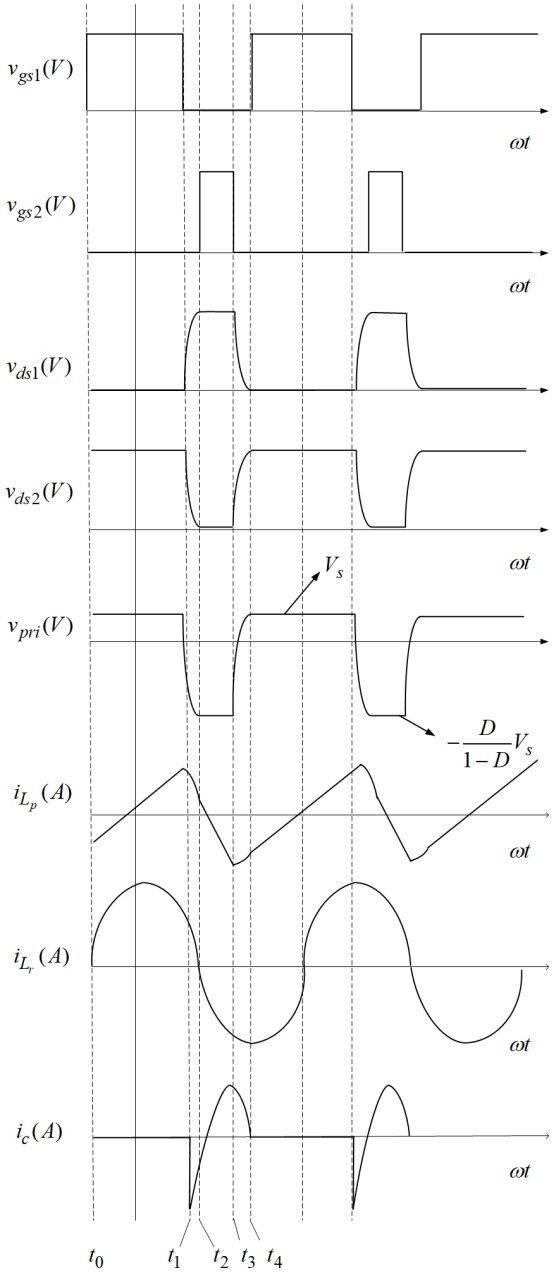

Fig. 4. Steady-state waveform ($D < 0.5$).

The peak link capacitor voltage is related to the tank inductor current due to the series connection , the value is shown as in the following

$$V_{Clink,p} = I_{L_r,p}\sqrt{\frac{L_r}{C_{link}}} = \frac{\pi}{2}\frac{P_{o\max}}{V_o}\sqrt{\frac{L_r}{C_{link}}}, \tag{25}$$

and in this paper, a parallel capacitor is used with copper material and 500 mm by 500 mm lateral dimension. The space between the two palates is 3 mm and the glass is used as the spacing material.

2) The Shunt Inductor, L_p: According to Fig.7 and the condition as shown in below, the value of inductor can be chosen as the minimum value among them to satisfy ZVS

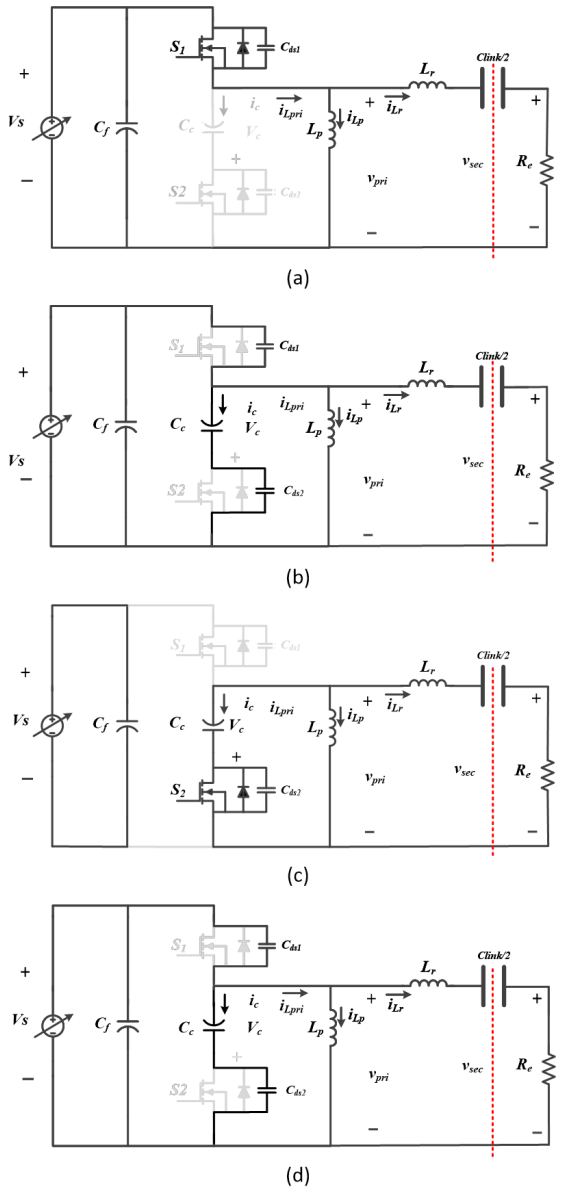

Fig. 5. Equivalent of the proposed topology (a) Stage 1. (b) Stage 2. (c) Stage 3. (d) Stage 4.

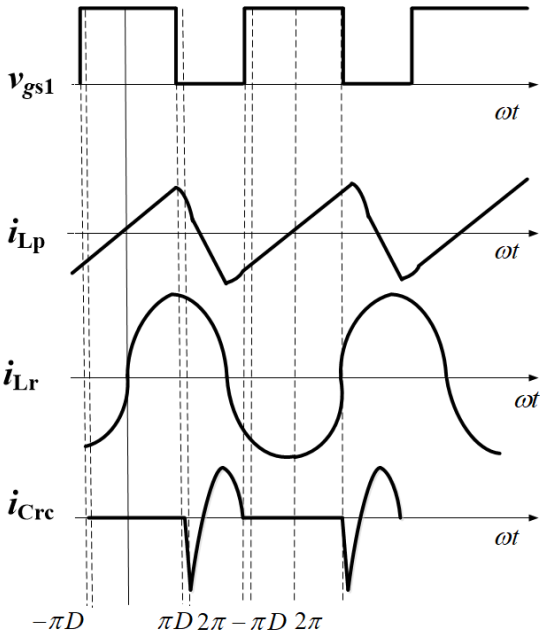

Fig. 6. Switch voltage and current waveforms.

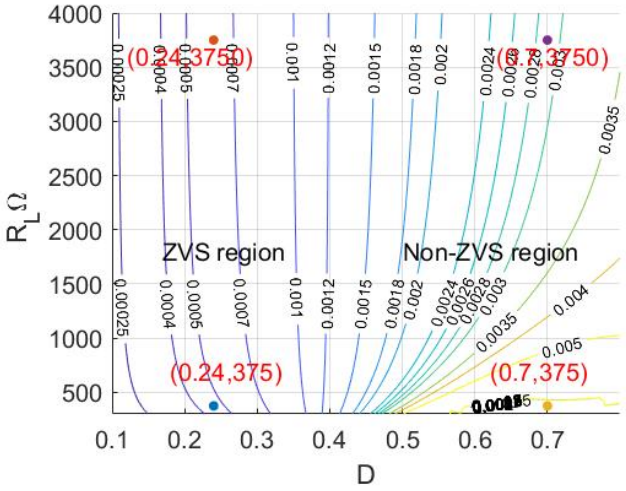

Fig. 7. ZVS boundaries. θ_d = 0.2666 rad, ω = 2π.147000 rad/s, C_{eq1} = C_{eq1} = 240 pF.

of all conditions, and then the value of the inductor can be designed base on the target system specification as shown in Section V.A. The maximum stress current of the inductor can be calculated as

$$i_{Lp,p} = i_{Lp,n}(-\pi D) + \frac{DTV_s}{L_p}. \tag{26}$$

3) The Clamp Capacitor, C_c: The minimum value of the clamp capacitor can be approximately calculated as shown in the following

$$C_{c,\min} = \frac{(1-D)(q_{L_p} + q_{L_r})}{DV_s}, \tag{27}$$

where q_{Lp} and q_{Lr} are calculated in (14) and (15), and the voltage stress is already calculated in (1).

4) The Switches, S_1 and S_2: The voltage stress in the switches S_1 and S_2, can be calculated as

$$V_{S,p} = \frac{V_s}{1-D}. \tag{28}$$

5) The Rectifier Diode: The voltage stress of the diode in the rectifier can is approximately given as

$$V_{D,p} = V_o. \tag{29}$$

The average current stress of the diode can be expressed as

$$I_{D,avg} = \frac{1}{2} I_{o,avg}. \tag{30}$$

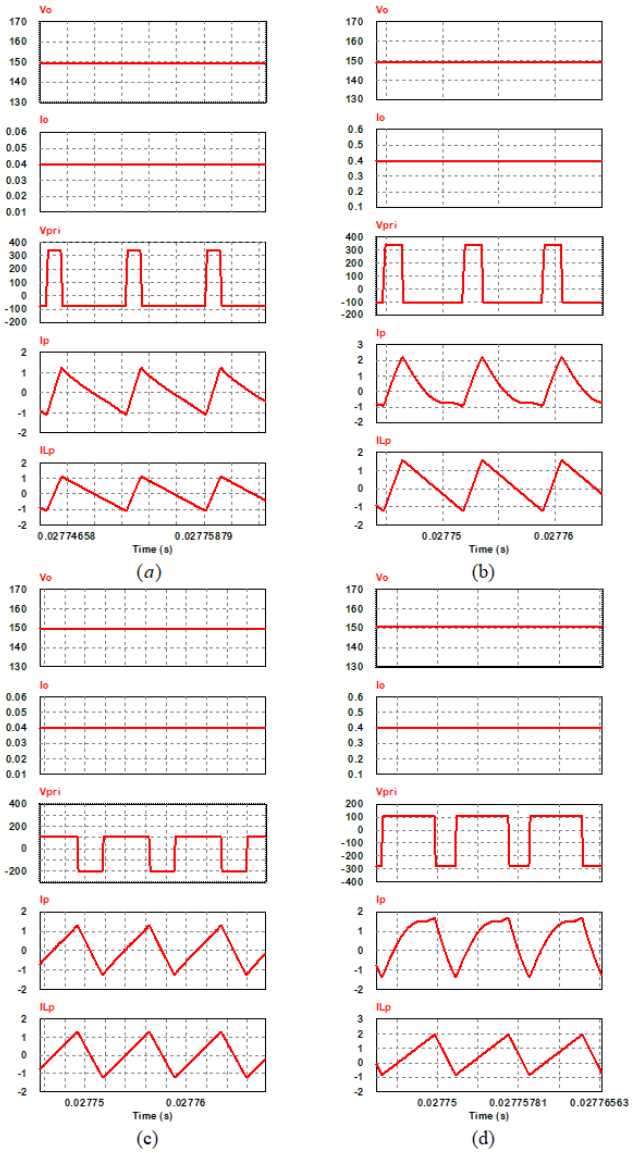

Fig. 8. Simulation results (a) Scenario 1 (b) Scenario 2 (c) Scenario 3 (d) Scenario 4.

VI. Verification

Following the design procedure in section V, we can obtain the simulation parameters as shown in the Table I. The proposed topology is verified by the simulation in PSIM. Table I shows the parameters of the simulation. As shown in the Table II, the proposed system is tested with a universal input voltage and the output power is changed from 6W to 60W. The simulation results are shown in Fig. 8, the ZVS condition is achieved for all scenarios. It should be noted that the dependency of the ZVS boundary on the output power increases as the duty ratio increases. The waveforms of the current in the parallel inductor and the current in the clamp capacitor match well with operation analysis in section III.

TABLE I
Simulation Parameters

Parameter	Value
f_o	$141kHz$
L_p	$200uH$
$C_{ds1} = C_{ds2}$	$240pF$
C_c	$10uF$
L_r	$1407uH$
C_{link}	$0.9nF$
C_f	$10uF$
t_d	$300ns$

TABLE II
Simulation Scenarios

Scenario	Input Voltage	Output Power
High voltage and light load (1)	$340V$	$6W$
High voltage and heavy load (2)	$340V$	$60W$
Low voltage and light load (3)	$110V$	$6W$
Low voltage and heavy load (4)	$110V$	$60W$

VII. Conclusion

This paper proposes an asymmetry half-bridge topology for capacitive wireless power transmission. Since it has the features of the wide voltage gain, less active component, simple gate driving, and wide ZVS range, it is expected to further strengthen the merits of CPT over IPT system. The performance of the proposed topology is verified by using simulation with universal input voltage and wide load range.

References

[1] P. Si, A. P. Hu, S. Malpas, and D. Budgett, "A Frequency Control Method for Regulating Wireless Power to Implantable Devices," in IEEE Transactions on Biomedical Circuits and Systems, vol. 2, no. 1, pp. 22-29, March 2008.

[2] F. Lu, H. Zhang, and C. Mi, "A Review on the Recent Development of Capacitive Wireless Power Transfer Technology," Energies, vol. 10, no. 11, p. 1752, Nov. 2017.

[3] J. Dai, S. Hagen, D. C. Ludois, and I. P. Brown, "Synchronous Generator Brushless Field Excitation and Voltage Regulation via Capacitive Coupling Through Journal Bearings," in IEEE Transactions on Industry Applications, vol. 53, no. 4, pp. 3317-3326, July-Aug. 2017.

[4] H. S. Choi, J. Y. Park, and S. J. Choi, "Analysis and control of capacitive-coupled wireless power transmission system," 2015 15th International Conference on Control, Automation and Systems (ICCAS), Busan, 2015, pp. 1005-1009.

[5] I. H. Cho, Y. D. Kim, and G. W. Moon, "A Half-Bridge LLC Resonant Converter Adopting Boost PWM Control Scheme for Hold-Up State Operation," in IEEE Transactions on Power Electronics, vol. 29, no. 2, pp. 841-850, Feb. 2014.

[6] M. Kline, I. Izyumin, B. Boser, and S. Sanders, "Capacitive power transfer for contactless charging," 2011 Twenty-Sixth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), Fort Worth, TX, 2011, pp. 1398-1404.

[7] J. A. Sabate, R. W. Farrington, M. M. Jovanovic and E. C. Lee, "Effect of FET output capacitance on ZVS of resonant converters," in IEEE Transactions on Aerospace and Electronic Systems, vol. 32, no. 1, pp. 255-266, Jan. 1996.

[8] A. F. Witulski and R. W. Erickson, "Design of the Series Resonant Converter for Minimum Component Stress," in IEEE Transactions on Aerospace and Electronic Systems, vol. AES-22, no. 4, pp. 356-363, July 1986.