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Novel Burst-Mode Control for Medium-to-Light Load Operation of Dual-Active-Bridge Converters, Achieving Minimum Backflow Power, Zero-Voltage-Switching, and DC Bias Suppression

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Abstract: The dual-active-bridge (DAB) converter is widely used in many applications such as solid-state transformers, multi-port converters, and on-board chargers. Nevertheless, its efficiency degrades significantly under light-load conditions due to high switching and conduction losses. Since a detailed analysis for burst-mode design has not been presented in the literature, effective burst-mode control for the light-load condition is proposed in this paper. In the proposed burst-mode, the regular duty cycle and the burst duty cycle are optimally coordinated to achieve the zero-voltage-switching (ZVS) condition and the minimum backflow power at the same time. Moreover, DC bias current is effectively eliminated in the proposed burst-mode. The switching loss and conduction loss are simultaneously minimized in the proposed burst-mode control. Therefore, the light-load efficiency is significantly improved. The detailed analysis and design procedure are also presented for both buck- and boost-mode operations to deal with widely varying output voltage ranges. The control mode switching condition is determined for achieving the ZVS condition for the whole load condition; thus, the proposed burst-mode control flowchart is presented. A 4 kW DAB converter prototype is built to verify the proposed method and the experiment results show about a 2% increment in efficiency of the proposed method compared to the conventional burst-mode method.

Keywords: dual-active-bridge converter; burst-mode; optimal backflow power; efficiency; light-load condition; ZVS condition

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1. Introduction

The isolated dual-active-bridge (DAB) converter is one of the most popular converters in applications such as solid-state transformers, multi-port converters, and other applications due to its bidirectional and symmetrical structure, zero-voltage-switching (ZVS), and wide voltage gain regulation capabilities [1–3]. These features allow it to be used in systems such as energy storage systems and uninterruptible power supplies, which are characterized by widely varying output voltage conditions from renewable energy sources or loads such as energy storages that include batteries and variable loads. These characteristics of the DAB converter necessitate high efficiency over a wide range of effective input/output voltage ratios, particularly under light-load conditions.

The single-phase-shift (SPS) control for DAB converters is the most popular modulation method for DAB control strategies used by industrial practitioners due to its low cost, simple implementation, and easy design [4]. However, SPS control of DAB increases backflow power under light-loads, generating circulating currents [5–8]. To overcome this limitation, many modulation controls such as extended-phase-shift (EPS), dual-phase-shift (DPS), and triple-phase-shift (TPS) have been proposed [9–13]. However, the complexity

of control strategies with many control variables make optimal control difficult [14]. Furthermore, if the voltage gain is not unity in light-load conditions, hard switching occurs, resulting in reduced efficiency [15,16]. Although the magnetizing inductance of a transformer is utilized by introducing an air gap to achieve a full-range ZVS and improve the light-load efficiency of the DAB converter [4], this is not recommended due to the increased size, cost, and losses [17–19].

To address the two main issues of SPS control under a light-load operation of the DAB, burst-mode is widely used. Burst-mode significantly reduces conduction loss, switching loss, and core loss [20], and has been widely used in power converters [21–23]. In burst-mode control, the switching cycles are minimized during light-load conditions, which significantly improves efficiency. This is in contrast to EPS, DPS, and TPS, which continuously adjust phase shifts and maintain high switching losses, leading to a significant improvement in the light-load efficiency of the burst-mode control, particularly in applications with highly variable load conditions. Recently, burst-mode has been applied to DAB converters to improve light-load efficiency [24]. The design of burst-mode parameters, such as the burst-mode frequency and burst-mode duty cycle, are presented in [25]. Small-signal modeling for burst-mode control is presented in [26]. However, DC bias occurs in a conventional burst-mode at every first cycle of a burst-mode operation, which can cause current spikes in the inductor and an oversaturation of the transformer [27–29]. In conventional method, the current direction is considered for deriving the ZVS condition. However, the positive or negative direction of the current does not always guarantee soft switching in MOSFETs [30,31]. To further elaborate the ZVS condition, the energy in the output capacitors of the MOSFETs in the full-bridge should be considered as well [30,31]. Moreover, the regular duty cycle and the burst duty cycle are not optimally coordinated to achieve the zero-voltage-switching (ZVS) condition and the minimum backflow power at the same time. Therefore, the switching loss and conduction loss are not simultaneously minimized; thus, the light-load efficiency is not much improved.

To improve the performance of the burst-mode, the optimal burst-mode control for the light-load condition is proposed in this paper. In the proposed method, the optimal duty cycle is adaptively calculated in the burst-mode control to minimize the backflow power, while the burst duty cycle is used for regulating the output voltage. Moreover, the DC bias current is effectively eliminated in the proposed burst-mode. This paper is an expanded version of our conference paper, which was presented only for buck-mode operations [32]. In this paper, a detailed analysis and design procedure are presented for both buck- and boost-mode operations to deal with widely varying output voltage range. The control mode switching condition is determined for achieving the ZVS condition for whole-load conditions, and thus, the proposed burst-mode control flowchart is presented, which is newly appended. Moreover, the MOSFETs' nonlinear output capacitance characteristics are taken into account for the complete ZVS condition. The advantages of the proposed burst-mode can be listed as follows:

1. No additional components are needed for efficiency improvement under light-load conditions.
2. Complete ZVS condition is considered for optimal operation of burst-mode and ZVS is achieved for entire load range.
3. Backflow power is minimized at the light-load condition.
4. DC bias current elimination is applied for the burst-mode.
5. A mode switching algorithm between the burst-mode and normal-mode is proposed.

A comparative table of advantages and disadvantages of the proposed method compared with other investigations is shown in Table 1.

The rest of this paper is structured as follows: Section 2 discusses the operation of the DAB converter, then Section 3 presents the proposed burst-mode for the DAB converter. The design procedure and control mode sequence are presented in Sections 4 and 5, respectively. The analysis is verified via experimentation in Section 6. Finally, the results of the study are summarized in Section 7.

Table 1. Comparisons with previous control methods.

Ref.	Type of Control	Soft-Switching Range	Minimum Backflow Power	Implementation Complexity	DC Bias Elimination
[4]	SPS	Partial	No	Low	No
[9]	EPS	Partial	Yes	Medium	No
[10]	DPS	Partial	Yes	Medium	No
[11]	TPS	Full	Yes	High	No
[33]	SPS + burst-mode	Partial	No	Low	No
This paper	SPS + burst-mode	Full	Yes	Low	Yes

2. Operation of the Isolated DAB Converter

Figure 1 shows a DAB converter circuit that has two active full bridges to generate a square wave voltage; a series inductor L to store energy for power transfer; and a transformer with a turn ratio of 1:n to meet the high-voltage ratio and provide galvanic isolation. The key waveforms under the SPS modulation of the DAB converter in either buck or boost operation modes are shown in Figure 2, where the currents at the vertices are given by

$$I_0 = \left[V_s(2D-1) + \frac{V_o}{n}\right]\frac{T_s}{4L} \tag{1}$$
$$I_1 = \left[V_s + \frac{V_o}{n}(2D-1)\right]\frac{T_s}{4L}.$$

According to the analysis in [6,15], the voltage gain M and the output power P_o of the DAB converter are given by

$$M = \frac{V_o}{nV_s} = \frac{D(1-D)T_sR_L}{2Ln^2}, \tag{2}$$

$$P_o = \frac{V_sV_oD(1-D)}{2nf_sL} \tag{3}$$

where D, T_s, and R_L are the regular duty cycle, the switching period, and the load resistance, respectively. V_s and V_o are the input voltage and the output voltage of the DAB converter. The buck-mode and the boost-mode operations of the DAB converter can be defined as $nV_s \geq V_o$ and $nV_s \leq V_o$, respectively. The currents causing the backflow power Q of the DAB converter are shown by the red areas in Figure 2 and their formulae are given by

$$\begin{cases} Q = \frac{nV_sV_o[M+(2D-1)]^2}{16f_sL(M+1)} & nV_s \geq V_o \\ Q = \frac{nV_sV_o\left[\frac{1}{M}+(2D-1)\right]^2}{16f_sL\left(\frac{1}{M}+1\right)} & nV_s < V_o. \end{cases} \tag{4}$$

The ZVS conditions of the DAB converter are given by

$$\begin{cases} D > \frac{1}{2}(1-M) & nV_s \geq V_o \\ D > \frac{1}{2}\left(1-\frac{1}{M}\right) & nV_s < V_o. \end{cases} \tag{5}$$

The ratio of the backflow power to the real power and ZVS condition are plotted within the M-D plane in Figure 3. It should be noted that the operating point moves into the non-ZVS region with high backflow power as the load decreases. Therefore, system efficiency is significantly reduced under light-load conditions for an SPS modulation of the DAB converter.

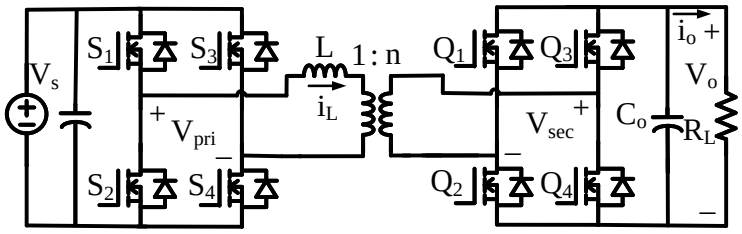
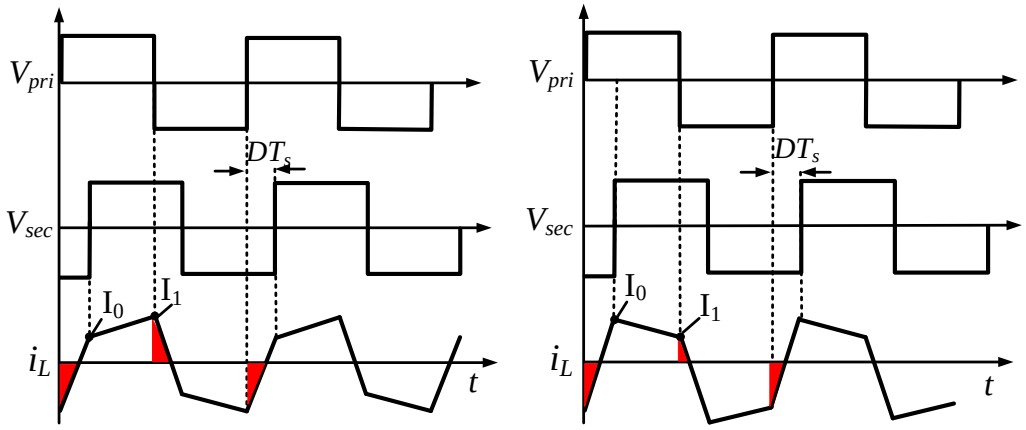


Figure 1. Isolated DAB converter.



(**a**) (**b**)

Figure 2. Key operation waveforms of the DAB converter with SPS modulation control: (**a**) buck operation mode and (**b**) boost operation mode.

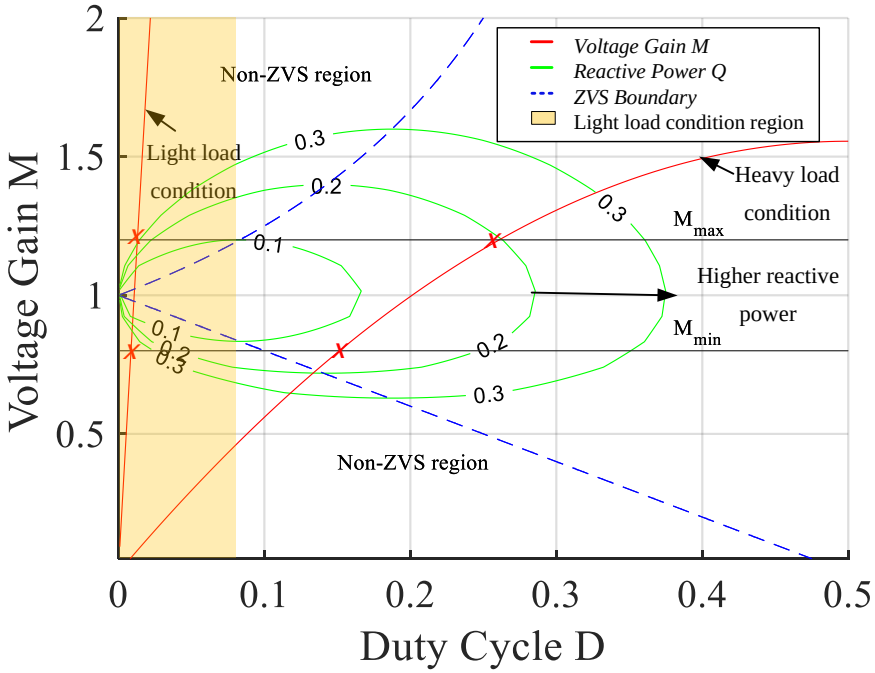


Figure 3. ZVS condition and backflow power for different voltage gains and load conditions.

3. Proposed Burst-Mode

3.1. Burst-Mode Operation

In this burst-mode operation, the PWM signal will be turned on with the burst-mode period T_b, and thus, the burst duty D_b is used as a control variable for regulating the output

voltage V_o, as shown in Figure 4. When the burst-mode is applied to the DAB converter, the voltage gain can be expressed as

$$M_b = MD_b. \tag{6}$$

Substituting (2) into (6), the voltage gain is derived as

$$M_b = \frac{D(1-D)T_sR_L}{2Ln^2}D_b. \tag{7}$$

It should be noted that the output voltage can be regulated by either the regular duty cycle, D, or the burst-mode duty cycle, D_b, as shown in Figure 5.

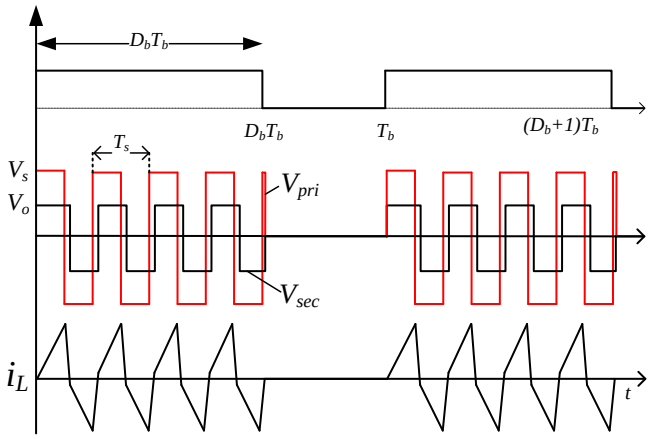


Figure 4. Burst-mode operation waveform.

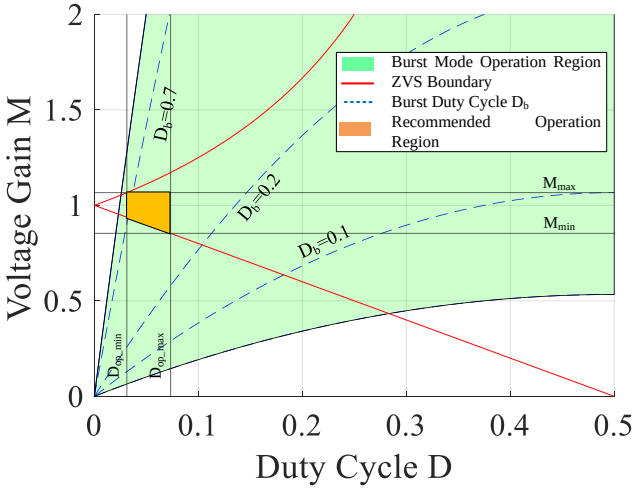


Figure 5. Determination of the operation region for proposed burst-mode control.

To minimize the backflow power in the burst-mode, the DAB converter should be operated at the optimally calculated duty cycle D_{op}. The optimal duty cycle D_{op} for the minimum backflow power of the DAB converter can be found when the backflow power in (4) is set to zero. As such, the optimal duty cycle D_{op} can be expressed as

$$\begin{cases} D_{op} = \frac{1}{2}(1 - M_b) & nV_s \geq V_o \\ D_{op} = \frac{1}{2}\left(1 - \frac{1}{M_b}\right) & nV_s < V_o. \end{cases} \tag{8}$$

While the minimum backflow power in burst-mode is achieved by D_{op}, the output voltage can be regulated by D_b. Substituting D_{op} into D in (7), the updated voltage gain formula, M_b is written as

$$M_b = \frac{D_{op}(1-D_{op})T_s R_L}{2Ln^2} D_b. \tag{9}$$

For widely varying output voltage application with maximum and minimum voltages, M_{max} and M_{min}, the maximum and minimum optimal duty cycles $D_{op,min}$ and $D_{op,max}$ can be calculated; thus, the recommended operation region can be determined as shown in Figure 5.

3.2. ZVS Condition

In the conventional way, ZVS condition in burst-mode can be given by

$$\begin{cases} D_{op} > \frac{1}{2}\left(1 - \frac{M_b}{D_b}\right) & nV_s \geq V_o \\ D_{op} > \frac{1}{2}\left(1 - \frac{D_b}{M_b}\right) & nV_s < V_o. \end{cases} \tag{10}$$

Substituting (10) into (9), the ZVS condition is found to be

$$\begin{cases} D_b > \frac{2Ln^2(1-2D_{op})}{D_{op}(1-D_{op})T_s R_L} & nV_s \geq V_o \\ D_b > \frac{2Ln^2}{D_{op}(1-2D_{op})(1-D_{op})T_s R_L} & nV_s < V_o. \end{cases} \tag{11}$$

This means that with the given load condition, the series inductor L can be optimally designed to achieve the ZVS condition. By performing this, minimum backflow and ZVS operation can be achieved simultaneously in the proposed burst-mode.

In the above conventional method, current direction is considered for deriving the ZVS condition. However, the positive or negative direction of the current does not always guarantee soft switching in MOSFETs [30,31]. To further elaborate on the ZVS condition, the energy in the output capacitors of the MOSFETs in the full-bridge should be considered as well [30,31]. As such, the ZVS condition is given by

$$\frac{1}{2}Li_L^2(t) \geq 2Q_{oss}(V_s)V_o \tag{12}$$

where $Q_{oss}(V_s)$ is the total stored charge of the output MOSFET capacitor C_{oss} at input voltage V_s. Substituting (1) into (12), the ZVS condition considering the parasitic capacitance is derived as

$$\begin{cases} D > \frac{1}{2}\left[1 - \frac{M_b}{D_b}\left(1 - \frac{8\sqrt{Q_{oss}(V_s)V_o L}}{V_s T_s}\right)\right] & nV_s \geq V_o \\ D > \frac{1}{2}\left[1 - \frac{D_b}{M_b}\left(1 - \frac{8n\sqrt{Q_{oss}(V_s)V_o L}}{V_o T_s}\right)\right] & nV_s < V_o. \end{cases} \tag{13}$$

The further updated optimal duty cycle D_{op} for ZVS and minimum backflow is given by

$$\begin{cases} D_{op} = \frac{1}{2}\left[1 - \frac{M_b}{D_b}\left(1 - \frac{8\sqrt{Q_{oss}(V_s)V_o L}}{V_s T_s}\right)\right] & nV_s \geq V_o \\ D_{op} = \frac{1}{2}\left[1 - \frac{D_b}{M_b}\left(1 - \frac{8n\sqrt{Q_{oss}(V_s)V_o L}}{V_o T_s}\right)\right] & nV_s < V_o. \end{cases} \tag{14}$$

The ZVS boundary considering the parasitic capacitances of the MOSFETs is shown as Figure 6. From (14), the adjusted voltage gain for achieving ZVS condition for the entire load condition M_{zvs} can be calculated as

$$M_{zvs} = \sqrt{\frac{1 - \frac{8\sqrt{Q_{oss}(V_s)V_o L}}{V_s T_s}}{1 - \frac{8n\sqrt{Q_{oss}(V_s)V_o L}}{V_o T_s}}}. \tag{15}$$

It should be noted that the value of M_{zvs} is not unity as is in the conventional method and is slightly shifted upward.

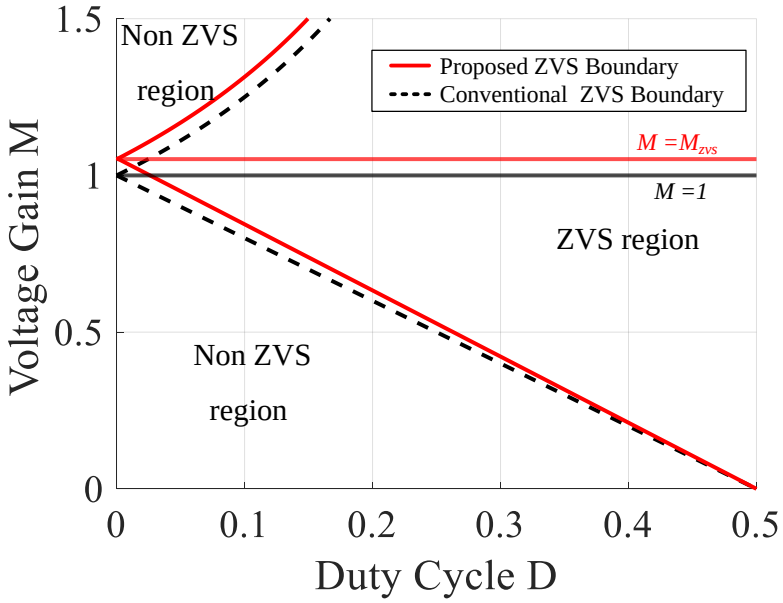


Figure 6. ZVS condition boundary with the new ZVS condition.

3.3. DC Bias Elimination

In the burst-mode operation, the series inductor current i_L jumps from zero to the burst-mode current. In this case, DC bias I_{DC} occurs as shown in Figure 7, which may cause transformer saturation [27,28]. To eliminate the DC bias current, the additional duty cycle D_x can be introduced to the optimal regular duty D_{op} to cancel this effect. The value of D_x can be calculated by simple algebraic manipulation.

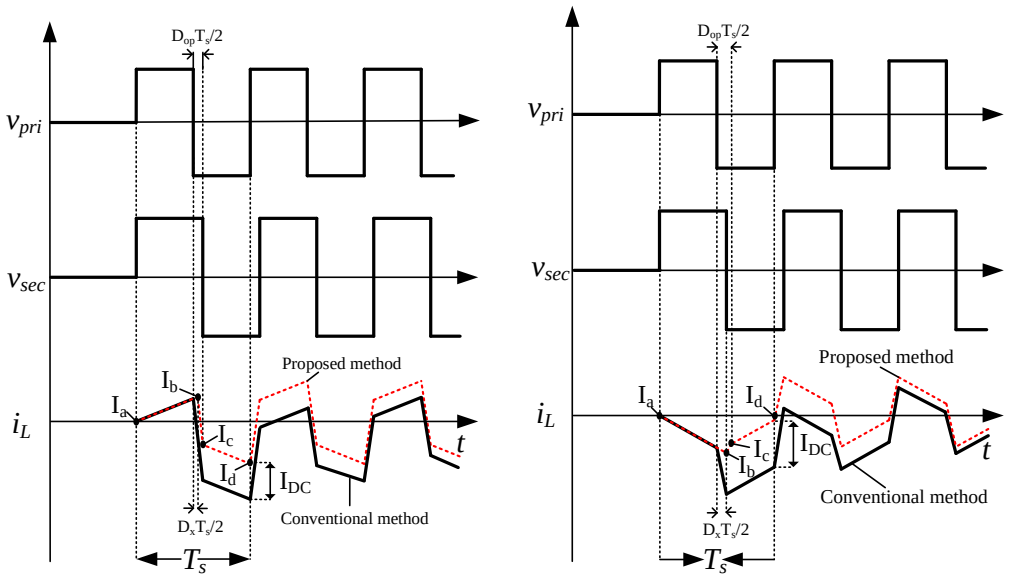


Figure 7. DC bias elimination key waveforms of the proposed burst-mode control in (**a**) buck operation mode and (**b**) boost operation mode.

In the burst-mode operation, the vertex value of the series inductor current i_L for both buck and boost mode can be expressed as follows:

$$
\begin{aligned}
I_a &= 0 \\
I_b &= I_a + \frac{nV_s - V_o}{L}(1 + D_x)\frac{T_s}{2} \\
I_c &= I_b - \frac{nV_s + V_o}{L}(D_{op} - D_x)\frac{T_s}{2} \\
I_d &= I_c - \frac{nV_s - V_o}{L}(1 - D_{op})\frac{T_s}{2},
\end{aligned} \tag{16}
$$

By arranging (16), the DC bias I_{DC} can be expressed as

$$I_{DC} = \left(D_x n V_s - D_{op} V_o\right)\frac{T_s}{L} \tag{17}$$

At steady state, when the DC bias is zero, the value of I_d can be expressed as

$$I_d = -\left[V_s + \frac{V_o}{n}(2D_{op} - 1)\right]\frac{T_s}{4L}. \tag{18}$$

By substituting (18) into (16), the value of D_x for zero bias current is given by

$$D_x = \frac{1}{4}\left(M(2D_{op} + 1) - 1\right) \tag{19}$$

In order to not disturb the optimal duty operation, the additional duty cycle is applied only for the first pulse of each burst-mode cycle, and its formula is given by

$$D_n' = D_{op} + D_x. \tag{20}$$

4. Design Procedure

Based on to the analysis in Section 3, we developed the design procedure, which is established in this section. Choosing a series inductance L is a critical design step, as it impacts power transfer, efficiency, and control dynamics. The series inductance L should enable efficient power transfer based on the converter's rated power, input and output voltage levels, and switching frequency. Upon rearranging the power transfer formula in (3), the series inductance L should be satisfied as

$$L \leq \frac{V_s V_o D(1 - D)}{2n f_s P_{o,max}}. \tag{21}$$

where $P_{o,max}$ is the output power at the maximum load condition. In the proposed burst-mode control, the DAB converter achieves the zero-voltage-switching (ZVS) condition and the minimum backflow power at the same time. Therefore, (12) should be satisfied when the series inductor current at optimal duty condition is given by

$$L \geq \frac{4Q_{oss}(V_s)V_o}{I_{L,ZVS}^2} \tag{22}$$

where $I_{L,ZVS} = \min(I_{o,D_{op}}, I_{1,D_{op}})$, $I_{0,D_{op}}$ and $I_{1,D_{op}}$ are series inductor currents at optimal duty D_{op}. With the combined condition of (21) and (22), the series inductor L of the DAB should be within the following specified range:

$$\frac{4Q_{oss}(V_s)V_o}{I_{L,ZVS}^2} \leq L \leq \frac{V_s V_o D(1 - D)}{2n f_s P_o}. \tag{23}$$

Choosing the burst-mode frequency f_b in burst-mode control is an important factor which directly affects the efficiency, output ripple, and response time of the power converter, particularly under light-load conditions. A higher f_b results in smaller output ripple voltage, but can lead to higher switching losses. Therefore, burst-mode frequency f_b should be chosen to balance those factors. In this paper, the burst-mode frequency is chosen as 2.5 kHz.

From the updated voltage gain formula in (9), it can be realized that when the duty cycle D is fixed at the optimal duty cycle D_{op} for the minimum backflow power, the burst duty cycle D_b should be used to regulate the output voltage while in the burst-mode, and it is determined by

$$D_b = \frac{2M_bLn^2}{D_{op}(1-D_{op})T_sR_L}. \tag{24}$$

As can be seen from (24), the burst-mode duty cycle D_b is a function of the load resistance R_L. It is well known that the range of the burst duty cycle is $0 \leq D_b \leq 1$. Therefore, the critical load value $R_{critical}$ for the mode switching between the burst-mode and the normal mode of the DAB converter is determined as shown in Figure 8a, and its formula is given by

$$R_{critical} = \frac{2M_bLn^2}{D_bD_{op}(1-D_{op})T_s}. \tag{25}$$

Notably, the output filter capacitor C_o plays a very important role in the burst-mode. Since the power is directly supplied from C_o to the load under the burst-mode, the maximum allowable output voltage ripple $V_{o,max}$ is directly related to the capacitance value of C_o, as shown below:

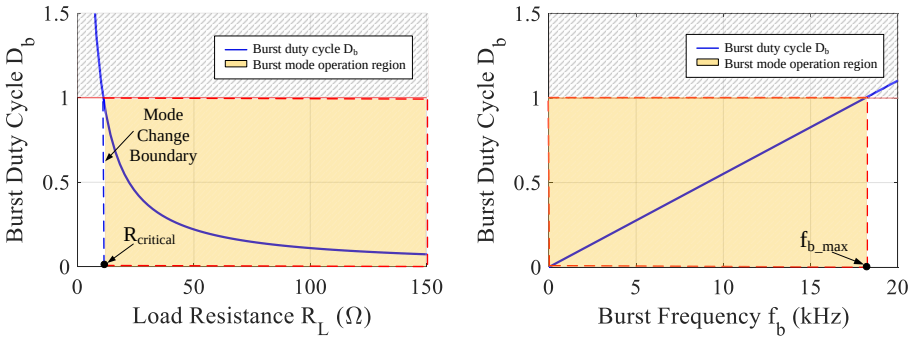
$$C_o = \frac{I_o}{(V_{o,max}-V_o)f_b}. \tag{26}$$

where I_o is the output current of the DAB converter. By substituting (26) into (24), the burst duty cycle D_b can be rewritten as

$$D_b = \frac{2M_bLn^2}{D_{op}(1-D_{op})T_s}\frac{f_bC_o(V_{o,max}-V_o)}{V_o}. \tag{27}$$

It should be noted that with a given maximum allowable output voltage ripple $V_{o,max}$, a higher f_b would lead to a smaller C_o. The burst-mode duty cycle D_b versus burst frequency f_b can be plotted as shown in Figure 8b; therefore, the burst-mode frequency f_b is also determined. The design process of the proposed burst-mode is shown in Figure 9 and detailed as follows:

Step 1: The initial system parameters such as V_s, V_o, P_o f_s, f_b, and $V_{o,max}$ are given by the system requirement.
Step 2: The value of inductance L can be calculated by (3).
Step 3: The voltage gain M_b and the optimal duty cycle D_{op} can be calculated by (2) and (14).
Step 4: The critical load resistance value $R_{critial}$ is calculated by (25).
Step 5: Output capacitor value C_o is calculated by (26).
Step 6: The value of series inductance L should be satisfied by (23). If it is not satisfied, then the design procedure is repeated from Step 3. If the condition is met, the design procedure is finished.



(**a**) (**b**)

Figure 8. (**a**) Critical load value $R_{critical}$ for mode change condition; (**b**) the burst-mode duty cycle D_b versus burst frequency f_b.

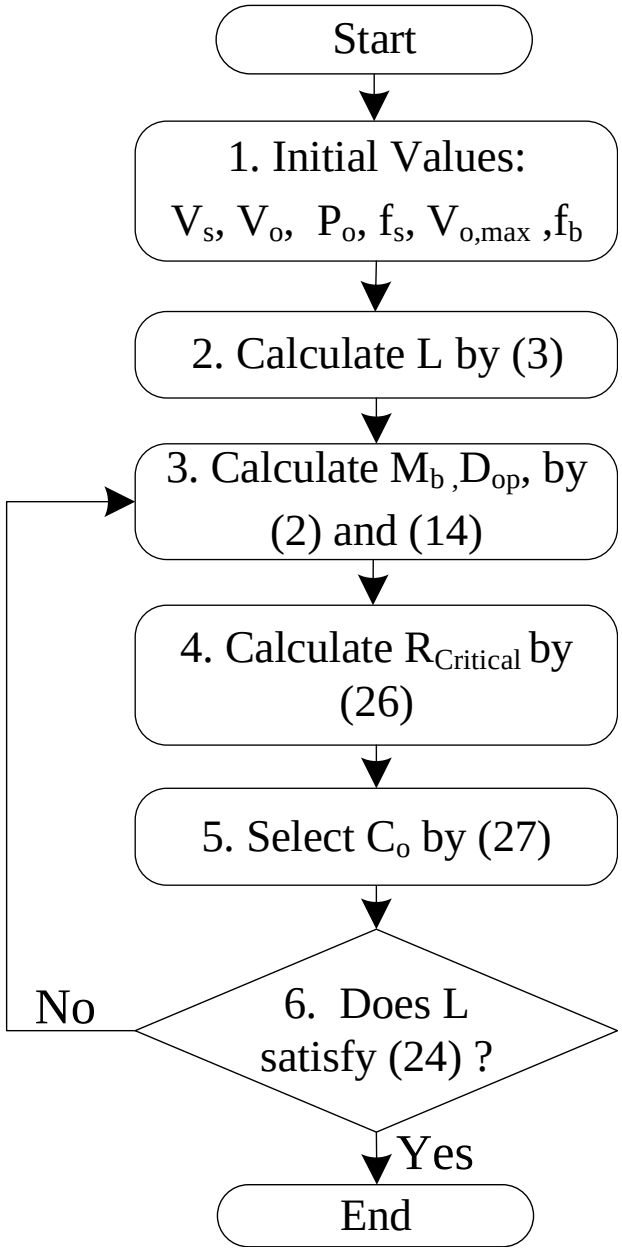


Figure 9. Design procedure of the proposed burst-mode method.

5. Control Mode Switching

The control mode sequence is presented in this section for the dynamic operation of the DAB converter. The critical value of the output current $I_{o,critical}$ can be calculated by the resistance value $R_{critial}$ and the output voltage V_o, which can be used for the mode change condition. Whenever the measured output current I_o is smaller than $I_{o,critical}$ the burst-mode is activated. The proposed burst-mode is, therefore, used as the optimal duty cycle D_{op} is calculated for minimum backflow power as well as the ZVS condition of the proposed burst-mode. The operation mode of the DAB converter for buck mode or boost mode is determined by comparing the value of nV_s with V_s. If $nV_s \geq V_o$, the buck operation mode is used; otherwise, the boost operation mode is applied. The DC bias current elimination is applied at the first switching period. Moreover, the output voltage V_o is regulated by the burst-mode duty cycle D_b. If I_o becomes larger than $I_{o,critical}$, the normal SPS mode is activated and the output voltage is regulated by the regulation duty cycle D. The burst-mode period T_b can be used as the update period for this sequence. The overall control flowchart of the proposed system is shown in Figure 10.

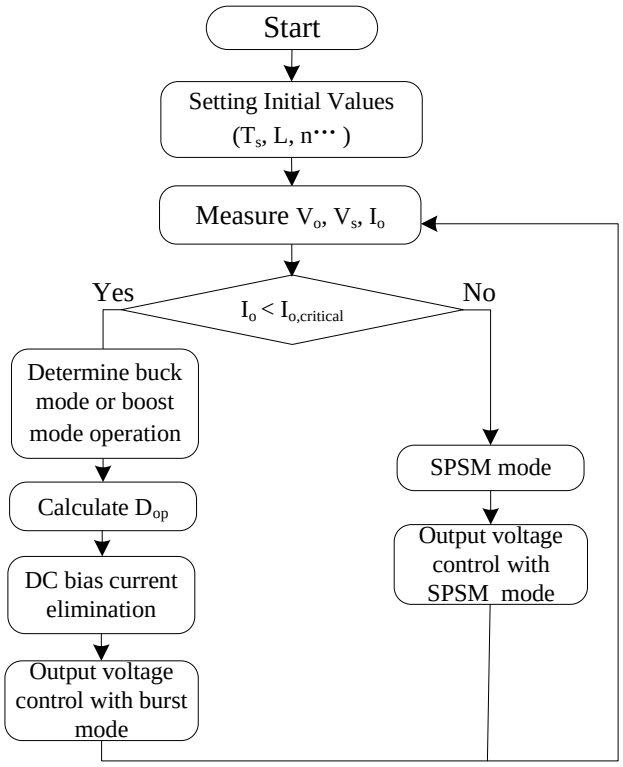
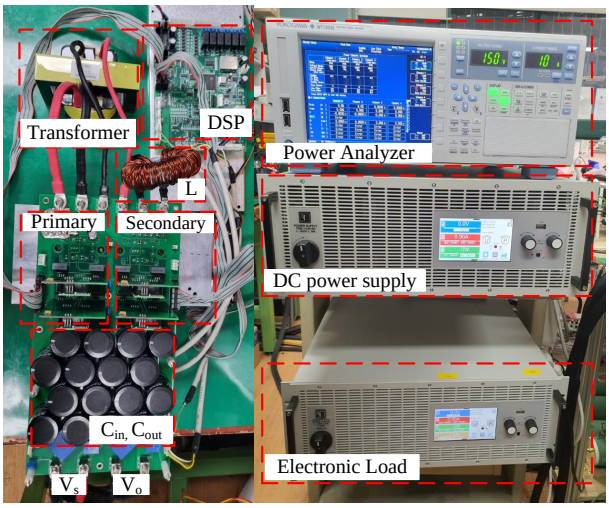


Figure 10. Proposed burst-mode control flowchart.

6. Experimental Verification

To verify the proposed control strategy, a 4 kW DAB converter prototype was built as shown in Figure 11. The design procedure in Section 4 is applied to design the system parameters shown in Table 2. The DSP (TMS320F28335 from Texas Instruments, Dallas, TX, USA) is used as the digital controller for algorithm implementation. The MOSFET module (F4-17MR12W1M1H B76 from Infineon, Augsburg, Germany) is used for the main power switches. A power analyzer (Yokogawa Electric, WT1804E, Tokyo, Japan) is used for efficiency measurement. Several experimental tests are conducted to verify the performance of the proposed burst-mode control, which have been performed with a buck-mode configuration.



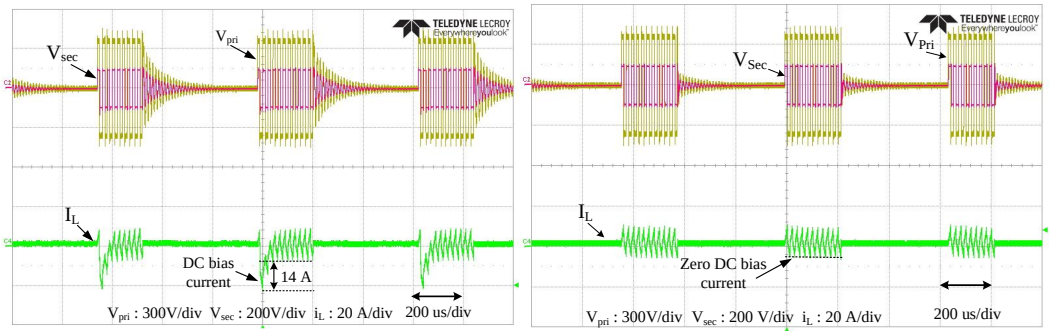
(**a**) (**b**)

Figure 11. Experimental setup: (**a**) prototype DAB converter; (**b**) DC power supply, electronic load, and measurement equipment.

Table 2. System parameters.

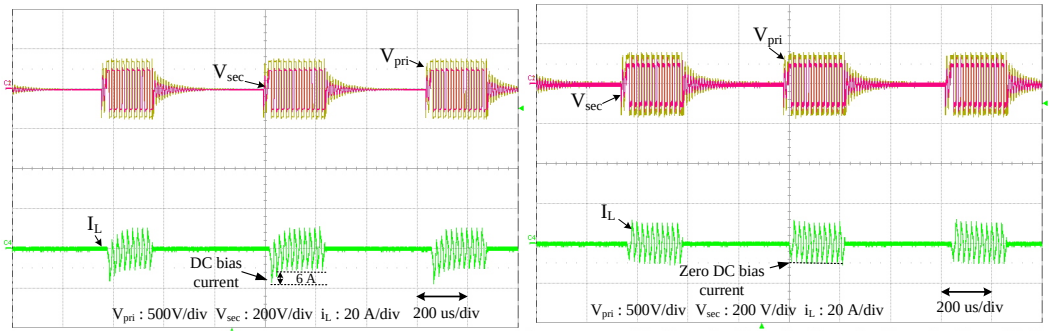
Symbol	Parameters	Values	Calculated	Unit
V_s	DC input voltage	400		V
V_o	DC output voltage	100–180		V
f_s	Switching frequency	50		kHz
P_o	Output power	0–4		kW
n	Transformer turn ratio	2:1		
C_o	Output filter capacitance	500	450	µF
L	Series inductance	50	44	µH
f_b	Burst frequency	2.5		kHz
$R_{critical}$	Critical value of load resistance	50	50.16	Ω

In case of the conventional burst-mode without DC bias elimination, there are 14 A DC and 6 A DC bias currents for buck and boost modes while starting up the PWM of the burst-mode as shown in Figures 12a and 13a. In the proposed method, after the DC bias current elimination is activated, there is zero bias current as shown in Figures 12b and 13b. Moreover, when SPS modulation is applied, the ZVS condition of switches S_1 and S_2 are similar with switches S_3 and S_4, and thus, only ZVS of switches S_1 and S_2 are checked. As shown in Figure 14a, ZVS is achieved at the primary side switches. Likewise, ZVS is achieved at the secondary side switches as shown in Figure 14b.



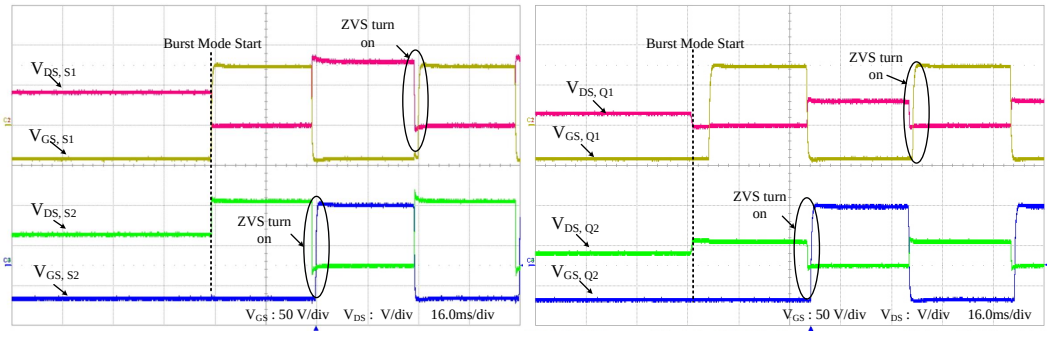
(**a**) (**b**)

Figure 12. Experimental waveforms of DC bias elimination for buck operation mode: (**a**) conventional burst-mode and (**b**) proposed burst-mode.



(**a**) (**b**)

Figure 13. Experimental waveforms of DC bias current elimination for boost operation mode: (**a**) conventional burst-mode and (**b**) proposed burst-mode.



(**a**) (**b**)

Figure 14. Experimental waveforms for ZVS of (**a**) primary side and (**b**) secondary side.

The step change of the output voltage V_o is also tested when V_{ref} steps up from 90 V to 120 V. The output voltage V_o can be regulated well with the reference value. Moreover, the optimal duty cycle D_{op} is changed from 0.275 to 0.2 when the V_o is increased from 90 V to 120 V, which matches well with the calculated value in Figure 15.

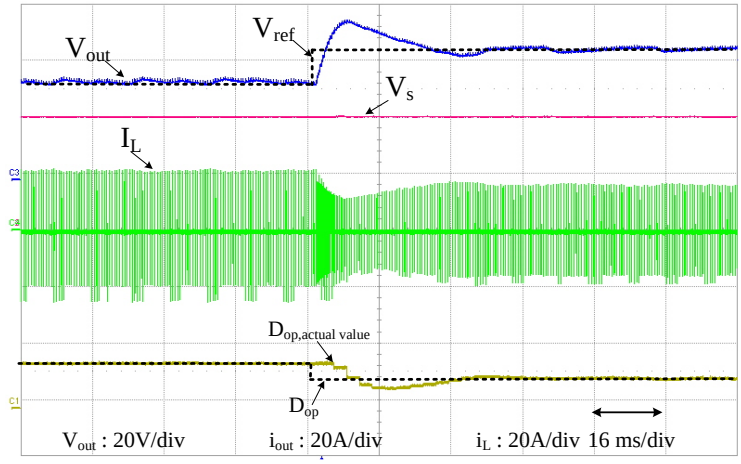


Figure 15. Experimental waveforms of the proposed burst-mode control when V_{ref} changes from 90 V to 120 V.

The load current is increased from 1.5 A to 3 A when the load resistance is changed from 80 Ω to 40 Ω. The undershoot of the output voltage is 4 V, which is 4% of the steady-state output voltage as shown in Figure 16.

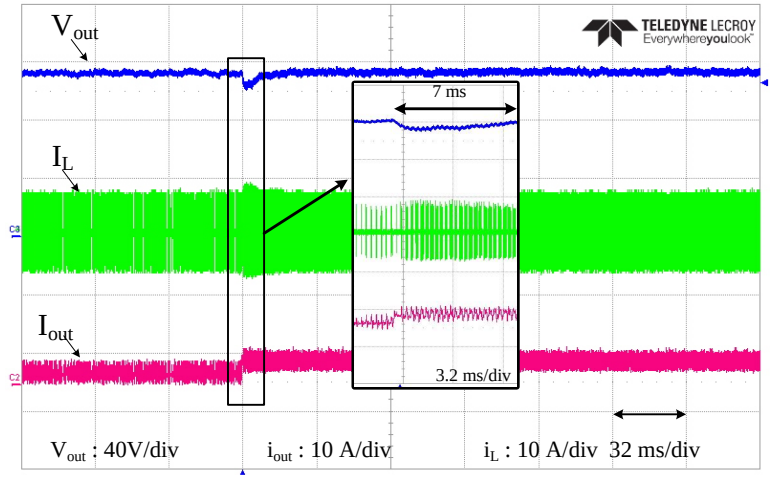
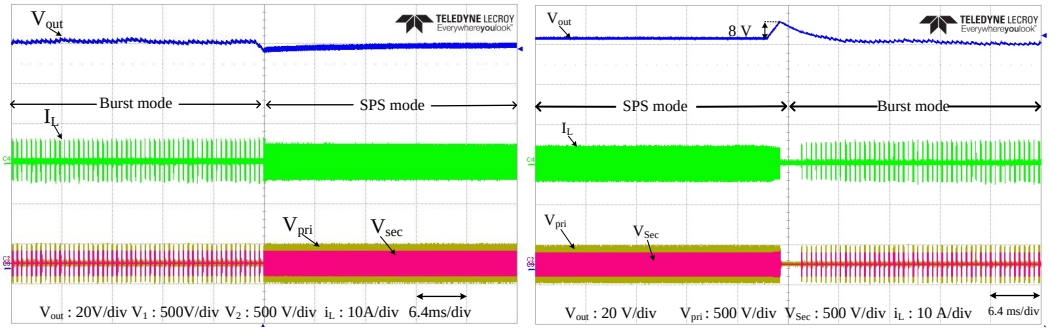


Figure 16. Experimental waveforms of DAB converter of the proposed burst-mode control when load changes from 80 Ω to 40 Ω.

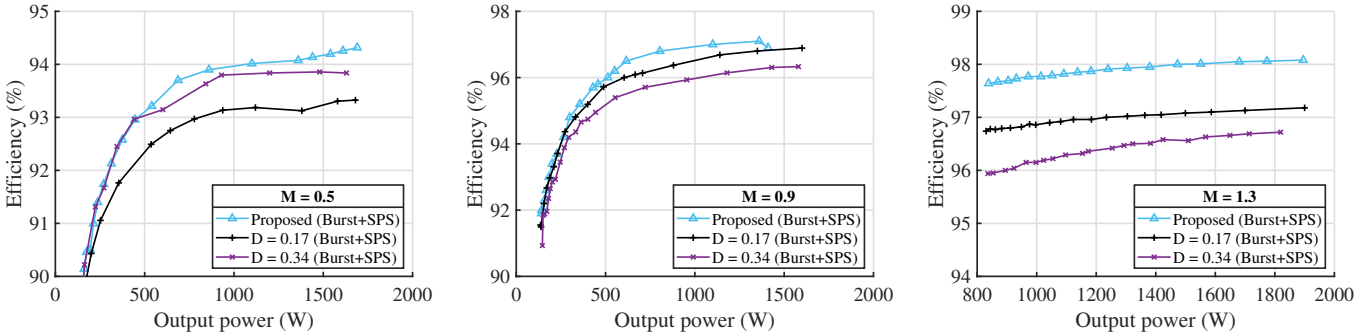
The mode switching operation of the proposed control strategy is also tested: burst-mode to normal mode and normal mode to burst-mode. In the case of burst-mode to normal mode, the load resistance is reduced from 80 Ω to 40 Ω when the output current changes from 1.5 A to 3 A. During the mode switching, the output voltage can be regulated with a slight undershoot as shown in Figure 17a. Moreover, in the case of normal mode to burst-mode, when the load resistance is increased from 40 Ω to 80 Ω, the output current changes from 3 A to 1.5 A. During the mode change, the output voltage can be regulated with a slight overshoot as shown in Figure 17b.



(**a**) (**b**)

Figure 17. Experimental waveforms of the mode switching (**a**) from burst-mode to normal mode and (**b**) from the normal mode to burst-mode.

The three different voltage gains M = 0.5, 0.9, and 1.3 are tested to verify the effectiveness of the proposed burst-mode control method over the conventional method. In the proposed burst-mode control, the duty cycle D is equal to the optimal duty cycle D_{op} which is equal to 0.256, 0.06, and 0.116 while M = 0.5, 0.9, and 1.3, respectively. However, the duty cycle D is fixed for all voltage gain conditions in conventional burst-mode control, which is 0.17 and 0.34. Due to the ZVS operation and minimum backflow power, the efficiency of the proposed method is always higher than conventional burst-mode control as shown in Figure 18. The efficiency improvement of the proposed burst-mode control can be more significant, in case higher-frequency operations are used due to the whole-load range ZVS feature.



(**a**) (**b**) (**c**)

Figure 18. Efficiency measurement comparison for (**a**) M = 0.5 (**b**) M = 0.9 (**c**) M = 1.3.

7. Conclusions

In order to achieve ZVS for the whole operation range and improve efficiency of light-load conditions, the burst-mode for the SPS modulation of the DAB converter is proposed in this paper. With the proposed burst-mode, the DAB converter is operated with minimum backflow power as well as achieving ZVS under light-load conditions. Therefore, the system efficiency is significantly improved. The DC bias current issue of the conventional burst-mode is also mitigated in the proposed method. The detailed analysis

of proposed burst-mode operation of the DAB converter is derived for both buck and boost operation modes. The detailed design procedure of the DAB converter for the burst-mode control is also presented. Moreover, the proposed burst-mode control flowchart is also presented for achieving ZVS in all load conditions. Therefore, the efficiency of the whole load range condition is also improved. The effectiveness of the proposed burst-mode is verified by experiment. The system efficiency can be improved by 2% compared with the conventional burst-mode method.

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Conflicts of Interest: The authors declare no conflicts of interest.

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