Planar Transformer Design and Optimization for Isolated Partial-Power Processing Converters

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***Abstract*—In Battery Energy Storage Systems (BESS), partial-power processing architecture is used to reduce the fraction of total power processed by the converter to attain high system efficiency. Moreover, galvanic isolation is essential to interface widely separated voltage domains of battery and DC bus, and for operational safety to prevent ground loop short-circuit fault. Conventional wirewound transformers are bulky with comparably higher leakage inductance, resulting in reduced power density. Therefore, this article presents a design framework for partial power processing planar transformer to select winding turns with current density consideration while satisfying flux-density and window utilization limits. The merits of reduced volume profile for compactness and lower leakage are presented. Finite-element analyses simulation and physical implementation are carried out. The designed planar transformer exhibits substantially lower leakage inductance and achieves a $67.6\,\%$ volume reduction, demonstrating increased compactness for integration into partial-power processing converters.**

I. Introduction

The deployment of large-scale battery energy storage systems (BESSs) in renewable-energy applications places demands on the DC–DC bus converter interface as high efficiency must be maintained and galvanic isolation must withstand ground fault occurrence [1]. Meeting these simultaneously through conventional full-power conversion is increasingly impractical because losses scale with processed power and because the isolation transformer becomes prohibitively large at multi-kilowatt levels.

Partial-power-processing (PPP) architectures, hence, resolve this limitation by routing only a fraction of the system power through the converter while passing the remainder along a direct path between source and load [2]. Partial-power-processing ratio is also determined as $K_p = V_\Delta/V_{\rm bus}$. As K_p reduces, the system efficiency then approaches unity in $\eta_s = \eta_c/(K_p+(1-K_p)\eta_c)$, such that even when converter efficiency η_c deviates system efficiency is still maintained whenever K_p is small.

Planar transformer in the PPP converter design as shown in Fig. 1 (a), therefore, presents the following benefits:

- The flat winding stack combined with the planar core geometry enables profile and volume reductions. Hence, compact PPP converter benefits from this volume-oriented design.
- Reduced leakage inductance from interleaving the primary and secondary layers suppresses leakage inductance-induced voltage spikes at switch-off.

However, planar windings are strongly capacitively coupled by virtue of their broad overlap area and thin dielectrics. As demonstrated in Fig. 1 (b), interwinding capacitance $C_{\rm ps}$ and self capacitances $C_{p,\rm self}, C_{s,\rm self}$ inflate the parallel Q-factor due to dominant self-resonant frequency peak of the transformer, affecting the converter efficiency η_c. Nonetheless, η_s is barely affected by this trade-off.

II. Planar Transformer Design Framework

In parellel-input-series-output PPP architecture considered in this study as illustrated in Fig. 1, the battery is paralleled across the

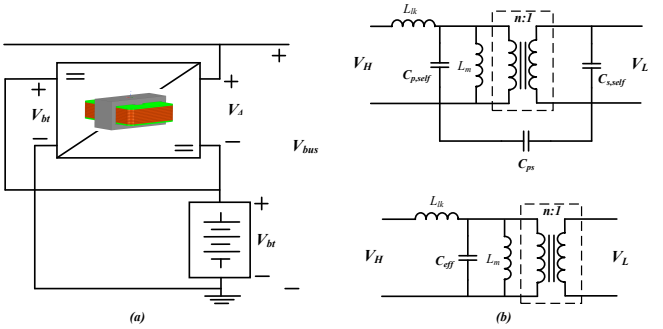

Fig. 1. Illustration of (a) partial power processing architecture with planar transformer FEA design, and (b) transformer parasitics effect in planar transformer.

converter input and the converter output is placed in series with the bus port [3]. The primary-side ($V_{\rm H}$) and secondary-side ($V_{\rm L}$) terminal voltages of the transformer are $V_{\rm H} = V_{\rm bt} = V_{\rm bus}(1-K_p), V_{\rm L} = V_\Delta = K_p V_{\rm bus}$ and the nominal turns ratio is $n = N_p/N_s = V_{\rm H}\kappa/V_{\rm L}$, where κ is the topology-dependent conversion factor discussed in [4], [5]. The factor κ envelopes the fraction of the high-side voltage actually presented across the transformer primary and the fraction of the transformer secondary voltage delivered to the load per switching half-cycle. The target turns ratio depends on $K_{p,\rm nom} = (V_{\rm bus} - (V_{\rm bt,min} + V_{\rm bt,max})/2)/V_{\rm bus}$ and the topology factor

$$n_{\rm target} = \frac{1-K_{p,\rm nom}}{K_{p,\rm nom}}\,\kappa. \tag{1}$$

The minimum primary turns are calculated as

$$N_{p,\rm min} = \frac{V_{\rm bus}(1-K_{p,\rm max})\,D_{\rm max}}{C_f\,f_{\rm sw}\,B_{\rm max}\,A_e}, \tag{2}$$

where the Faraday volt-second balance for bipolar core excitation, with topology volt-second coefficient $C_f = n_{\rm act}\alpha_b$, where $n_{\rm act}$ is the number of active half-cycles per period and α_b accounts for the bipolar flux swing $\Delta B = 2B_{\rm pk}$. C_f values for common topologies such as full-bridge, half-bridge, push–pull yields $C_f = 4$ because they exercise both flux polarities [4]. The peak flux density for $N_p \geq N_{p,\rm min}$ follows by inversion

$$B_{\rm pk} = \frac{V_{\rm bus}(1-K_{p,\rm max})\,D_{\rm max}}{C_f\,f_{\rm sw}\,N_p\,A_e} \leq B_{\rm max}, \tag{3}$$

where $N_p > N_{p,\rm min}$ is desirable for core loss derating as it reduces the peak flux.

With $k_{w,p}$ and $k_{w,s}$ as the topology-specific waveform correction factors for a half-bridge topology as 1 and $1/\sqrt{D_{\rm max}}$, respectively, [5], RMS winding currents are determined as

$$I_{p,\rm rms} = k_{\rm w,p}\,\frac{K_{p,\rm max}\,P_s}{V_{\rm bus}(1-K_{p,\rm max})\,\eta_c}, I_{s,\rm rms} = k_{\rm w,s}\,\frac{P_s}{V_{\rm bus}\,\eta_c}. \tag{4}$$

Table I: System specifications

Parameter	Symbol	Value
DC bus voltage	V_{bus}	380 V
Battery voltage range	V_{bt}	350 −360 V
Headroom voltage range	V_{Δ}	20 −40 V

Table II: Comparison of planar transformer with conventional wire-wound transformer

Parameter	Conventional	Planar	Change
Volume	$1\,258\,\mathrm{cm}^3$	$408\,\mathrm{cm}^3$	−67.6%
Leakage inductance	10.8 µH	4.0 µH	−63.0%
C_{eff}	114.55 pF	379.20 pF	+231.03%

Taking the secondary-to-primary current ratio,

$$\frac{I_{s,\mathrm{rms}}}{I_{p,\mathrm{rms}}} = \frac{k_{\mathrm{w},s}}{k_{\mathrm{w},p}} \frac{n_{\mathrm{target}}(K_{p,\max})}{\kappa}, \tag{5}$$

for $K_{p,\max} \ll 1$ gives $I_{s,\mathrm{rms}} \gg I_{p,\mathrm{rms}}$, confirming the asymmetric winding sizing for primary and secondary windings.

The asymmetry seen in (5) propagates directly to the planar copper geometry. For a rectangular cross-section of copper thickness h_c and trace width w, the cross-sectional area is wh_c, and the current-density limit $J_{\max}$ imposes a lower bound on w on each side. The per-conductor current-density constraints become

$$\frac{I_{p,\mathrm{rms}}}{w\,h_c} \le J_{\max}, \qquad \frac{I_{s,\mathrm{rms}}}{w\,h_c} \le J_{\max}. \tag{6}$$

The window utilization K_u sums the primary and secondary cross-sections and is bounded by the maximum $K_{u,\max}$ as

$$K_u = \frac{N_p\,w\,h_c + N_s\,w\,h_c\,n_{\mathrm{par}}}{A_w} \le K_{u,\max}, \tag{7}$$

while geometric clearance to the core leg and inter-winding creepage d_{clear} confines w within the available window breadth $w_{\max}(c)$ as $w \le w_{\max}(c) - 2\,d_{\mathrm{clear}}$. Combining with (6) yields a feasible winding-width band $w_{low} \le w \le w_{up}$, where the lower and upper width bounds are, respectively,

$$w_{low} = \max\left(\frac{I_{p,\mathrm{rms}}}{J_{\max}\,h_c}, \frac{I_{s,\mathrm{rms}}}{J_{\max}\,h_c}\right), \tag{8}$$

$$w_{up} = \min\left[w_{\max}(c) - 2\,d_{\mathrm{clear}}, \frac{K_{u,\max}\,A_w}{h_c\,(N_p + N_s\,n_{\mathrm{par}})}\right]. \tag{9}$$

III. Simulation Verification

Specifications provided in Table I are used to perform verification for the planar transformer design. An ELP $102/20/38$ core is used. With $K_{p,\max} = 0.078$, the minimum primary turns from (2) evaluates to $N_{p,\min} = 1.99$, hence $N_p = 14$ is chosen and the turns ratio $N_p/N_s = 2$.

Fig. 2(a) finite-element-analysis (FEA) simulation shows the flux is well confined to the core, and the peak flux density in the centre limb remains below the ferrite saturation limit while Fig. 2(b) shows the current density is uniformly distributed along the conductor width, indicating that interleaving the primary and secondary layers effectively suppresses proximity-effect and that the winding width sits comfortably within the $[w_{low}, w_{up}]$ feasibility band. Fig. 2(c) illustrates the volume comparison between the conventional wire-wound transformer and the planar transformer of equal rating, showing the substantial profile reduction enabled by the planar geometry. Table II summarizes the comparison of the designed PPP planar transformer with a conventional transformer under the same specifications.

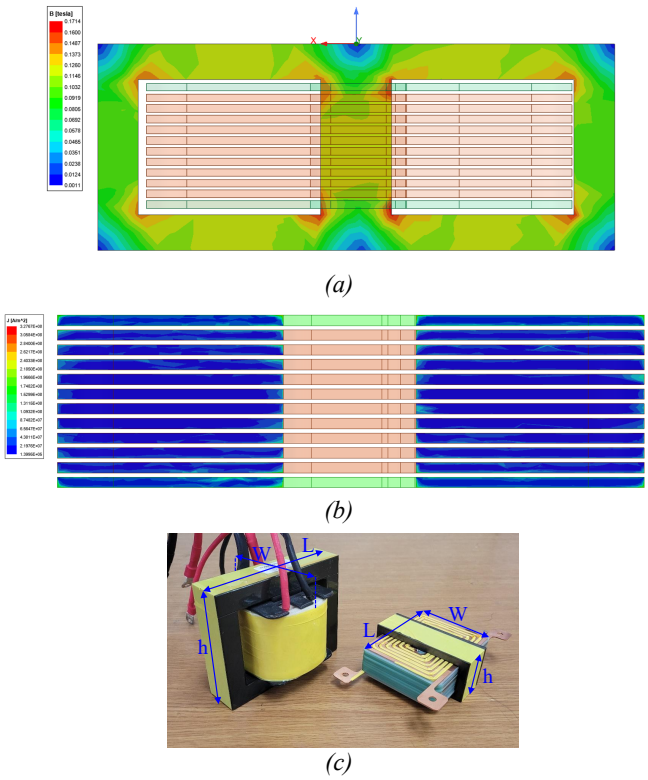

Fig. 2. Ansys FEA simulation results of (a) magnetic flux distribution, and (b) windings current density distribution. (c) Volume comparison.

IV. Conclusion

This article presents a planar transformer design approach for isolated PPP converters by considering power processing ratio effect, flux-density constraint, and a jointly imposed current-density and window-utilization constraint that bounds the feasible winding. The FEA simulation results show that this framework yields a feasible transformer design that is compact for the same converter rating, has reduced leakage inductance, and makes it well suited for battery energy storage system applications where isolation and high voltage conversion ratio are required. Future work will develop the design framework in detail with optimization and hardware verification.

Acknowledgement

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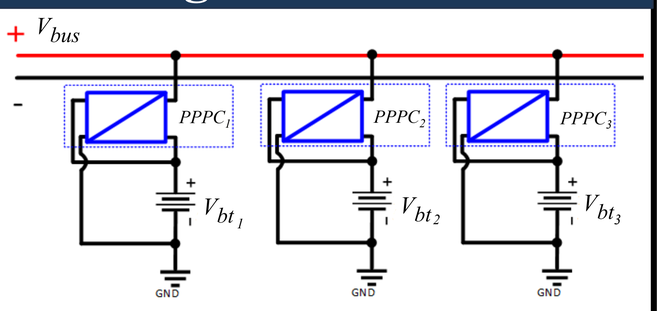
1. Introduction

- In parallel battery energy management systems (BESS), bus interface converters with **high efficiency** are essential, necessitating the application of partial-power processing converters (PPPC) that are able to handle **high voltage gain**.
- Conventional wire-wound transformers meet these requirements at the cost of **bulkiness**, higher **leakage inductance**, and reduced **power density**.
- Planar transformer winding stacks and planar core geometry leads to **low-profile**, volume-oriented **compact** design, and interleaving **reduces leakage inductance**, suppressing switch-off voltage spikes.
- This paper presents a design and optimization framework for a 1 kW PPPC planar transformer that selects winding turns, winding copper trace dimensions and winding loss while jointly satisfying flux density, current density and window utilization. The framework is formulated as a mixed-integer multi-objective nonlinear programme over loss, leakage inductance and effective capacitance.

2. Planar Transformer Design Framework

- In this study, input-parallel-output–series (IPOS) PPP architecture is the target system with a half-bridge push-pull converter topology where the battery is paralleled across the converter input, and the converter output is placed in series with the bus port.



Input-parallel-output–series (IPOS) partial-power processing architecture.

- Transformer **terminal voltages** are

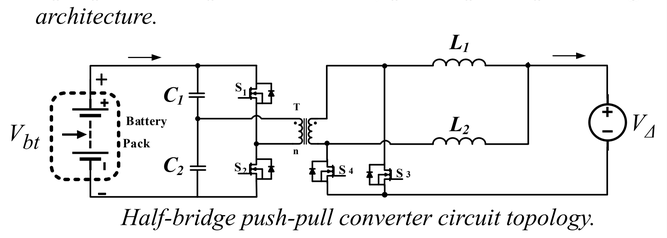
$$V_H = V_{bt} = V_{bus}(1-K_p), \quad V_L = V_\Delta = K_p V_{bus},$$

where $n = \frac{N_p}{N_s} = \frac{V_H \kappa}{V_L}$,

$$K_p = \frac{V_\Delta}{V_{bus}},$$

and $\kappa = 1/2$ is half-bridge topology conversion factor. With $K_{p,nom} = (V_{bus} - (V_{bt,min} + V_{bt,max})/2)/V_{bus}$, the target turns ratio is

$$n_{target} = \frac{1-K_{p,nom}}{K_{p,nom}}\kappa.$$



Half-bridge push-pull converter circuit topology.

- **Minimum primary turns** from the Faraday volt-second balance for bipolar core excitation, with volt-second coefficient $C_f = 4$

$$N_{p,min} = \frac{V_{bus}(1-K_{p,max})D_{max}}{C_f f_{sw} B_{max} A_e},$$

and choosing $N_p > N_{p,min}$ derates core loss by reducing the **peak flux density**

$$B_{pk} = \frac{V_{bus}(1-K_{p,max})D_{max}}{C_f f_{sw} N_p A_e} \le B_{max}.$$

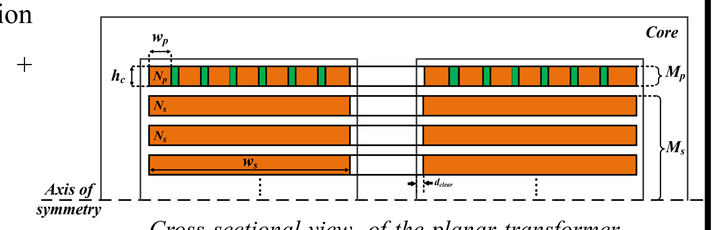
- **RMS winding currents**, with topology-specific waveform correction factors $k_{w,p} = 1$ and $k_{w,s} = 1/\sqrt{D_{max}}$ for a half-bridge are obtained as

$$I_{p,rms} = k_{w,p}\frac{K_{p,max}P_s}{V_{bus}(1-K_{p,max})\eta_c},$$

$$I_{s,rms} = k_{w,s}\frac{P_s}{V_{bus}\eta_c}$$

- **Secondary-to-primary current ratio** for $K_{p,max} \ll 1$, produces $I_{s,rms} \gg I_{p,rms}$, confirming asymmetric sizing of the primary and secondary windings

$$\frac{I_{s,rms}}{I_{p,rms}} = \frac{k_{w,s}}{k_{w,p}}\frac{1-K_{p,max}}{K_{p,max}} = \frac{1-K_{p,max}}{K_{p,max}\sqrt{D_{max}}}.$$



Cross-sectional view of the planar transformer winding geometry.

- **The window-fill factor** is

$$K_{u,fill} = \frac{N_p w_p h_c + N_s w_s h_c}{A_{w,eff}} \le K_{u,max},$$

where current-density limits impose lower bounds on conductor of feasible width

$$w_{low} \le w \le w_{up},$$

given copper thickness h_c,

$$\frac{I_{p,rms}}{w_p h_c} \le J_{max}, \qquad \frac{I_{s,rms}}{w_s h_c} \le J_{max}.$$

- **The copper loss** is

$$P_{cu} = k_{ac,p} I_{p,rms}^2 (R_{p,tr} + R_{via,p}) + k_{ac,s} I_{s,rms}^2 (R_{s,tr} + R_{via,s}), \ldots(1)$$

with the trace DC resistances

$$R_{p,tr} = \frac{\rho_{Cu} N_p \ell_T}{w_p h_c}, \qquad R_{s,tr} = \frac{\rho_{Cu} N_s \ell_T}{w_s h_c},$$

where ℓ_T is the mean turn length.

- **The core loss** through Steinmetz expression is

$$P_{core} = k_c f_{sw}^{\alpha} B_{pk}^{\beta} V_{e,pair}, \ldots(1)$$

where k_c, α and β are Steinmetz coefficients of the ferrite core.

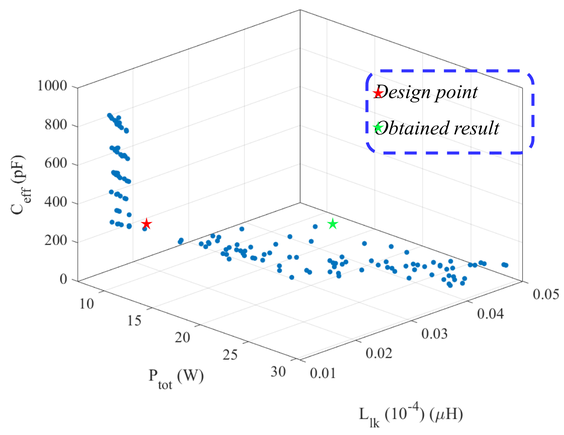
3. Multi-objective Optimization

- With design variables of the transformer being both continuous and discrete, design problem is therefore a multi-objective mixed-integer non-linear programme (MO-MINLP),

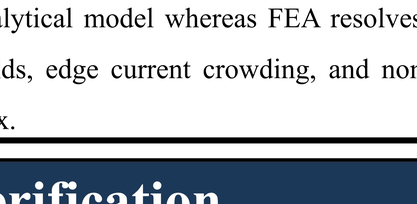
$$\min_{\boldsymbol{x}} \quad \boldsymbol{f}(\boldsymbol{x}) = [f_1(\boldsymbol{x}), f_2(\boldsymbol{x}), f_3(\boldsymbol{x})]^\top,$$
$$\text{s.t.} \quad \boldsymbol{g}(\boldsymbol{x}) \le \boldsymbol{0}, \quad h(\boldsymbol{x}) = 0,$$
$$\boldsymbol{x}_c \in [\boldsymbol{x}_c^L, \boldsymbol{x}_c^U] \subset \mathbb{R}^{n_c},$$
$$\boldsymbol{x} = [h_c, w_p, w_s, N_p, N_s, M_p, M_s]^\top$$

where the figures of merit to be minimized are

$$f_1(\boldsymbol{x}) = P_{tot}(\boldsymbol{x}) = P_{cu}(\boldsymbol{x}) + P_{core}(\boldsymbol{x}), \ldots(1)$$
$$f_2(\boldsymbol{x}) = L_{lk}(\boldsymbol{x}), \ldots(2)$$
$$f_3(\boldsymbol{x}) = C_{eff}(\boldsymbol{x}), \ldots(3)$$



Pareto front for the MO-MINLP *(200 samples).*



Transformer parasitics effect in planar transformer.

- The primary-referred effective capacitance is

$$C_{eff} = \frac{(M_p + M_s - 1)C_{ps}}{n^2}, \ldots(3)$$

where M_P and M_s are the primary and secondary layer counts, and C_{Ps} is the interwinding capacitance

$$C_{ps} = \frac{\varepsilon_0 \varepsilon_r w_s \ell_T}{t_d}.$$

- The primary-referred leakage inductance of the interleaved stack is

$$L_{lk} = \frac{\mu_0 N_p^2 \ell_T}{3 M_{tot}^2} \cdot \frac{t_d}{w_s}, \ldots(2)$$

where t_d is the dielectric thickness and M_{tot} is total winding layer count.

- The obtained result deviates from the optimal design point since the optimization employs ideal analytical model whereas FEA resolves fringing fields, edge current crowding, and non-uniform flux.

4. Simulation Verification

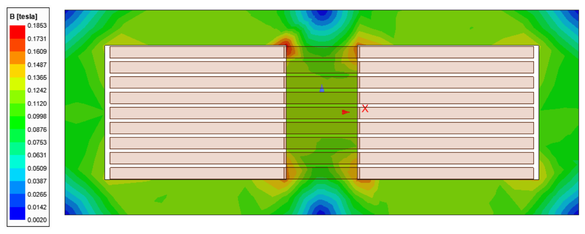
Table 1. System specifications

Parameter	Symbol	Value
DC bus voltage	V_{bus}	380 V
Battery voltage range	V_{bt}	350-360 V
Headroom voltage range	V_Δ	20-30 V
Frequency	f_{sw}	100 kHz

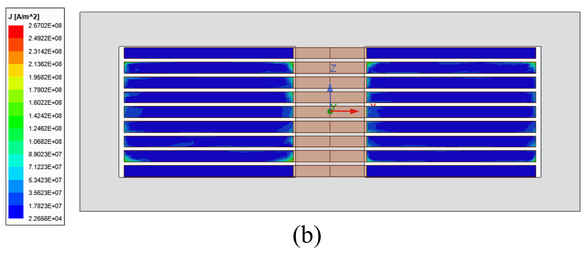
- FEA verification via Ansys Maxwell 3D is carried out with an ELP 102/20/38 core.
- $M_p = 2$ and $M_s = 7$
- $K_{p,max} = 0.078$ gives $N_{p,min} = 1.83$, hence $N_p = 14$ turns chosen to derate core loss, thus turns ratio $n = 2$.
- Flux is well confined to the core as centre-limb peak flux stays below the ferrite saturation limit.
- Uniform current density is observed as interleaving suppresses proximity effect; w sits within w_{low} and w_{up}.
- 67.6% volume and 63.0% leakage-inductance reductions are obtained compared to a wire-wound of equal rating.

Table 2. Comparison of planar transformer with conventional wire-wound transformer

Parameter	Conventional	Planar
Core volume	*1258 cm³*	*408 cm³*
L_{lk}	*10.8 µH*	*4.0 µH*
C_{eff}	*114.55 pF*	*379.20 pF*



(a)



(b)

Ansys FEA simulation results of (a) magnetic flux distribution, and (b) winding current density distribution.

5. Conclusion

- A planar transformer design and optimization framework for PPP converters is presented.
- The PPP ratio effect, flux-density constraint, and jointly imposed current-density and window-utilization limits bound the feasible winding,
- FEA verification shows compact, low-leakage design with 67.6% volume, and 63.0% leakage reduction for the same converter rating, well suited to BESS demanding high voltage conversion ratio.
- The parasitic capacitances inflate the parallel Q factor of the transformer, eroding the converter efficiency η_c. However, η_s is barely affected by this trade-off.
- Future work: detailed development of the framework with hardware verification.