Equivalent Resistance-Based Design Optimization of Switched-Capacitor Battery Cell Equalizers for Faster Balancing

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ABSTRACT

Maintaining cell equilibrium within a battery pack is critical for maximizing usable capacity and mitigating capacity fade. Active balancing topologies are widely studied for their ability to redistribute energy between cells. Among these, the switched capacitor (SC) architecture is frequently utilized due to its hardware simplicity and cost-effectiveness. However, the efficiency and reliability of SC balancers are heavily dependent on precise capacitor selection. This paper presents a comparative analysis and a design framework for evaluating capacitor parameters based on the analysis of worst case high-frequency ripple current and the maximum voltage differentials between adjacent cells. By focusing on the relationship between capacitance, switching frequency, and voltage differentials, this study establishes criteria for selecting capacitors that optimize balancing speed while maintaining voltage stability. This study explores a simplified design approach that may assist in identifying capacitor requirements, providing a basis for further optimization of SC balancing circuits.

1. INTRODUCTION

Lithium battery packs are widely used in electric vehicles, renewable energy systems, and portable electronics due to their high cell voltage and energy efficiency [1]. However, voltage imbalance between cells during charging and discharging can lead to overcharge, undercharge, and reduced battery lifespan [2]. Switched capacitor active equalizers are widely adopted because of their low cost, simple control, and low energy loss. In this work, the switched capacitor equalizer is modeled as an equivalent resistance to simplify design trade-off analysis. The effects of switching frequency and capacitance on the equivalent resistance are evaluated, and a two cells simulation model is developed to investigate equalization performance and efficiency.

2. PROPOSED METHOD

For a switched capacitor equalizer with two cells, the balancing capacitor is charged in one half-cycle and is discharged during the other half-cycle. According to [2] and [3], in a periodic steady state, capacitor voltage alternates between V_{c1}, the voltage at the end of the charge half-cycle, and V_{c2}, the voltage at the end of the discharge half-cycle. Assuming both half-cycles have the same duty cycle D, the relationship between the cell's open circuit voltage and capacitor voltage in steady state can be described as:

$$V_{c1} - V_{c2} = (V_{b1} - V_{b2}) \frac{e^{\frac{D}{fRC}} - 1}{e^{\frac{D}{fRC}} + 1} \quad (1)$$

where V_{b1} and V_{b2} are the open circuit voltages of battery cell 1 and 2 respectively, V_{c1} and V_{c2} are the capacitor voltages at the end of the charging and discharging half-cycles respectively, f is the switching frequency, C is the balancing capacitance and R is the total resistance between the battery cells and capacitor, including capacitor ESR, switch resistance, and battery internal resistance. Using (1), the average charge-transfer current per cycle is given by (2):

$$I = fC(V_{c1} - V_{c2}) = fC\Delta V_c \quad (2)$$

A switched capacitor equalizer for two battery cells can be modeled as two cells connected by an equivalent resistance. Combining equations (1) and (2), an expression for equivalent resistance can be obtained:

$$R_{eq} = \frac{(V_{b1} - V_{b2})}{I} = \frac{1}{fC} \frac{1 + e^{-\frac{D}{fRC}}}{1 - e^{-\frac{D}{fRC}}} \quad (3)$$

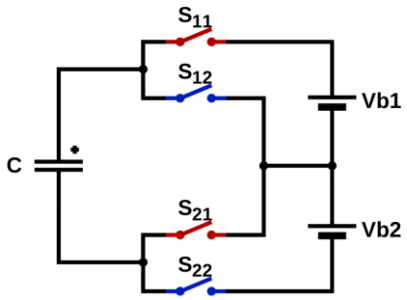


Fig.1: Switched capacitor equalizer for two cells.

Using the equivalent resistance value, it is possible to estimate the balancing time of the switched capacitor using the equivalent RC model proposed in [4]:

$$t_b = \tau_b ln(\frac{(V_{b1}(0) - V_{b2}(0))}{\Delta V_b}) \quad (4)$$

with $V_{b1}(0)$ and $V_{b2}(0)$ being initial voltage of each battery cells at the beginning of the equalizing process and ΔV_b being the target voltage difference between cells. The time constant τ_b is defined using the following expressions:

$$\tau_b = \frac{R_{eq} C_{eq,1} C_{eq,2}}{C_{eq,1} + C_{eq,2}} \quad (5)$$

The equivalent capacitance for both cell is calculated as:

$$C_{eq,i} = Q_{max} \frac{\Delta SOC_{bi}}{\Delta V_{bi}} \quad (6)$$

where ΔSOC_{bi} and ΔV_{bi} represent the SOC difference and open circuit voltage difference of each cell from the beginning to the end of the balancing process.

3. DESIGN PROCEDURES

To reduce balancing time, the equivalent resistance of the equalizer must be minimized. Since R is fixed, a design space based on switching frequency and balancing capacitance is constructed. Equation (2) is used to determine the capacitance range from the selected frequencies, voltage difference, and balancing current ranges, while equation (3) is used to evaluate the equivalent resistance over the resulting design space.

To choose the maximum switching frequency, the minimum equivalent resistance of the equalizer must be examined. According to [3], the minimum equivalent resistance for a switched capacitor equalizer expressed as:

$$R_{eq,min} = \lim_{f \to \infty} R_{eq} = \frac{2R}{D} \quad (7)$$

$$R_{ideal} = \frac{1}{fC} \quad (8)$$

From [2] and [3], the equivalent resistance of the switched-capacitor equalizer is governed by the product of the balancing capacitor value with the switching frequency and approaches its minimum value as the frequency rises. The highest and lowest switching frequency for the design space is decided based on gate driver limitation, typically between 1kHz and 100kHz.

According to [1], the 50%–100% SOC range corresponds to approximately 400 mV, giving about 8 mV per 1% SOC variation. A minimum SOC fluctuation of 5% therefore corresponds to a voltage fluctuation of about 40 mV, the minimum ΔV_c is chosen as 40mV. The maximum ΔV_c value is selected as 0.7 V based on the open circuit voltage

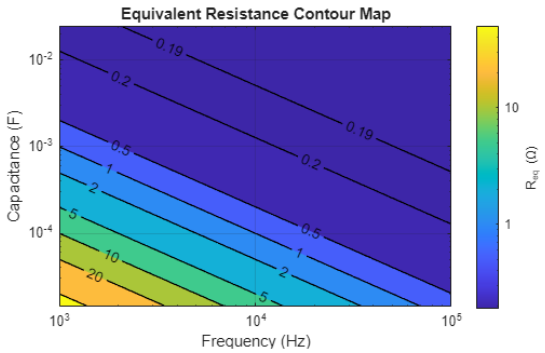


Fig.2: Contour graph of equivalent resistance value.

range of Li-ion cell according to [1]. The balancing current I is chosen as 0.5A minimum and 1A maximum. Applying the selected frequencies, voltage difference, and balancing current ranges results in a balancing-capacitance range from 0.025F to 14.2 µF.

The battery cell model used within the simulation has a maximum capacity of 94Ah, which is then scaled back to $94/10^5$ Ah to reduce computational time. Therefore, the Q_{max} value of each cell is 3.384 C.. Based on these factors, the equivalent capacitance C_{eq} for each cell is estimated to be 4.23F, assuming both cells are identical chemically. In this study, R is assumed equal to the battery internal resistance and is fixed at 0.0426Ω.

Fig. 2 shows the equivalent resistance distribution for the selected switching frequency and capacitance ranges. From this plot, the operating points corresponding to the maximum and minimum R_{eq} values can be identified. Based on Fig.2, the maximum and minimum R_{eq} value are approximately 70.4Ω and 0.189Ω, respectively.

4. SIMULATION RESULTS

To validate the proposed method, a two-cell switched-capacitor equalizer was simulated in PLECS using 3.68 V/94 Ah battery models. Each cell was modeled as a voltage source with series internal resistance and SOC-dependent voltage. To reduce computational time, the battery capacity was scaled to $94/10^5$ Ah. The initial SOC values were set to 70% and 50%, corresponding to an initial voltage difference of approximately 160 mV according to [1]. The target final voltage difference was set to 80 mV. Table 1 lists the switching frequency and balancing capacitance used in each simulation scenario.

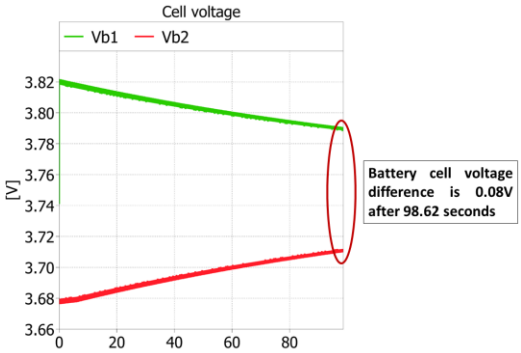
Using (4), the estimated balancing times are 0.2775 seconds for R_{eq}=0.189Ω and 103.24 seconds for R_{eq}=70.4Ω. Simulation results show good agreement, where the lower R_{eq} equalizer reaches the target condition in about 0.2765 seconds, while the higher R_{eq} equalizer requires 98.62 seconds to reach the targeted voltage difference between cells. Table 2 and Fig. 3 show that switched capacitor equalizer with the lowest R_{eq} reduces voltage difference between cells faster than that switched capacitor equalizer with the higher R_{eq}.

Table 1: Switching frequency and capacitor set up

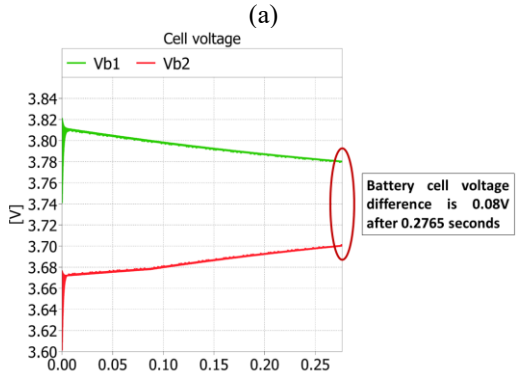
Simulation scenarios	Switching frequency	Capacitance	Equivalent resistance
Case 1	1kHz	14.2 µF	70.4Ω
Case 2	100kHz	0.025 F	0.189Ω

Table 2: Balancing time of equalizer at different R_{eq} value

Balancing time	Case 1	Case 2
Estimated (second)	103.24	0.2775
Simulation result (second)	98.62	0.2765



(a)



(b)

Fig.3. State-of-charge of the two cells when equalized by a switched capacitor with: (a)Case 1, (b)Case 2

5. CONCLUSION

This paper presents an equivalent resistance-based method for reducing balancing time in switched capacitor equalizers. The relationship between switching frequency, capacitance, and equivalent resistance was analyzed to evaluate balancing speed under different operating conditions. Results show that lower equivalent resistance increases balancing current and improves balancing speed. Simulation results were consistent with the theoretical analysis, demonstrating the effectiveness of the proposed approach for selecting suitable switching frequency and capacitance values.

ACKNOWLEDGEMENT

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1. Introduction

- Selecting the **switching frequency** and **capacitor value** of switched capacitor battery equalizers typically relies on:
  - **Repeated simulation or experimental tuning**
  - **Providing limited analytical insight into balancing performance**
- **Equivalent resistance representation** was developed to **relates circuit parameters directly to balancing performance**.
- A design space was created to analyze the effect of switching frequency and capacitance on balancing performance.
- The effects of switching frequency and capacitance on equivalent resistance are evaluated using a two cells simulation model.

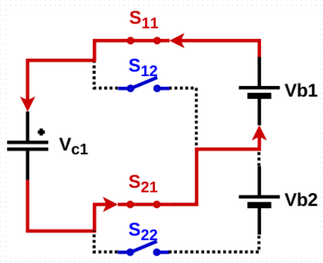
2. Theoretical Basis

- Between charging and discharging, the peak-to-peak voltage across capacitor is

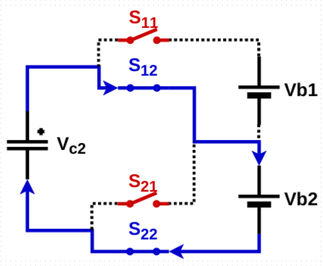
$$V_{c1} - V_{c2} = (V_{b1} - V_{b2})\frac{e^{\frac{D}{fRC}}-1}{e^{\frac{D}{fRC}}+1}$$

- The **average charge transfer current** describe the average current transfer from high voltage cell to low voltage cell.

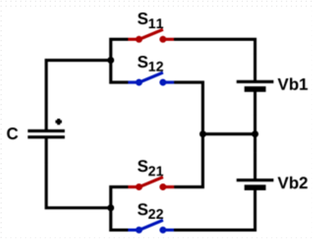
$$I = fC(V_{c1} - V_{c2}) = fC\Delta V_c$$



Charging mode of the equalizer.



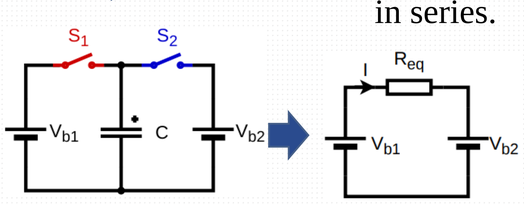
Discharging mode of the equalizer.



- Therefore, **switched capacitor equalizer** can be modeled as an equivalent resistance Req between the two battery cells [1].

$$R_{eq} = \frac{(V_{b1} - V_{b2})}{I} = \frac{1}{fC}\frac{1 + e^{-\frac{D}{fRC}}}{1 - e^{-\frac{D}{fRC}}}$$

- **The averaged model can be considered as an RC network**, with battery cells acting as capacitor connected in series.



Averaged model of the switched capacitor equalizer.

$$C_{eq,i} = Q_{max}\frac{\Delta SOC_{bi}}{\Delta V_{bi}} \qquad \tau_b = \frac{R_{eq}C_{eq,1}C_{eq,2}}{C_{eq,1} + C_{eq,2}}$$

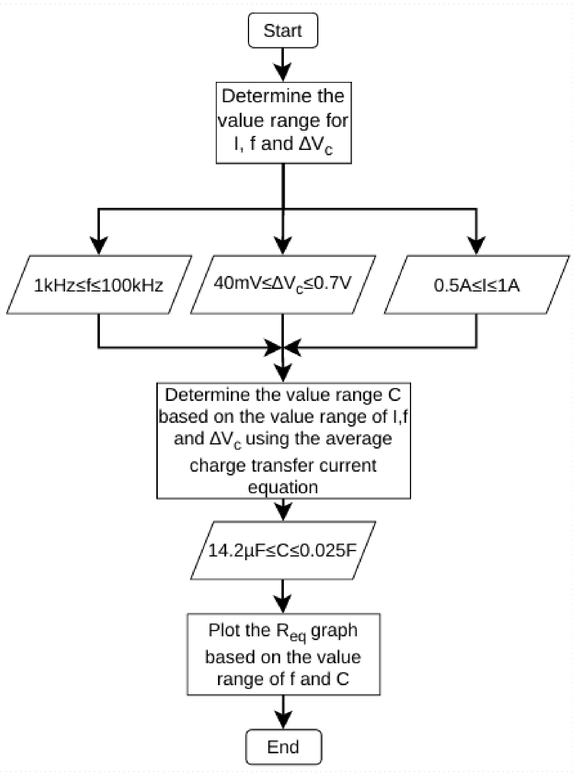
- The balancing time can be estimated based on [2]:

$$t_b = \tau_b ln(\frac{(V_{b1}(0) - V_{b2}(0))}{\Delta V_b})$$

3. Proposed Design Procedure

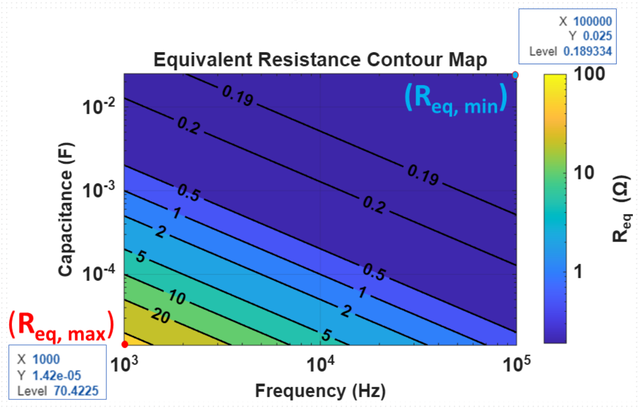
Value range for the design space

Switching frequency	Peak-to-peak capacitor voltage	Average charge transfer current
1kHz≤f_{sw}≤100kHz	40mV≤ΔV_c≤0.7V	0.5A≤I≤1A



Flow chart for the development of the equivalent resistance design space.

- **A design space** is created to **choose the switching frequency and capacitance to minimize equivalent resistance.**
- Using the range for f_{sw}, ΔV_c, I and the average charge transfer equation, the capacitance range can be calculated.



Contour graph of equivalent resistance value.

- According to the design space, **maximum R_{eq} is 70.4Ω**, while **minimum R_{eq} is 0.189Ω.**

4. Simulation Results

- A **two cells switched capacitor equalizer** was **simulated in PLECS** to validate the proposed method.
- **Initial voltage for the high voltage cell is 3.82V and 3.68V for low voltage cell.** The **target final voltage difference of 80 mV.**
- The cell model is **based on the Samsung 94Ah SDI** cell with its **internal resistance fixed and its capacity reduced** to **simplify analysis and speed up simulation.**

Parameters of the battery cell model

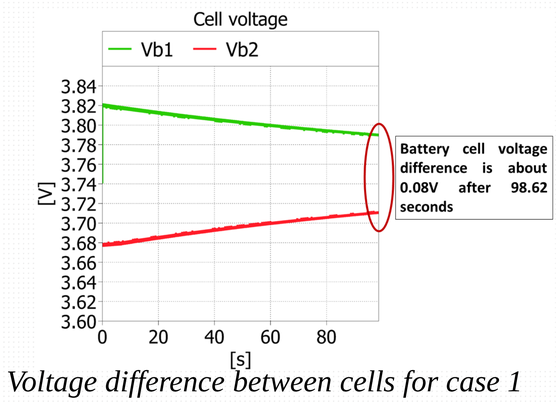
Maximum capacity (Q_{max})	Internal resistance	Equivalent capacitance (C_{eq})
94/10^5Ah	42.6mΩ	3.384C

Switching frequency and capacitor set up

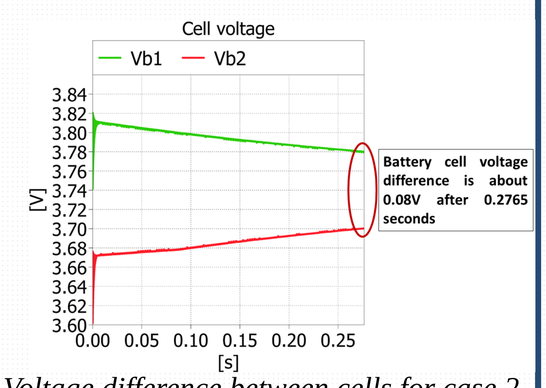
Simulation scenarios	f_{sw}	C	R_{eq}
Case 1	1kHz	14.2 μF	70.4Ω
Case 2	100kHz	250 mF	0.189Ω

Balancing time of equalizer at different R_{eq} value

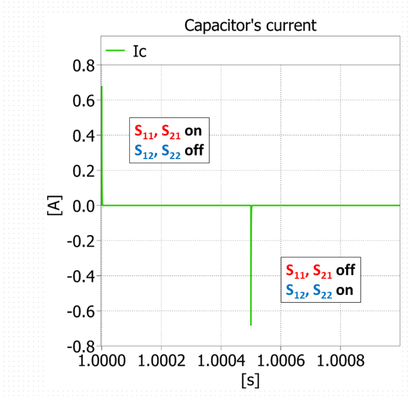
Balancing time	Case 1	Case 2
Estimated (second)	103.24	0.2775
Simulation result (second)	98.62	0.2765



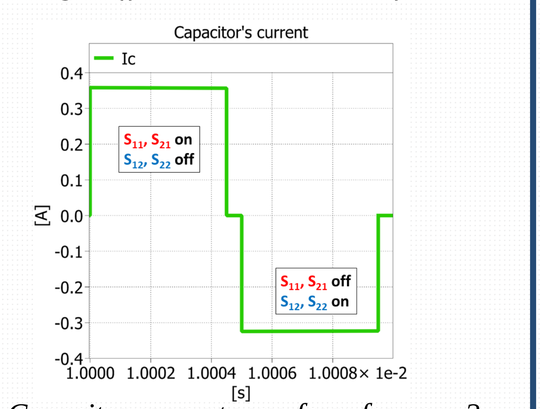
Voltage difference between cells for case 1



Voltage difference between cells for case 2



Capacitor current waveform for case 1



Capacitor current waveform for case 2

4. Conclusions

- The **averaged model of switched capacitor** and **balancing time estimation** can be applied to choose capacitance to **improve balancing speed** of the equalizer.
- **Design space** provides guidance for **selecting suitable design parameters.**
- **Lower equivalent resistance** is **shown** **to increase balancing current and reduce balancing time.**

5. References

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