Direct Cell-to-Cell Equalizer for Series Battery String Using Switch-Matrix Single-Capacitor Equalizer and Optimal Pairing Algorithm

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***Abstract*—In series battery strings, cell-inconsistency is caused by the state-of-charge (SOC) mismatch, non-identical battery impedance, or different self-discharging rates, and this leads to over-charge and over-discharge. Practically, switched-capacitor equalizers are the most promising means to eliminate the cell-inconsistency by virtue of automatic equalization, but the performance is heavily dependent on the initial cell voltage distribution and the number of series connections due to inefficient switch utilization. This paper proposes a direct cell-to-cell equalizer for a series-connected battery using a switch-matrix single-capacitor converter to further improve the switched-capacitor equalizer in term of performance consistency and coulomb efficiency. By adopting one extra current sensor and an optimal pairing algorithm, energy is transferred directly between the highest-SOC cell and the lowest-SOC cell to eliminate the impact of battery-impedance difference and false voltage measurement in BMIC caused by polarization effect. The experimental results verify the feasibility of the proposed scheme. Real-time tests are also implemented to fairly compare the proposed with the conventional methods. It is found that the performance of the proposed method is independent from initial voltage distribution in a series string, where the performance indices are consistent regardless of initial conditions. Besides, the energy loss of the proposed equalizer is further reduced and its overall efficiency is high in all test scenarios.**

***Index Terms*—Direct cell-to-cell equalizer, optimal pairing algorithm, switched-matrix single-capacitor (SMSC) equalizer, series-connected battery, SOC equalization.**

I. Introduction

IN efforts against climate change, the electrification of transportation has accelerated [1]. Accompanying the rapid growth of electric vehicle (EV) fleets, battery disposal for retired EVs will be a serious problem as the predicted number of retired batteries will reach $100-120GWh$ by 2030 according to IEA [2]. Although material recycling options have been taken into account [3], [4], the utilization of retired battery packs for energy storage systems (BESS) is also a promising solution [5], [6]. In fact, almost $70-80\%$ of the battery pack capacity of an EV still remains even after the retirement, so it can be re-utilized [7].

In an EV and BESS, batteries are connected in series to increase the voltage level. Although battery cells work under similar conditions, their performance can be dissimilar if there are the mismatches between the SOC levels, internal impedance, self-discharging rates, or available capacities. Such cell-inconsistency increases the risk of over-charging and over-discharging for battery strings as shown in Fig. 1 [8]. As a result, the battery cell could be deformed, catch fire, or explode. What's worse, the risks become more serious in second-life batteries (SLB) because the characteristics of the battery cells has further drifted after serving their first life in EV [9]–[12].

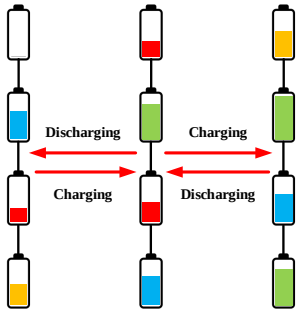

Fig. 1: Possible inconsistency in series-connected battery.

Therefore, an improved balancing scheme is essential in SLB system and various balancing techniques have been introduced as in [13]–[15]. In general, the battery voltages of the cells are monitored using a dedicated circuit, so-called battery monitoring integrated circuit (BMIC). The collected data are used to make a decision for cell balancing or to force the battery management system (BMS) to shut down [16], [17]. The cell balancing techniques are classified into passive and active methods according to their operating principle, as shown in Table I.

Passive balancing methods are popular in industrial applications due to their advantages of a low-cost, circuit simplicity, and ease of integration into BMIC. The main idea in passive balancing methods is to dissipate the excessive energy of higher SOC-level battery cells via shunt resistors [18], [19]. Due to their energy dissipation scheme, passive balancing methods reduce the available capacity of the battery system. Thus, passive methods are applied only in the charging process to ensure that the dissipated energy is compensated by the charger, and all cells are fully charged before they come back to work. Sometime, MOSFETs are utilized to dissipate extra energy of higher SOC-level battery cells or to regulate the

This paper is an extension of a conference paper, *A Single-Capacitor Equalizer Using Optimal Pairing Algorithm for Series-Connected Battery Cells*, in Proc. 2019 IEEE Energy Conversion Congress and Exposition (ECCE) which is listed in [37].

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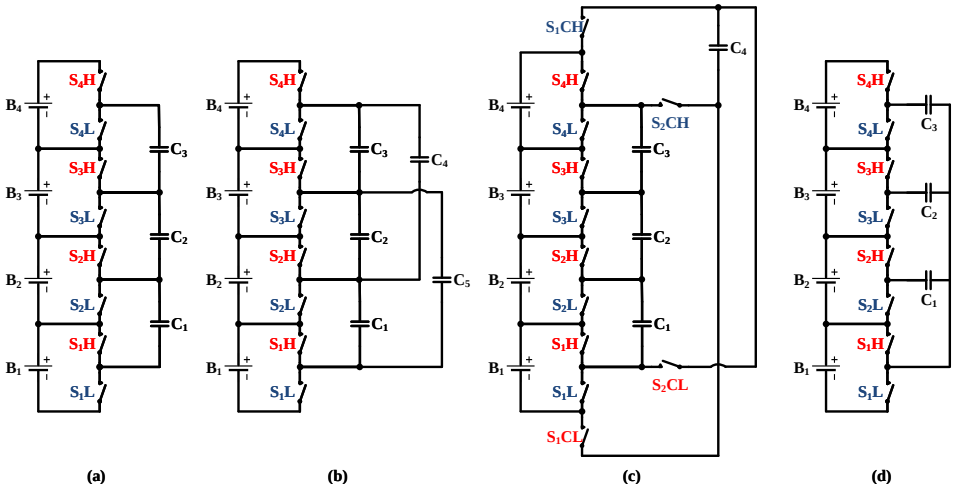


Fig. 2: Conventional SC equalizers - (a) classical structure, (b) double-tiered structure, (c) chain structure, and (d) star structure.

TABLE I: CLASSIFICATION OF CELL BALANCING TECHNIQUES

Ref.	Structure	Equalization Scheme	Target Objects	Control Technique
[18], [19]	Switched Resistor	Dissipative	Individual cell	Governed
[20]	Shunt MOSFET	Dissipative	Individual cell	Governed
[21]	Multiple Converters	Regenerative	Individual cell	Governed
[22]	Switch-matrix and Converter	Regenerative	Direct pack to cell	Governed
[23], [24], [25]	Multi-winding or Multiple Transformer	Regenerative	Any-cell to any-cell	Autonomous
[26], [27]	Switched Inductor	Regenerative	Adjacent cells	Autonomous
[28]	Switch-matrix and Inductor	Regenerative	Direct any-cell to any-cell	Governed
[29]	Switched Capacitor-Classical Structure	Regenerative	Adjacent cells	Autonomous
[30]	Switched Capacitor-Double-tiered Structure	Regenerative	Adjacent cells	Autonomous
[31]	Switched Capacitor-Chain Structure	Regenerative	Adjacent cells	Autonomous
[32]	Switched Capacitor-Star Structure	Regenerative	Any-cell to any-cell	Autonomous
[33]	Switched Capacitor-Reconfiguration	Regenerative	Adjacent cells	Autonomous
[34], [35], [36]	Switched Resonance Structure	Regenerative	Any-cell to any-cell	Autonomous
Proposed	**Switch-matrix Single-Capacitor Structure**	**Regenerative**	**Direct any-cell to any-cell**	**Governed**

charging current into the battery cells [20]. Because the energy dissipation scheme discharges the battery cells more frequently than is needed, the lifetime of the battery cells is reduced.

Meanwhile, active balancing techniques have been introduced for the purpose of adjacent cell-to-cell, direct cell-to-cell, pack-to-cell, or cell-to-pack equalization to improve the efficiency. They can be categorized by structures, equalization schemes, target objects, and control techniques as shown in Table I. Energy is transferred from the higher SOC-level cell to the lowest SOC-level cell by multiple DC-DC converters [21] or by a single converter with a switch-matrix [22]. Although the balancing current is well regulated and the efficiency is high due to the regenerative scheme, the high cost and bulky volume are shortcomings that reduce their practical applicability. To reduce the cost and size, multi-winding transformer-based or multiple transformer-based methods were introduced in [23]–[25]. However, the maximum available number of winding in a transformer limits the number of series-connections. By inheriting the advantages of multi-winding transformer-based and converter-based techniques, switched-inductor equalizers are used to balance the voltage of adjacent battery cells [26], [27], in which energy can be autonomously transferred between the adjacent cells. When it is combined with the switch-matrix structure [28], the highest SOC-level cell and the lowest SOC-level cell could be equalized directly such that it can be applied to any number of series-connections. However, the magnetic components in the balancing circuit still result in a high cost, heavy-weight, bulky volume, and relative low efficiency in seconds life battery application.

On the contrary, switched-capacitor techniques are the most promising methods due to their compact size, high efficiency, and low cost. Various structures of switched-capacitor (SC) equalizers have been published and are presented in Fig. 2. For a classical structure in Fig. 2(a) [29], each battery cell is connected to two serial switches, and one capacitor serves as the energy carrier. The upper switches and the lower switches are alternately turned on and off by the same complementary PWM signal pair. Since adjacent battery cells are connected to the capacitor one after the other, charge flows from the high

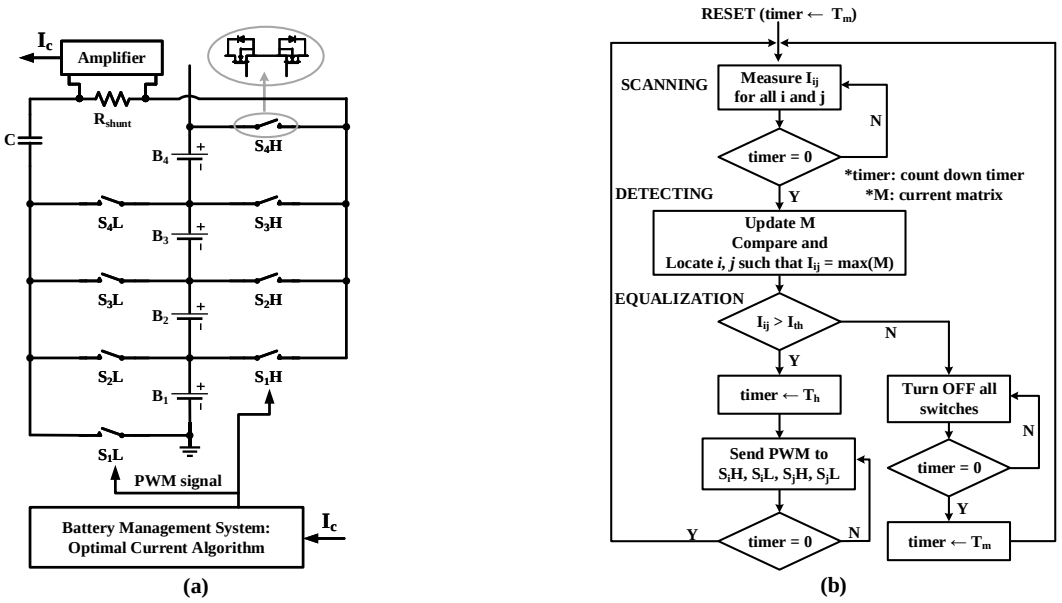


Fig. 3: Proposed equalizer - (a) topology structure, (b) control flowchart.

TABLE II:
COMPONENT COUNT COMPARISON

Topology	Total Switches	Activated Switches ◇	Capacitors	Current Sensors
Classical	$2N$	$2N$	$N-1$	–
Double -tiered	$2N$	$2N$	$2N-3$	–
Chain	$2N+4$	$2N+4$	N	–
Star	$2N$	$2N$	$N-1$	–
Proposed	$\boldsymbol{2N-Dual}$	**4**	**1**	**1**

◇: Number of the concurrent switch activation in one cycle.

*N: number of series connection.

*Dual: dual MOSFET package.

voltage cell to the low voltage one autonomously. However, since the energy is exchanged only between adjacent cells, the balancing speed becomes rather slow when the number of series-connection increases. To improve the balancing speed, other tiers of the capacitor are mounted to the classical structure as shown in Fig. 2(b) [30], helping the energy exchange between non-adjacent cells. Similarly, four additional switches and one capacitor can be additionally used to transfer energy between the battery cells at two ends of the series-string [31]. Technically, if the battery string forms a chain as in Fig. 2(c), the equalization speed increases by twice as much. On the other hand, one free poles of the capacitors are connected in the star structure as Fig. 2(d) and energy is directly transferred between any cells [32]. To increase the equalization current, a configuration of super-capacitor circuit is adopted in [33]. Although the equalization speed is increased, energy still flows between the adjacent cells, which makes the performance of the equalizer is inconsistent in various initial conditions. On the other hand, the switched-resonance circuits are applied to reduce the switching loss [34]–[36], but the extra components and EMC issue impose another problem.

In general, conventional switch-capacitor (SC) equalizers are an autonomous type, and thus, have three fundamental disadvantages. First, they have inefficient power switch utilization caused by continuous operation of free-running gate signals. The persistent charging-discharging operation even after the equalization results in additional power losses in the balancing circuit and inside the battery. Second, the extra voltage difference caused by battery polarization effect makes the balancing speed further slower. Third, the speed of conventional SC equalizers are strongly dependent on the initial cell voltage distributions in the string. Fourth, the conventional equalizers require multiple-channel voltage-sensors to monitor the battery voltages for the inconsistency-status detection and the switching pattern decision.

To mitigate these fundamental limitations, this paper proposes a direct cell-to-cell equalizer based on the switch-matrix single-capacitor. Instead of free-running operation, the switching decisions are governed by an optimal pairing algorithm in the equalization process. Since the basic concept was originally presented in [37], we have extended it by appending the operational analysis, optimal design consideration, and more experimental test results to verify the advantages of the proposed method over the conventional SC equalizers. The topology description and the principle of operation are presented in Section II. The design guide is provided with the theoretical analysis in Section III. The verification is given in Section IV, and the conclusions are drawn in Section V.

II. Proposed Equalizer

A. Topology structure

The proposed battery equalizer utilizes a switch-matrix single-capacitor (SMSC) structure as shown in Fig. 3(a), where a pair of back-to-back MOSFETs serves as one bi-directional

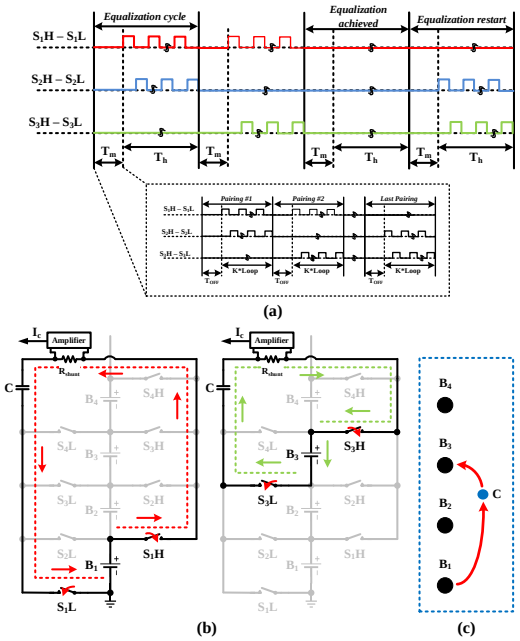


Fig. 4: Operating principle: (a) Timing diagram of the equalization process; (b) Operation principle of one cycle; (c) energy flow path (B: Battery, C: capacitor)

TABLE III:
BALANCING-CURRENT MATRIX

	B_1	B_2	B_3	...	B_N
B_1	X	$\|I_{12}\|$	$\|I_{13}\|$	...	$\|I_{1N}\|$
B_2	$\|I_{12}\|$	X	$\|I_{23}\|$	...	$\|I_{2N}\|$
B_3	$\|I_{13}\|$	$\|I_{23}\|$	X	...	$\|I_{3N}\|$
...	...	...	...	X	...
B_N	$\|I_{1N}\|$	$\|I_{2N}\|$	$\|I_{3N}\|$	...	X

***X: not available.**

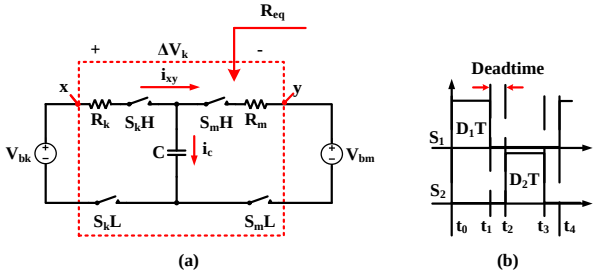


Fig. 5: Equivalent circuit of equalization principle.

switch to block the unexpected current flow in the reverse direction during the equalization process. The battery cells are alternately connected to the equalization capacitor, C, by two switches, S_iH and S_iL (i is the index of the cells). Besides, one current sensor is installed to observe the capacitor current, by which the optimal pairing algorithm decides the switching pattern. In the view of the component count, the proposed equalizer and the conventional methods utilize the same number of switches as shown in Table II; however, only one capacitor and one additional current sensor are used to transfer the energy between cells, which reduces the circuit volume. Furthermore, only four switches are activated at the same time during the equalization process, while all switches should be persistently switching in conventional methods. Thus, the energy loss during the equalization process is significantly reduced, which will be further analyzed in Section III.

B. Operating principle

The control flowchart of the proposed equalization process is illustrated in Fig. 3(b), and it consists of three stages: scanning, detection, and equalization. For visualization, a timing diagram is shown in Fig. 4(a). The equalization process starts with a current scanning interval, T_m, where the battery cells are sequentially connected to the capacitor for a short duration to measure the balancing current between each battery cell pairing, as shown in Fig. 4(b). To illustrate the operation, the pairing scenario could be similar to a football league where the home-cell #1 and the away-cell #2 are matched to get I_{12}; then, cell #1 and #3 give I_{13} and so on. After cell #1 is matched with all the other cells, cell #2 becomes the home-cell to get I_{23}, I_{24},...,I_{2N}. The process repeats to form a current-matrix shown in Table III during the scanning stage.

Due to the symmetry of the current-matrix, only the upper diagonal matrix is considered in the detection stage to locate the optimal home-away cells-pair that generates the highest balancing current. If the highest current is larger than a threshold value, I_{th}, the equalization stage starts. The PWM signals are sent to the corresponding switches of the optimal home-away pair for a hold duration, T_h, to directly deliver the energy from the highest SOC cell to the lowest SOC cell without passing any other switches and cells as Fig. 4(c). The direct charge transfer scheme helps to improve the equalization speed, but requires less energy loss than the conventional switched-capacitor equalizers. After T_h, another cycle repeats from the scanning stage. In fact, the optimal home-away pair is dynamically selected due to the change of cell energy levels during the equalization stage. When the highest current is smaller than I_{th}, all switches are stopped to reduce the energy loss, regarding that the equalization has been achieved as in Fig. 4(a).

After the equalization is achieved, the current scanning and detecting stages are periodically run in the background. When the highest current becomes larger than I_{th} again, which means the cells have inconsistency, the equalization process is executed to achieve another balancing status. Such an automatic process helps to reduce the energy loss of the equalization process and will not disturb the other functions of BMS.

III. Theoretical Analysis and Design Consideration

A. Theoretical analysis

During one equalization cycle, only two cells that have been regarded as the optimal pair exchange the energy with each other. Let their open circuit voltages be V_{bk} and V_{bm} to describe the operation. The equivalent circuit during one equalization cycle is illustrated in Fig. 5(a) where the switches

are controlled by a PWM signal pair with duty D_1 and D_2 as in Fig. 5(b). Assume $V_{bk} > V_{bm}$, an equalization cycle is divided into phase A ($t_0 \sim t_1$) when battery B_k is connected to the equalization capacitor, C, and phase B ($t_2 \sim t_3$) when the capacitor is connected to the other battery, B_m. Motivated by the research in [38], a theoretical analysis is made for the proposed method.

During phase A, switches S_kH and S_kL are turned on while the others are kept off. Let us denote that R_k is the total circuit resistances including the internal impedance of the battery, on-resistance of the MOSFETs, and ESR of the capacitor; τ_k is the time constant of the R_kC circuit. In addition, $i_k(t)$ is the current flowing from the battery B_k to the equalization capacitor, C; $v_c(t)$ is the capacitor voltage; and E_k is the energy loss of the circuit in phase A. Then, the following relationships are obtained.

$$R_k = R_{bk} + R_{d,on} + ESR, \tag{1}$$

$$\tau_k = R_kC, \tag{2}$$

$$i_k(t) = \frac{V_{bk} - v_c(t_0)}{R_k} e^{\frac{-t}{\tau_k}}, \tag{3}$$

$$\begin{aligned} E_k &= \int_{t_0}^{t_1} i_k^2(t) R_k dt \\ &= \int_{0}^{D_1T} i_k^2(t) R_k dt \\ &= \frac{1}{2} \left(V_{bk} - v_c(t_0)\right)^2 C \left(1 - e^{\frac{-2D_1T}{\tau_k}}\right). \end{aligned} \tag{4}$$

Furthermore, the stored charge in the capacitor throughout phase A and the capacitor voltage increment are expressed as

$$\begin{aligned} Q_{in} &= \int_{t_0}^{t_1} i_k(t) dt \\ &= \left(V_{bk} - v_c(t_0)\right) C \left(1 - e^{\frac{-D_1T}{\tau_k}}\right), \end{aligned} \tag{5}$$

$$\begin{aligned} v_c(t_1) - v_c(t_0) &= \frac{Q_{in}}{C} \\ &= \left(V_{bk} - v_c(t_0)\right) \left(1 - e^{\frac{-D_1T}{\tau_k}}\right), \end{aligned} \tag{6}$$

where D_1 is the duty cycle ratio and T is the switching period. From t_1 to t_2, all switches are turned off to prevent a short-circuit. Thus, the capacitor voltage is constant during this deadtime, and thus $v_c(t_1) = v_c(t_2)$.

Since the capacitor is connected to the battery cell B_m by switches S_mH and S_mL in phase B ($t_2 \sim t_3$), the current flows to battery cell B_m and the energy losses in the circuit are calculated by

$$i_m(t) = \frac{v_c(t_2) - V_{bm}}{R_m} e^{\frac{-t}{\tau_m}}, \tag{7}$$

$$\begin{aligned} E_m &= \int_{t_2}^{t_3} i_m^2(t) R_m dt \\ &= \int_{T/2}^{D_2T} i_m^2(t) R_m dt \\ &= \frac{1}{2} \left(v_c(t_2) - V_{bm}\right)^2 C \left(1 - e^{\frac{-2D_2T}{\tau_m}}\right) e^{\frac{-T}{\tau_m}}, \end{aligned} \tag{8}$$

$$R_m = R_{bm} + R_{d,on} + ESR, \tag{9}$$

$$\tau_m = R_mC, \tag{10}$$

where R_m and τ_m denote the total circuit resistance and the time constant. In addition, the out-going charge from the capacitor in phase B and the capacitor voltage decrement are expressed as

$$\begin{aligned} Q_{out} &= \int_{t_2}^{t_3} i_m(t) dt \\ &= \left(v_c(t_2) - V_{bm}\right) C \left(1 - e^{\frac{-D_2T}{\tau_m}}\right) e^{\frac{-T}{2\tau_m}}, \end{aligned} \tag{11}$$

$$\begin{aligned} v_c(t_2) - v_c(t_3) &= \frac{Q_{out}}{C} \\ &= \left(v_c(t_2) - V_{bm}\right) \left(1 - e^{\frac{-D_2T}{\tau_m}}\right) e^{\frac{-T}{2\tau_m}}. \end{aligned} \tag{12}$$

Because the proposed equalizer is operating in the quasi-steady state condition due to the slow-varying voltage of the battery, the in-coming charge can be regarded as equal to the out-going charge, $Q_{in} = Q_{out}$. As a result, the current of the capacitor is calculated by

$$\begin{aligned} I_c &= Q_{in} f_s = Q_{out} f_s \\ &= \left(V_{bk} - v_c(t_0)\right) C f_s \left(1 - e^{\frac{-D_1}{f_s\tau_k}}\right) \\ &= \left(v_c(t_2) - V_{bm}\right) C f_s \left(1 - e^{\frac{-2D_2}{f_s\tau_m}}\right) e^{\frac{-1}{2f_s\tau_m}}, \end{aligned} \tag{13}$$

where the switching frequency is $f_s = \frac{1}{T}$. Therefore, the voltage difference between the battery cells and the capacitor are derived as in the following equations.

$$\Delta V_k = V_{bk} - v_c(t_0) = \frac{I_c}{f_sC} \frac{1}{1 - e^{\frac{-D_1}{f_s\tau_k}}}, \tag{14}$$

$$\Delta V_m = v_c(t_2) - V_{bm} = \frac{I_c}{f_sC} \frac{e^{\frac{1}{2f_s\tau_m}}}{1 - e^{\frac{-2D_2}{f_s\tau_m}}}. \tag{15}$$

By (14) and (15), the energy losses in the circuit resistance, which are given in (4) and (8), become

$$E_k = \frac{I_c^2}{2f_s^2C} \frac{1 + e^{\frac{-D_1}{f_s\tau_k}}}{1 - e^{\frac{-D_1}{f_s\tau_k}}}, \tag{16}$$

$$E_m = \frac{I_c^2}{2f_s^2C} \frac{1 + e^{\frac{-D_2}{f_s\tau_m}}}{1 - e^{\frac{-D_2}{f_s\tau_m}}}. \tag{17}$$

Next, by multiplying the total energy losses of the circuit with the switching frequency, f_s, the power loss in the equalizer is derived as (18). Denoting the equivalent resistance of the switched-capacitor cell that has been seen from the $x - y$ terminal in Fig. 5(a) by R_{eq}, the power loss of the circuit can be expressed by

$$\begin{aligned} P_{loss} &= (E_k + E_m) f_s \\ &= \frac{I_c^2}{f_sC} \frac{e^{\frac{D_1}{f_s\tau_k}} e^{\frac{D_2}{f_s\tau_m}} - 1}{\left(e^{\frac{D_1}{f_s\tau_k}} - 1\right)\left(e^{\frac{D_2}{f_s\tau_m}} - 1\right)}, \end{aligned} \tag{18}$$

$$P_{loss} = I_c^2 R_{eq}. \tag{19}$$

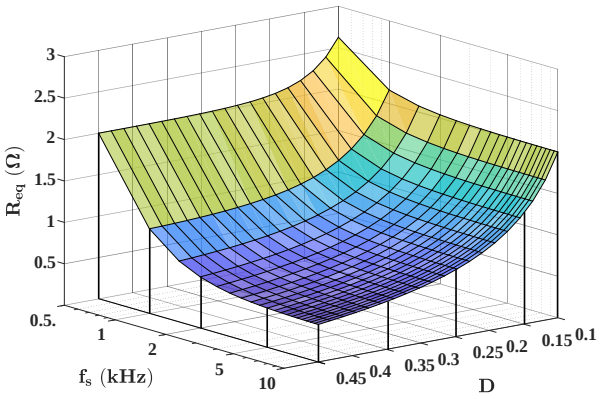


Fig. 6: Equivalent resistance of equalizer circuit, R_{eq}, by f_s and D ($C = 2200\mu$F, $\tau = 0.22$ ms).

Finally, by comparing (18) and (19), the equivalent resistance of the equalizer becomes

$$R_{eq} = \frac{1}{f_s C} \frac{e^{\frac{D_1}{f_s \tau_k}} e^{\frac{D_2}{f_s \tau_m}} - 1}{\left(e^{\frac{D_1}{f_s \tau_k}} - 1\right)\left(e^{\frac{D_2}{f_s \tau_m}} - 1\right)}, \tag{20}$$

which is a function of the duty ratio (D_1, D_2), the capacitance, C, and the switching frequency, f_s. To simplify (20), if the duty cycle ratio and the time constant are assumed that $D_1 = D_2 = D$ and $\tau_k = \tau_m = \tau$, the equivalent resistance is expressed as

$$R_{eq} = \frac{1}{f_s C} \frac{1 + e^{\frac{-D}{f_s \tau}}}{1 - e^{\frac{-D}{f_s \tau}}}. \tag{21}$$

B. Design consideration

To obtain the optimal equalization current and ensure a high equalization-speed for the proposed method, the design guidance needs to be established. Firstly, the duty cycle ratio of the switches is chosen to get a minimum equivalent resistance, R_{eq}. By substituting $\Delta V = 0.3$V, $C = 2200\mu$F, and $\tau = 0.22$ms into (21), the equivalent resistance of the equalizer is plotted in Fig. 6 as a function of f_s and D. It is found that the equivalent resistance is reduced when the duty cycle ratio, D, becomes as close to 0.5 as possible while the switching frequency is higher than 10kHz. After considering a small dead-time period to prevent short-circuit, the duty cycle ratio of equalization cycle is set to $D_1 = D_2 = 0.45$.

Secondly, to select the optimal switching frequency, f_s, and the equalization capacitance, C, some additional assumptions are made as follows: the maximum voltage difference between cells, ΔV, is 0.3V; the allowable switching frequency is in the range from 500Hz to 40kHz; the available equalization capacitance, C, is in the range from 470μF to 4700μF; and the duty cycle ratio is fixed to 0.45. Besides, the total circuit resistances are alternatingly set to 0.1Ω, 0.25Ω, and 0.5Ω, which includes the ESR of the capacitor, the on-resistance of the MOSFETs, and the wiring resistances. Under these assumptions, the equalization current, I_c, is calculated by (13) and is plotted in Fig. 7(a).

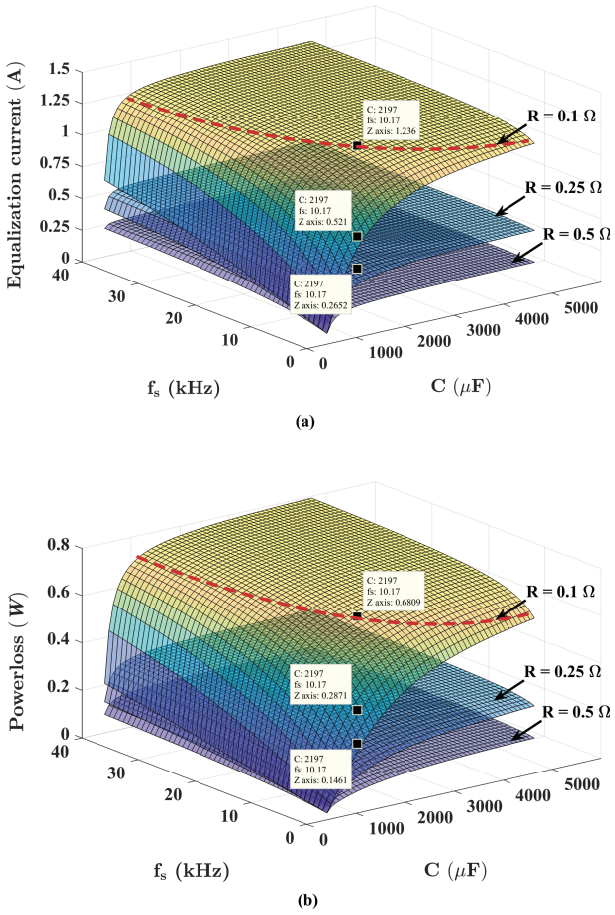


Fig. 7: Performance indices according to f_s and C: (a) average equalization current; (b) total power loss in the circuit (IRF8313, $\Delta V = 0.3$V).

Besides, the conduction loss in the equalization circuit is calculated by (19) while the switching loss of the MOSFETs is calculated by

$$P_{sw} = N_A \frac{1}{2} \Delta V I_c \left(t_r + t_f\right) f_s, \tag{22}$$

where N_A is the number of activated switches in one equalization cycle while the rising, t_r, and falling time, t_f, are provided in the datasheet of IRF8313 (dual MOSFET) [39]. Hence, the total loss of the circuit is expressed as

$$P_{total} = P_{loss} + P_{sw}, \tag{23}$$

and is also plotted in Fig. 7(b).

According to Fig. 7(a), the average equalization current increases when C and f_s are enlarged. Besides, the equalization current is heavily dependent on the total circuit resistance. The equalization current is reduced from 1.25A to 0.25A as the total circuit resistance changes. On the other hand, the conduction loss also increases when the equalization current increases. Thus, the losses are directly proportional to the equalization current. Furthermore, Fig. 7 reveals the satura-

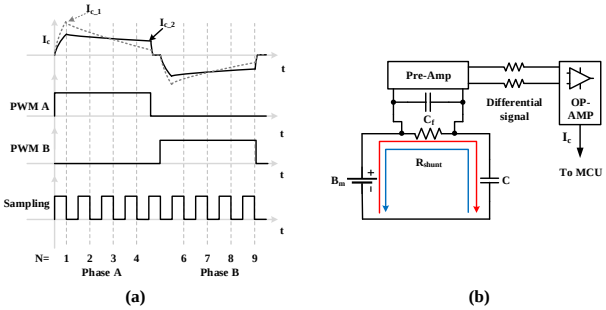


Fig. 8: Current measurement scheme in the proposed pairing algorithm: (a) sampling; (b) shunt resistor with pre-amplifier circuit.

tion of the equalization current (red dashed line) when the switching frequency is higher than 10kHz and the equalization capacitance is higher than 2200μF in all design cases of the total circuit resistance. Since the increment of the equalization current is trivial when C and f_s cross the saturation point, it is ineffective to increase the equalization current just by increasing C and f_s. Instead, the total circuit resistance should be minimized by choosing the low resistance switches, PCB artwork, and capacitor. Based on the above design guidance, the switching frequency is set to 10kHz and the equalization capacitance is set to 2200μF to achieve both the minimum power loss and a high equalization current.

To choose the suitable switches, the current and voltage stress of the switch-matrix are analyzed. When the balancing process is terminated, the voltage stress of the switch is calculated by

$$V_{sw} = V_{b\_max} - V_c = V_{b\_max} - V_{b\_min}. \tag{24}$$

where V_{b_max} and V_{b_min} are the initial highest and lowest voltage of the cells. Because of the low cell voltage (less than 5V), the voltage stress is trivial. Meanwhile, the current stress of the switches can be determined by (13). According to the stress calculation, IRF8313 dual MOSFET is utilized as a switch pair in this paper due to its low on-resistance for the circuit resistance reducing.

On the other hand, precise current measurement is critical in the optimal pairing algorithm. To get a high accuracy measurement, the sampling frequency has to be at least 8 times higher than the switching frequency like Fig. 8(a). Because the current waveforms of the battery pairs are different (I_{c_1} vs. I_{c_2}), the average equalization current of four sampling points $N = 1,\ 2,\ 3,\ 4$ is used to decide the optimal switching pattern. Due to the symmetry of the current waveform, the average current in phase B ($N = 6,\ 7,\ 8,\ 9$) is similar to that in phase A.

Among the various current measurement schemes in [40], [41], the measurement using a shunt resistor has high accuracy, high resolution, and simplicity as Fig. 8(b). For the implementation, two $50m\Omega$ resistors in parallel are used to convert the equalizing current information to a voltage signal. By an ACPL-C78A pre-amplifier circuit, the measured signal becomes a differential voltage which helps to protect MCU

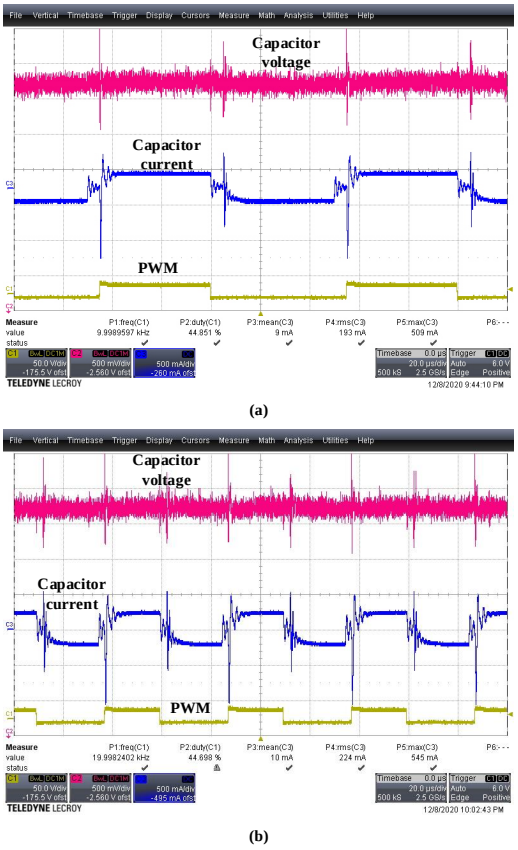


Fig. 9: Hardware waveform: (a) Design #1: 10kHz - 1000μF, (b) Design #4: 20kHz - 2200 μF.

with isolation. Next, the differential signal is amplified by an OP-AMP circuit. Finally, the output signal of the OP-AMP circuit is measured by the ADC of MCU.

In addition, the value of scanning time, T_m, and switching-pattern holding time, T_h, need a deeper analysis to address their impact on equalization performance and energy loss. In this paper, an approximate calculation is provided. According to the balancing current matrix in Table III, two cells are paired in to get a balancing current at a time. For N number of cells, there is ${}_NC^2$ combinations. To make sure that the previous combination scan will not affect the next one, the process is repeated in K operation loop of MCU for each pairing. Besides, between two scanning steps, all switches are turned off during T_{off}. Thus, the scanning time, T_m, is calculated by

$$T_m = [K\frac{1}{f_s} + T_{off}]\frac{N!}{2!(N-2)}. \tag{25}$$

On the other hand, a long switching-pattern holding time, T_h, can result an ineffectively equalization cycles when the voltage deviation of the cells is low. However, too short T_h can increase the total operation since the scanning process is regularly executed. In the experiments, T_h is fixed to 60 seconds.

IV. Verification Results

In section IV-A, hardware experiments are implemented with actual battery cells to verify the optimal design in Section

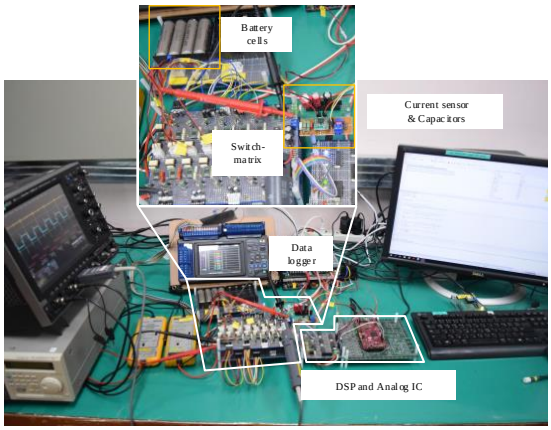


Fig. 10: Experimental hardware set-up for the proposed method.

TABLE IV:
EXPERIMENTAL RESULTS-BATTERY VOLTAGES (mV)

	#1	#2	#3	#4	ΔV
Initial #1	4000	3905	3896	3835	165
Exp. #1	**3905**	**3900**	**3895**	**3890**	**15**
Initial #2	3914	4017	3934	3864	153
Exp. #2	**3914**	**3912**	**3902**	**3896**	**18**
Initial #3	3898	3825	3760	3912	152
Exp. #3	**3823**	**3823**	**3814**	**3844**	**20**
HIL 4 cells	3826	3823	3820	3839	19

III-B. In Section IV-B, the performance is compared with the conventional methods. To exclude the effect of the battery cell impedance variation on the circuit evaluation and to make a fair comparison, hardware-in-the-loop (HIL) tests are implemented for the proposed and the conventional SC methods under three different test scenarios, where the mathematical model replaces the actual battery cells.

A. Hardware experimental results

To verify the design in Section III-B, the proposed equalizer is applied for two series battery cells that have a 320mV voltage difference ($V_1 = 4.163$V; $V_2 = 3.843$V). By changing the switching frequency and the equalization capacitance, the equalization currents are measured and compared with the theoretical calculation in four design cases: 10kHz / 1000μF (design #1), 10kHz/2200μF (design #2), 20kHz/1000μF (design #3), and 20kHz/2200μF (design #4). Besides, the measured total resistance of the circuit is 0.45Ω. The waveform of design #1 and #4 are shown in Fig. 9, and the measured equalization currents of the four designs are 193mA, 206mA, 212mA, and 224mA, respectively. Since the theoretical equalization currents in four designs are 191mA, 215mA, 213mA, and 226mA, the maximum error between the experimental results and the theoretical calculation is 4.65%. Thus, the theoretical analysis is proven to be sufficiently accurate for equalizer circuit design.

On the other hand, four design cases represent the influence of the switching frequency and the equalization capacitance to

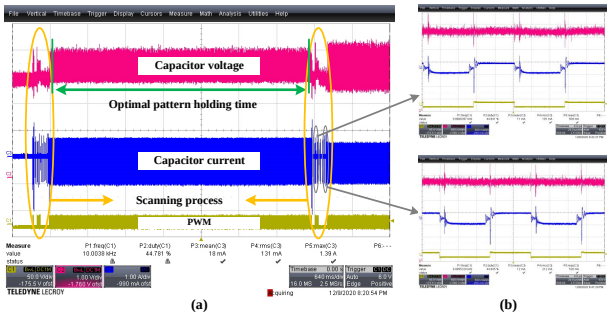


Fig. 11: Operation waveform: (a) one cycle in experiment #1; (b) two cell-pairings.

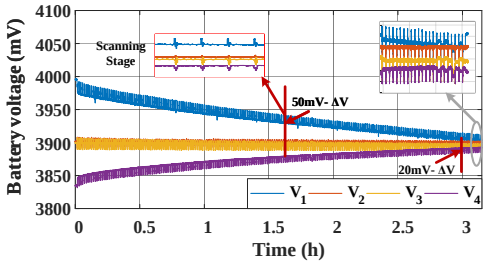
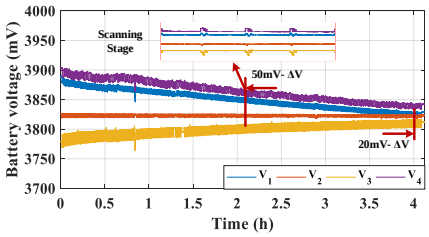


Fig. 12: Voltage profile of the equalization in experiment #1.

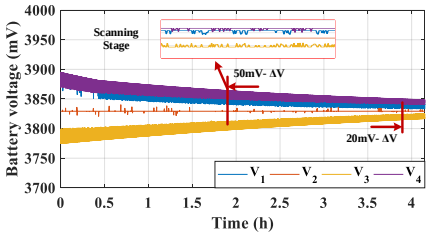
the equalization current, where the increments in the equalization currents are assessed. Although the switching frequency and the equalization capacitance in design #4 are twice those of design #1, the increments in the equalization current are trivial due to the high total resistance of the circuit. In other words, the switching frequency and the balancing capacitance that increases to enlarge the equalization current are ineffective from the view of equalization speed and power loss. Instead, the total resistance of the circuit should be designed to be as small as possible.

To further verify the performance of the proposed method, a hardware prototype is implemented for four series 18650 Li-ion cell string as in Fig. 10. The switching patterns are generated and controlled by a TMS320F28379D and analog ICs. For the data visualization, the voltage profiles of the equalization process are logged by the Hioki LR8402 and the recorded data are plotted by Matlab. Based on the optimal design, the equalization capacitance, C, and the switching frequency, f_s, are set to 2200μF and 10kHz, respectively. By setting the off time, T_{off} as 10ms and K as 200, the scanning period, T_m, and the switching-pattern holding-time, T_h, are 500ms and 60s, respectively.

The equalization performance of the proposed equalizer is assessed using various experiments, where the initial voltages of the battery cells are made to be randomly different from each other. After the voltage difference becomes lower than 20mV, the equalization process is stopped and the final voltages of the battery cells are summarized in Table IV. According to the results, the voltage differences are equalized within 15mV in exp. #1, 18mV in exp. #2, and 20mV in exp. #3, respectively. This means that the equalization performance of the proposed equalizer is independent from the initial cell



(a)



(b)

Fig. 13: Voltage profile comparison: (a) the experiment #3; (b) HIL test for 4 cells.

voltage distribution in the series string.

The waveform during one equalization cycle is shown in Fig. 11(a) to explain the operating principle of the proposed method. Based on the balancing current-matrix, the switches of the optimal home-away battery cells are activated during a hold time until another equalization cycle is repeated. Besides, the detailed waveform of two battery pairing shows the difference in the voltage and current of the capacitor as Fig. 11(b). On the other hand, the voltage profile of the battery cells in experiment #1 is plotted in Fig. 12. The proposed equalizer requires a 1.6h to achieve the 50mV voltage difference level and 3h to reach the 20mV voltage deviation.

B. Performance comparison based on the HIL tests

The proposed equalizer is implemented in the HIL test, where the setup follows experiment #3 in Section IV-A. The results of the HIL tests are also summarized in Table IV, including voltage, SOC, and current profiles. It is found that the performance of the HIL test and the experiment #3 are almost the same. The final voltage difference of the battery cells in experiment #3 and the HIL test are 20mV and 19mV, respectively. While experiment #3 requires $2.1h$ to achieve the 50mV voltage difference level, the proposed method in the HIL test takes $1.9h$. The voltage profiles of the experiment #3 and the HIL test are plotted in Fig. 13, and are similar. Evidently, the HIL test results can replace the hardware tests to confirm and compare the performance of the equalizers.

A battery string that consists of six 18650 Li-ion battery cells (3.6V-2600mAh) is implemented in the Typhoon HIL602+. In the tests, the proposed equalizer, the conventional chain [31], double-tiered (DT) [30], and star [32] equalizers are constructed. The initial SOC of the battery cells are distributed by the following three scenarios as Fig. 14:

- Scenario #1: SOCs of the cells are distributed from cell #1 to cell #6 descendingly.

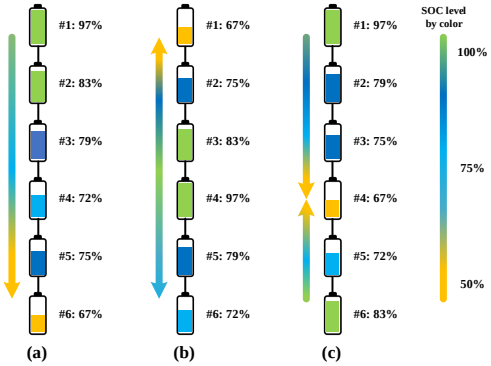


Fig. 14: Initial SOC-distribution of the cells in: (a) Scenario #1, (b) Scenario #2, (c) Scenario #3.

- Scenario #2: Two higher-SOC cells are in the middle of the string while the lowest-SOC cell is at the end of the string.
- Scenario #3: Two higher-SOC cells are in two opposite ends of the string while the lower-SOC cell is in the middle of the string.

These scenarios represent the three worst cases to assess the equalization performances of the cell balancing methods. For all the test scenarios, the equalization capacitance, C, and the switching frequency, f_s, are set to 2200μF and 10kHz to get an optimal equalization speed as discussed in Section III-B. The total circuit resistance is set to $25m\Omega$. For the proposed method, the scanning period, T_m and the switching-pattern holding-time, T_h, are set to 500ms and 60s, respectively. The equalization process is stopped after 4 hours and the performance indices are calculated and compared.

The equalization performance is evaluated by the degree of SOC equalization (DoSE) that is calculated by

$$DoSE = \frac{\Delta SOC_{initial} - \Delta SOC_{final}}{\Delta SOC_{initial}}, \tag{26}$$

and the degree of voltage equalization (DoVE) that is expressed as

$$DoVE = \frac{\Delta V_{initial} - \Delta V_{final}}{\Delta V_{initial}}, \tag{27}$$

where $\Delta SOC_{initial}$ and $\Delta V_{initial}$ are the initial SOC difference and the initial voltage difference between the highest and the lowest battery cells; and ΔSOC_{final} and ΔV_{final} are the differences after the balancing process. DoSE or DoVE represents the amount of SOC or voltage equalization that have been achieved at the end of the process.

Besides, the equalization speed of the equalizer is assessed by the slew rate of SOC after a ΔT time period ($SR_{SOC}(t)$: %/h) and slew rate of voltage ($SR_V(t)$: mV/h), which are calculated by

$$SR_{SOC}(t) = \frac{\Delta SOC(t+\Delta T) - \Delta SOC(t)}{\Delta T}, \tag{28}$$

and

$$SR_V(t) \quad = \frac{\Delta V(t+\Delta T) - \Delta V(t)}{\Delta T}. \tag{29}$$

where ΔT is the evaluation interval.

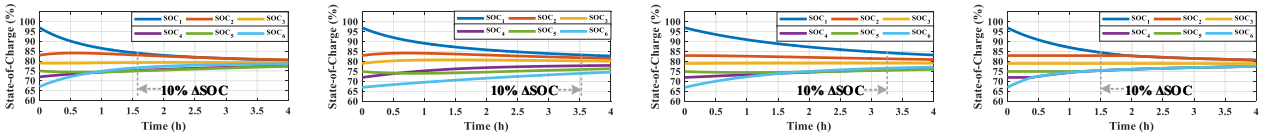


Fig. 15: HIL test results: SOC profiles in scenario #1- (a) Chain structure, (b) Double-tiered structure, (c) Star structure, (d) Proposed structure.

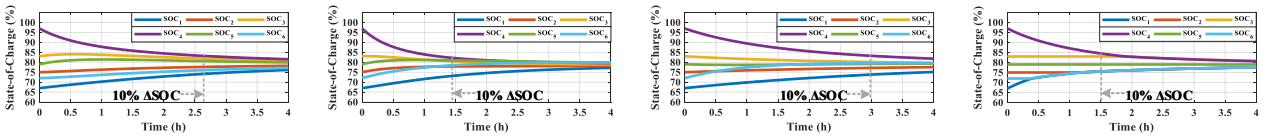


Fig. 16: HIL test results: SOC profiles in scenario #2- (a) Chain structure, (b) Double-tiered structure, (c) Star structure, (d) Proposed structure.

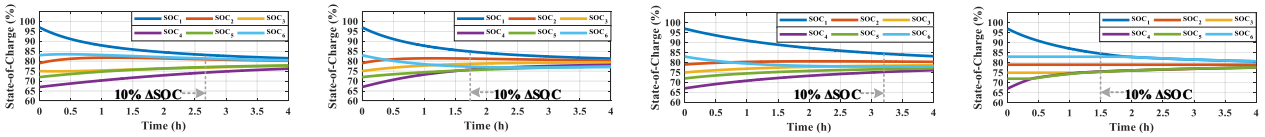


Fig. 17: HIL test results: SOC profiles in scenario #3- (a) Chain structure, (b) Double-tiered structure, (c) Star structure, (d) Proposed structure.

Furthermore, the energy loss is defined as the sum of the external loss in the balancing circuit and the internal loss during the equalization. The external loss, which includes the conduction loss and the switching loss, is calculated by (23). Besides, the internal loss inside the battery cells and the current sensing loss are calculated by

$$P_{int} = \sum_{k=1}^{N} I_k^2 R_b, \tag{30}$$

$$P_{shunt} = \sum_{k=1}^{N} I_k^2 R_{shunt}. \tag{31}$$

where N is the number of cells; R_b is the internal impedance of the battery cell provided by the datasheet ($70m\Omega$) [42]; R_{shunt} is the shunt resistor in the current sensing circuit; I_k is the RMS current that flows through the battery cell.

In addition, the gate charge loss also needs to be taken into the account due to a large number of used switches. Besides, the loss on the current sensing circuit should be analyzed for a process optimization. Thus, the gate charge loss and the sensing loss are calculated by

$$P_G = N_A[Q_G V_{gs} f_s + V_{cc} I_{cc}], \tag{32}$$

$$P_S = V_{dd} \frac{I_m T_m + I_h T_h}{T_m + T_h}, \tag{33}$$

where Q_G is the switch charge of MOSFET in datasheet [39]; V_{gs} is the gate drive voltage; N_A is the number of activated switches; V_{cc} is the power supply voltage for the gate driver; V_{dd} is the supply voltage of the current sensor and OP-AMP circuits; I_{cc} is the supply current of the gate driver; I_m is the supply current of sensing circuit during measuring period; I_h is the supply current of sensing circuit during the switching-pattern holding period. Thus, the total energy loss is calculated by

$$E_{total} = \sum_{t=0}^{t_{end}} [P_{int}(t) + P_{total}(t) + P_G(t) + P_{shunt}(t) + P_S(t)]T, \tag{34}$$

where t_{end} is the total operation time of the equalizer; T is the operating time of one equalization cycle.

In general, the effectiveness of equalizers is assessed by the Coulombic efficiency (CE). The physical meaning of CE is the ratio of total charge flows into the weak cells over the charge flow out of the high-SOC cell. Although CE already included the loss on equalizer circuit, the gate charge loss for the switches are unconsidered yet. Thus, the efficiency of the equalizer can be calculated by

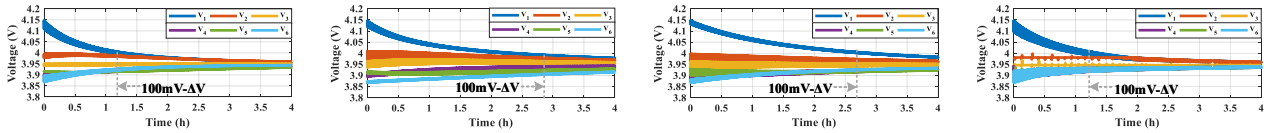
$$\eta = \frac{V_{avg} Q_{nom} \sum \Delta SOC_{Charge}}{V_{avg} Q_{nom} \sum \Delta SOC_{Discharge} + (P_G + P_s)T}, \tag{35}$$

where V_{avg} is the initial average voltage of the cells; Q_{nom} is the nominal capacity of the battery cell; $\sum \Delta SOC_{Discharge}$ is the total discharged energy from the high-voltage cells; $\sum \Delta SOC_{Charge}$ is the total charged energy to the low-voltage cells. Should the final SOC level of one cell is lower than the initial value, its SOC difference is taken into account of $\Delta SOC_{Discharge}$. In contrast, when the final SOC level of one cell is higher than the initial one, it is involved in ΔSOC_{Charge} calculation.

Because the conventional methods and the proposed equal-

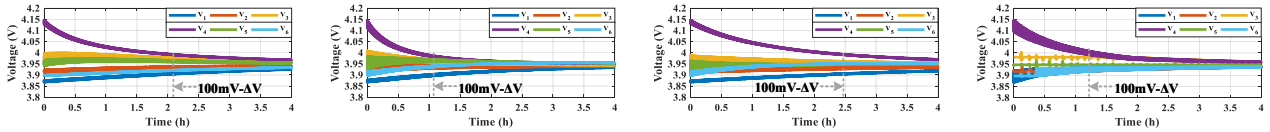
TABLE V: SUMMARY OF HIL TEST RESULTS

		State of Charge (%)							Voltage (mV)							Overall
		#1	#2	#3	#4	#5	#6	ΔSOC	#1	#2	#3	#4	#5	#6	ΔV	Eff. (%)
Scenario #1																
Initial		97.0	83.0	79.0	72.0	75.0	67.0	**30**	4146	3994	3947	3897	3917	3874	**272**	-
Final value	**Chain**	80.64	80.64	79.27	77.31	77.31	78.64	**3.33**	3959	3959	3950	3934	3934	3944	**25**	92.7
	DT	82.82	81.62	80.17	78.03	76.35	74.61	**8.21**	3979	3968	3956	3939	3917	3930	**62**	89.59
	Star	83.3	81.02	79.16	76.49	76.07	77.17	**7.23**	3984	3963	3948	3927	3923	3934	**61**	90.87
	Proposed	**80.73**	**80.73**	**79.00**	**77.55**	**77.55**	**77.55**	3.18	**3956**	**3956**	**3947**	**3937**	**3937**	**3937**	19	**94.76**
Scenario #2																
Initial		67.0	75.0	83.0	97.0	79.0	72.0	**30**	3874	3917	3994	4146	3947	3897	**272**	-
Final value	**Chain**	76.14	78.22	80.78	81.55	79.93	77.20	**5.41**	3926	3941	3961	3968	3934	3955	**42**	96.47
	DT	77.19	78.21	78.90	79.58	79.88	79.88	**2.69**	3925	3941	3946	3950	3954	3954	**21**	85.46
	Star	75.11	77.57	79.74	81.84	79.34	79.57	**6.73**	3918	3938	3953	3969	3951	3949	**51**	94.04
	Proposed	**77.60**	**77.67**	**80.67**	**80.67**	**79.00**	**77.60**	3.07	**3942**	**3944**	**3963**	**3963**	**3947**	**3942**	21	**92.57**
Scenario #3																
Initial		97.0	79.0	75.0	67.0	72.0	83.0	**30**	4146	3947	3917	3874	3897	3994	**272**	-
Final value	**Chain**	81.49	80.21	77.64	76.23	77.88	80.44	**5.26**	3966	3955	3937	3926	3959	3940	**40**	93.83
	DT	81.35	80.34	79.35	78.16	77.41	77.09	**4.26**	3965	3956	3950	3940	3932	3932	**34**	88.26
	Star	83.18	80.33	78.60	76.12	77.02	77.96	**7.06**	3980	3958	3943	3927	3938	3932	**53**	93.5
	Proposed	**80.71**	**79.00**	**77.62**	**77.62**	**77.62**	**77.62**	3.09	**3959**	**3947**	**3938**	**3938**	**3938**	**3958**	19	**94.41**



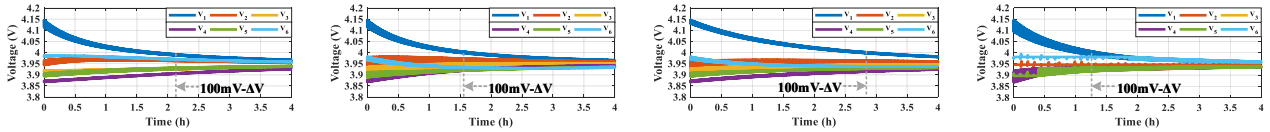
(a) (b) (c) (d)

Fig. 18: HIL test results: Voltage profiles in scenario #1 - (a) Chain structure, (b) Double-tiered structure, (c) Star structure, (d) Proposed structure.



(a) (b) (c) (d)

Fig. 19: HIL test results: Voltage profiles in scenario #2 - (a) Chain structure, (b) Double-tiered structure, (c) Star structure, (d) Proposed structure.



(a) (b) (c) (d)

Fig. 20: HIL test results: Voltage profiles in scenario #3 - (a) Chain structure, (b) Double-tiered structure, (c) Star structure, (d) Proposed structure.

izer are applied to the same battery configuration in the HIL and the circuit designs of all methods are individually optimized, the performance only reflects the topology structure and control schemes. The initial and the final test data are summarized in Table V. Distinctly, performances of conventional SC methods are strongly dependent on the initial voltage distribution of the cells. The conventional SC methods only achieve high performance in one specific test scenario among three. On the contrary, the performance of the proposed method shows a consistent performance across all scenarios.

The SOC and voltage profiles of the conventional SC methods and proposed equalizer are illustrated from Fig. 15 to Fig. 20, respectively. The proposed method can balance the SOC and voltage level of the cells within 3.2% and 21mV after 4 hours. Since the conventional SC methods are autonomous type, energy transfer between the cells is not so effective that it requires a lot of intermediate steps from the highest-voltage cell to the lowest-voltage cell as Fig. 21(a). On the contrary, the proposed method transfers energy from the highest-voltage cell to the lowest-voltage cell directly by adopting the optimal pairing algorithm as Fig. 21(b). Furthermore, the calculated efficiencies of the equalizers are summarized in Table V

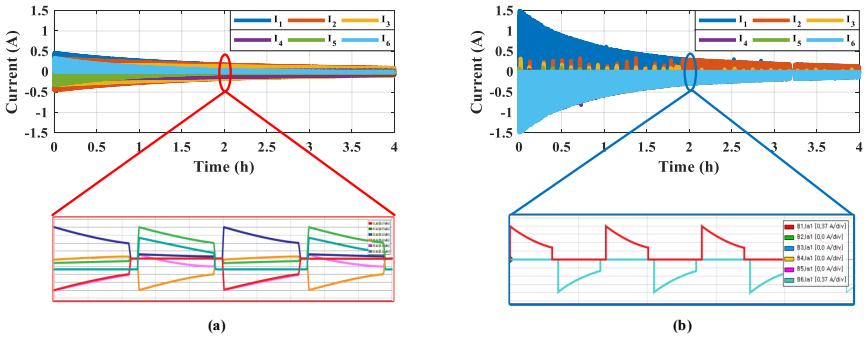


Fig. 21: HIL test results: Current profiles - (a) Star structure, (b) Proposed structure.

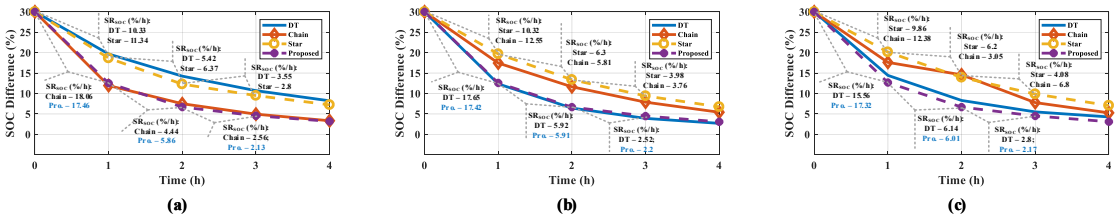


Fig. 22: HIL test results: SOC difference profiles: (a) scenario #1, (b) scenario #2, (c) scenario #3.

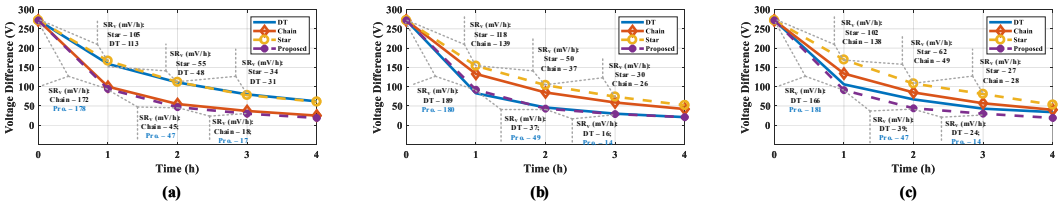


Fig. 23: HIL test results: Voltage difference profiles: (a) scenario #1, (b) scenario #2, (c) scenario #3.

show that the proposed method can maintain a high efficiency in all test scenarios ($> 93.76\%$). Besides, the SOC and voltage profiles of the proposed equalizer show a consistent performance in all test scenarios. Obviously, the influence of initial cell-voltage distribution on the performance of the proposed method is trivial, while it is considerable for the conventional methods.

To assess the equalization speed, the profiles of SOC-difference and voltage-difference are plotted in Fig. 22 and Fig. 23, respectively. Based on the test results, the slew rates of SOC and voltage differences are calculated for every 1 hour, which represents the amount of SOC and voltage difference changed. Generally, the switched-capacitor equalizer shows an exponentially decaying equalization current. Thus, slew rates are decreasing as time goes on. Since the most energy difference is equalized after the first 1 hour, the slew rates in the first 1 hour are assessed for the speed comparison. In terms of the equalization speed, only the proposed method can maintain a high slew rates in all test scenarios (over $17.3\%/h$ in SR_{SOC} and over $178mV/h$ in SR_V), while the slew rates of conventional methods are inconsistent due to the impact of voltage distribution in the battery string.

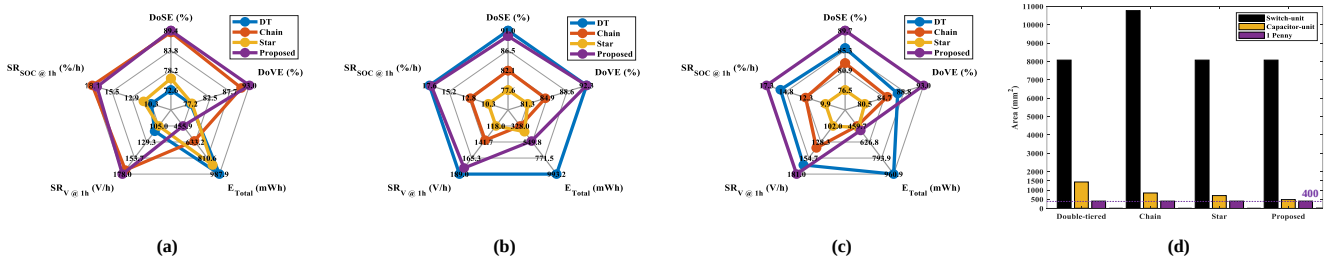
In summary, the $DoSE$, $DoVE$, SR_{SOC}, SR_V, and energy loss indices calculated by (26)∼(34), are illustrated in Fig. 24, and are summarized in Table VI. The spider charts and Table VI again confirm the consistent performance of the proposed equalizer in all test scenarios, where the indices are always high. (89.62% in DoSE, 92.77% in DoVE, $17.4\%/h$ in SR_{SOC}, and $179.67mV/h$ in SR_V, respectively.) In view of circuit size, the area of the switch-matrix, equalizing capacitor units, and auxiliary circuits of the equalizers are compared. Due to the series connection of the cells, the switches require floating ground drive circuits. Various gate drive techniques are reported in [43], where the pulse-transformer-based method and the gate drive IC with isolated power supply are popular. The conventional methods utilize single-MOSFET while the proposed method requires dual-MOSFET to implement a bi-directional voltage blocking. However, the conventional method requires one gate driver for each sing-MOSFET while the proposed method only requires one gate driver for each dual-MOSFET package. It is also noted that the dual-MOSFET is more size-effective than single-MOSFET solution. Thus, when considering the dimension of the MOSFET and the gate drive together, the switch-matrix part in the proposed equalizer occupies almost the same area as the conventional methods.

Furthermore, the dimension of the equalizing-capacitor unit in the equalizers can emphasize the advantage of the proposed equalizer over the conventional methods. In other to reduce

TABLE VI: SUMMARY OF PERFORMANCE INDICES

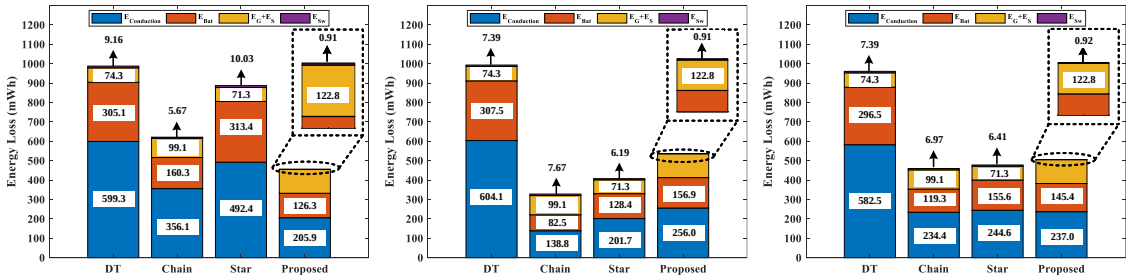
Topology	$DoSE[\%]$	$DoVE[\%]$	$SR_{SOC}[\%/h]$	$SR_V[mV/h]$	$Eff.[\%]$	*Charge transfer scheme*	*Additional sensing*	*Size*	*Initial voltage distribution dependency*
Double-tiered [30]	$72.6 \sim 91$	$77.2 \sim 93$	$10.3 \sim 17.6$	$105 \sim 189$	$85.46 \sim 89.59$	Free-wheeling	N-channel voltage sensors	L	Strong
Chain [31]	$80.9 \sim 89.2$	$84.7 \sim 92$	$12.3 \sim 18.1$	$128.3 \sim 176$	$92.7 \sim 96.47$	Free-wheeling	N-channel voltage sensors	L	Strong
Star [32]	$76.5 \sim 78.2$	$77.2 \sim 81.3$	$9.9 \sim 10.3$	$102 \sim 118$	$90.87 \sim 94.04$	Free-wheeling	N-channel voltage sensors	M	Strong
Proposed	$\mathbf{89 \sim 90.6}$	$\mathbf{92.3 \sim 93}$	$\mathbf{17.3 \sim 18.1}$	$\mathbf{154.7 \sim 178}$	$\mathbf{92.57 \sim 94.76}$	**Direct 1-to-1**	**One current sensor**	**S**	**Weak**

*N: number of series connection; L: Large; M: Medium; S: Small



(a) (b) (c) (d)

Fig. 24: Performance indices comparison: (a) Scenario #1; (b) Scenario #2; (c) Scenario #3; (d) Dimension comparison of the equalizers.



(a) (b) (c)

Fig. 25: Energy loss distribution of the equalizers in: (a) Scenario #1; (b) Scenario #2; (c) Scenario #3

the series resistance, three electrolytic capacitors of 820μF (ϕ5*12 mm) are connected in parallel to form a balancing capacitor unit. Depending on the circuit configuration, each equalizer requires the number of capacitor and switch units shown in Table II. The areas of the equalizers, including the switch and the equalizing capacitor with the current sensing circuit, are summarized in the spider chart as Fig. 24(d) for a clear comparison. Besides, the area of a US penny coin ($400mm^2$) is used as a reference.

Because the chain-structure requires 4 additional switch-units and one capacitor-unit to exchange energy from the first and the last cell in the string, the area of the chain-structure is significantly larger than the other methods. On the other hand, the area of the capacitor-unit in the double-tiered, chain, star, and proposed structures are $1441.5mm^2$, $842.8mm^2$, $700mm^2$, and $482.95mm^2$, respectively. Observed that the area of the capacitor-unit in the proposed equalizer is just slightly larger than one US penny coin even when the area of the current sensing circuit was included. Besides, the circuit area of conventional methods increases according to the number of series connections. Thus, the dimensions of the conventional methods are projected to be significantly larger. In contrast, the dimension of the capacitor unit in the proposed equalizer is unchanged since only one capacitor-unit is required even for an increased number of cells. Evidently, the proposed equalizer can significantly reduce the dimension of the capacitor-unit.

In addition, the loss distribution in Fig. 25 shows that the energy loss of the proposed method is only 46.15%, 55.36%, and 52.66%, respectively, of DT structure in all test scenarios. The loss distribution also shows some interesting results. Firstly, in view of the switching loss and the gate driver loss, the switching energy loss is trivial, but the gate charge loss is higher for the conventional methods. Observed that the gate charge loss can becomes significant when the number of cells increases. On the contrary, the proposed equalizer only utilizes four switches and one current sensor to directly transfer energy between two cells. The gate charge loss and the sensing loss of the proposed equalizer are $24.8mWh$ and $98.1mWh$, respectively. Although the gate charge and sensing losses of the proposed method is slightly higher than that in the conventional methods for the small number of series connection, it is almost constant and does not increase according to the number of cells. However, when the number of cells further increase,

the gate charge loss of the conventional methods is projected to be higher than that in the proposed method because it is dependent on the number of series connection. Thus, the proposed equalizer can reduce the loss dissipation. Secondly, it is observed that the conduction loss of the equalizer circuit and the internal losses of the battery cells take the most portion of the loss distribution. Thirdly, the chain and the star structure show a low energy loss only for scenario #2, but the proposed equalizer shows a relatively low energy loss for every test scenario that has been tested.

V. Conclusion

A direct cell-to-cell equalizer for a series battery string based on a switch-matrix single-capacitor converter has been presented to improve the performance of the switched-capacitor equalizer. The optimal pairing algorithm matches the highest-voltage and lowest-voltage battery pair to decide the switching pattern. Because energy is transferred directly from the highest-SOC cell to the lowest-SOC cell while just four switches are activated in one cycle, the performance of the proposed method is consistently high while the total energy loss has been significantly reduced. Design guidance has been provided to choose the optimal switching frequency, equalization capacitance, switches, and current sensor. Since the error between the theoretical calculation and the measured current is within 4.65%, the optimal design is verified. The HIL test results show the effectiveness of the proposed equalizer, where the energy loss is reduced down to $46.15\% \sim 55.36\%$ compared to the DT structure. Besides, the proposed method always shows a consistent equalization performance, Coulomb efficiency, and speed. Hence, it is expected to be useful especially for second-life battery systems that require an enhanced balancing method.

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