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Parameter identifcation for dual‑phase shift modulated DAB converters

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Abstract

Deadbeat control is an efective method for controlling the output voltage of dual active bridge converters. However, its efectiveness depends on the model parameter accuracy. In practice, the model parameters of dual active bridge converters vary depending on the operation conditions, manufacturing tolerances, and calendar aging. This leads to performance degradation and causes steady-state errors of the output voltage. To overcome the efect of parameter mismatch, this study proposed an algorithm to achieve the online identifcation of two model parameters, i.e., the series inductor and the output capacitor. Based on a least-squares analysis, the online parameter identifcation of a dual active bridge converter under dualphase shift modulation is implemented to obtain the actual values of model parameters. Consequently, the steady-state errors of the output voltage are immediately mitigated after every sampling period when the optimal predicted phase shift duty ratios are updated. The proposed algorithm was tested through both simulations and experiments to verify its efectiveness.

Keywords Dual active bridge · Deadbeat control · Dual-phase shift · Mismatch · Parameter identifcation

1 Introduction

Over the last few decades, the dual active bridge (DAB) converter has been a focus of studies due to its advantages such as galvanic isolation, ultrafast response, and high efficiency. In general, phase shift modulations are attractive techniques for DAB modulations. One of the simplest modulation techniques is single phase shift (SPS). However, it has low efficiency and high current stress. To overcome these issues, various modulation techniques such as extended phase shift (EPS), dual-phase shift (DPS), and triple-phase shift (TPS) have been proposed. For EPS, the operating states of the two bridges are not the same when the power flow direction is changed. Based on its implementation, TPS modulation is the most difficult method. Therefore, DPS is a relatively optimal modulation method in terms of ease of implementation and efficiency $[1, 2]$ $[1, 2]$ $[1, 2]$ $[1, 2]$.

To minimize current stress and increase efficiency, $[3-5]$ $[3-5]$ used a proportional-integral (PI) controller in combination with minimum current stress constraints to regulate the phase shift duty ratios with DPS modulation. However, in their studies, they did not give guidelines for determining the PI gains. Hence, the heuristic design is insufficient to determine the optimal predicted phase shift duty ratios. Consequently, the current stress cannot be minimized. Moreover, with fxed PI gains, the control performance degrades under parameter mismatch during operation. In [[6\]](#page-10-4), the authors verifed that the transient dynamic performance of a controller is afected with only a 10% parameter mismatch.

According to the authors of [[7](#page-10-5), [8\]](#page-10-6), deadbeat control emerged as one of the best methods among the various control methods used to control the output voltage of DAB converters. These studies performed EPS and SPS modulation with deadbeat current control. However, they required midpoint current sampling, which resulted in difficulty in terms of implementation. Additionally, in these studies, variations in the value of the series inductor led to performance degradation.

For the DAB converter shown in Fig. [1](#page-1-0), the series inductor *L* and the output capacitor C_2 have a great influence under any of the model-based control methods if the power is transferred from the left side to the right side. In practice, the inductance and capacitance can vary according to manufacturing tolerances, temperature drift, aging, vibrations, and stress, which results in mismatches of around 20% when the actual model

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Fig. 1 DAB converter topology

parameters difer from the original model parameters [[9–](#page-10-7)[12](#page-10-8)]. Therefore, to control the output voltage of the DAB converters, online parameter identifcation is needed to improve the regulator performance. When mismatches of L and C_2 occur, the output voltage of the DAB converters haves a steady-state error since the predicted value of the output voltage is diferent from the calculated value.

To identify parameters online, improve transient and steady-state performances, minimize current stress, and achieve easy implementation, this study proposed deadbeat control under DPS modulation. The least-squares analysis (LSA) method [[13](#page-10-9), [14](#page-11-0)] is used for the online parameter identification of L and C_2 . Under DPS modulation, deadbeat control is performed to make the output voltage tracks its reference value. Moreover, the current and voltage are sampled at the same time, and the switching frequency and sensor sampling frequency are the same. Thus, the proposed algorithm is easy to implement. In addition, the Lagrange multiplier method (LMM) [[14](#page-11-0)] is used to minimize current stress. When compared with deadbeat control under DPS modulation without online parameter identifcation, the proposed algorithm can provide actual parameter values and reduce the steady-state error of the output voltage after every sampling period.

The remainder of this paper is organized as follows. Deadbeat control under DPS modulation is briefy reviewed in Sect. [2.](#page-1-1) In Sect. 3, the effects of parameter mismatch are shown. The proposed algorithm is presented in Sect. [4](#page-4-0). Simulation and experimental results are presented in Sect. [5](#page-8-0) to verify the efectiveness of the proposed algorithm. Finally, Sect. [6](#page-10-10) provides some conclusions.

2 Deadbeat control under DPS modulation

2.1 Predicted phase shift duty ratios derivation

Figure [2](#page-1-2) represents waveforms of the DAB converter under DPS modulation. The series inductor current i_L and the

Fig. 2 Waveforms of a DAB converter under DPS modulation: **a** $0 ≤ D_1 ≤ D_2 ≤ 1$; **b** $0 ≤ D_2 < D_1 ≤ 1$

average transferred power *P* under DPS modulation in the case of $0 \le D_1 \le D_2 \le 1$ are derived as [\[15](#page-11-1)]:

$$
v_p(t) - v_s(t) = Ldi_L(t)/dt
$$
\n(1)

$$
P = \frac{1}{T_h} \int_{0}^{T_h} v_p(t) i_L(t) dt.
$$
 (2)

From Eqs. [\(1](#page-1-3)), and ([2](#page-1-4)), and Fig. [2a](#page-1-2), *P* is derived as:

$$
P = nv_1v_2\big(D_2\big(1-D_2\big)-0.5D_1^2\big)/(2fL)
$$
\n(3)

where D_1 is the inner phase shift duty ratio, D_2 is the outer phase shift duty ratio, *f* is the switching frequency, and *n* is the transformer turn ratio.

Similarly, in the case of $0 \le D_2 < D_1 \le 1$:

$$
P = nv_1v_2(1 - D_1 - 0.5D_2)D_2/(2fL).
$$
 (4)

In the case of $0 \le D_1 \le D_2 \le 1$, the secondary current *i_s* is derived as:

$$
i_s = P/v_2 = nv_1(D_2(1 - D_2) - 0.5D_1^2)/(2fL).
$$
 (5)

In addition, the dynamic equation of v_2 is shown as:

$$
C_2 dv_2/dt = i_s - i_2. \tag{6}
$$

Utilizing the forward approximation, Eq. [\(6](#page-2-0)) is discretized as:

$$
v_2[k] = (i_s[k-1] - i_2[k-1])/(fC_2) + v_2[k-1]
$$
 (7)

where $v_2[k]$ is the output voltage at the k^{th} sampling period; $v_2[k-1], i_2[k-1],$ and $i_s[k-1]$ are the output voltage, output current, and secondary current at the $(k - 1)$ th sampling period, respectively.

Combining Eqs. (5) (5) and (7) (7) , the output voltage is derived as:

where:

$$
a_2 = fC_2(v_{2ref} - v_2[k]) + i_2[k].
$$
\n(14)

There are infinite combinations of D_1 and D_2 that make Eq. (8) or Eq. (12) (12) achieve the goal in Eq. (9) (9) (9) . Due to the dependency between D_1 and D_2 , if D_1 is chosen, D_2 is automatically determined. Thus, in the deadbeat control, the determination of the optimal values of D_1 and D_2 become extremely important.

2.2 Current stress optimization of phase shift duty ratios using LMM

In this section, the optimal value of D_1 is derived. The maxi-

$$
v_2[k] = \frac{nv_1[k-1]}{2f^2LC_2} (D_2[k-1](1 - D_2[k-1]) - 0.5D_1^2[k-1]) - i_2[k-1]/(fC_2) + v_2[k-1]
$$
\n(8)

where $v_1[k-1], D_1[k-1]$, and $D_2[k-1]$ are the input voltage, inner phase shift duty ratio, and outer phase shift duty ratio at the $(k - 1)$ th sampling period, respectively.

Meanwhile, the goal to be achieved is:

$$
v_2[k] = v_{2ref} \tag{9}
$$

where v_{2ref} is the reference value of the output voltage v_2 .

From Eq. (8) (8) and Eq. (9) (9) , the predicted outer phase shift duty ratio in the k^{th} sampling period is obtained as:

$$
D_2[k] = 0.5 - (0.25 - 0.5D_1^2[k] - 2f^2LC_2a_1/(nv_1[k]))^{1/2}
$$
\n(10)

where:

$$
a_1 = v_{2ref} - v_2[k] + i_2[k]/(fC_2).
$$
 (11)

In Eqs. ([10\)](#page-2-5) and [\(11](#page-2-6)), $D_1[k], D_2[k], v_1[k]$, and $i_2[k]$ are the predicted inner phase shift duty ratio, predicted outer phase shift duty ratio, input voltage, and output current in the k^{th} sampling period, respectively.

Similarly, the output voltage in case of $0 \le D_2 < D_1 \le 1$ is obtained as:

mum transferred power P_m and the maximum transferred current i_m are defined as:

$$
P_m = nv_1v_2/(8fL)
$$
 (15)

$$
i_m = P_m/v_1 = nv_2/(8fL). \tag{16}
$$

From Eqs. (3) (3) (3) , (4) (4) (4) , and (15) (15) (15) , the unified transferred power p_u is defined as Eq. ([17](#page-2-9)) and Eq. ([18\)](#page-2-10) in cases of $0 \leq D_1 \leq D_2 \leq 1$ and $0 \leq D_2 < D_1 \leq 1$, respectively [\[3](#page-10-2)[–5](#page-10-3)].

$$
p_u = P/P_m = 4D_2(1 - D_2) - 2D_1^2 \tag{17}
$$

$$
p_u = P/P_m = 4D_2(1 - D_1) - 2D_2^2.
$$
 (18)

As shown in Fig. [2](#page-1-2)a, the current stress i_{ss} has its maximum value in the case of $0 \le D_1 \le D_2 \le 1$ at point G1, which is obtained as:

$$
i_{ss} = \max \left\{ i_L \right\}_{T_h} = n v_2 \big(M \big(1 - D_1 \big) + \big(D_1 + 2D_2 - 1 \big) \big) / (4fL) \tag{19}
$$

where $M = v_1/(nv_2)$ is the voltage conversion ratio.

$$
v_2[k] = \frac{nv_1[k-1]}{2f^2LC_2}D_2[k-1](1 - D_1[k-1] - 0.5D_2[k-1]) - i_2[k-1]/(fC_2) + v_2[k-1].
$$
\n(12)

By substituting Eq. (9) (9) (9) into Eq. (12) (12) , the predicted outer phase shift duty ratio in the k^{th} sampling period is derived as:

$$
D_2[k] = 1 - D_1[k] - \left(\left(1 - D_1[k] \right)^2 - 4fLa_2 / \left(nv_1[k-1] \right) \right)^{1/2}
$$
\n(13)

The unified transferred current i_u is calculated as:

$$
i_u = i_{ss}/i_m = 2(M(1 - D_1) + (D_1 + 2D_2 - 1)).
$$
 (20)

To find the optimal value of D_1 , LMM is used to ensure that i_u is minimized while p_u traces the reference p_{uref} . Thus, the Lagrange function F is outlined as follows:

Fig. 3 Percentage of output voltage steady-state error Δv_2 %

$$
F(\mathbf{d}, \psi) = i_u(\mathbf{d}) + \psi \left[p_u(\mathbf{d}) - p_{uref} \right]
$$
 (21)

where $\mathbf{d} = [D_1, D_2]^T$ is the vector of the phase shift duty ratios, ψ is the Lagrange multiplier, and the superscript symbol *T* indicates the matrix transpose.

Differentiating the Lagrange function $F(d,\psi)$ yields:

$$
\frac{\partial F(\mathbf{d}, \psi)}{\partial D_1} = 0; \ \frac{\partial F(\mathbf{d}, \psi)}{\partial D_2} = 0; \ \frac{\partial F(\mathbf{d}, \psi)}{\partial \psi} = 0.
$$
 (22)

Substituting Eqs. ([17](#page-2-9)), [\(18\)](#page-2-10), [\(20](#page-2-11)), and [\(21](#page-3-0)) into Eq. [\(22\)](#page-3-1), the optimal value of D_1 is derived in discretized form as Eq. [\(23\)](#page-3-2) and Eq. ([24\)](#page-3-3) when $\frac{(M[k-1]+1)^2-4}{2M^2[k-1]} < p_u[k-1] \le 1$ and $0 \le p_u[k-1] \le \frac{(M[k-1]+1)^2 - 4}{2M^2[k-1]}$, respectively.

$$
D_{1opt}[k] = \left(\frac{(1 - p_u[k-1])(M[k-1]-1)^2}{2(M^2[k-1]-2M[k-1]+3)}\right)^{1/2}
$$
 (23)

$$
D_{1opt}[k] = 1 - \left(\frac{p_u[k-1](M[k-1]+1)^2}{2(M^2[k-1]+2M[k-1]-3)}\right)^{1/2}
$$
 (24)

where $M[k-1]$ and $p_u[k-1]$ are calculated as follows:

$$
M[k-1] = v_1[k-1]/(nv_2[k-1])
$$
\n(25)

$$
p_u[k-1] = 8fLi_2[k-1]/(nv_1[k-1]).
$$
 (26)

Table 1 Simulation parameters

| Parameter | Symbol | Values |
|---------------------------------------|------------|-------------|
| Input voltage | v_{1} | 100V |
| Reference value of the output voltage | v_{2ref} | 95 V |
| Switching frequency | | 10 kHz |
| Transformer turn ratios | n | |
| Series inductor | L | $60 \mu H$ |
| Output capacitor | C_{2} | $220 \mu F$ |
| Load | R | 25Ω |

 $D_2[k]$ in Eqs. ([10\)](#page-2-5) and ([13\)](#page-2-12) becomes the optimal value $D_{2opt}[k]$ when $D_{1opt}[k]$ is utilized. Thus, it makes v_2 track v_{2ref} and minimizes the current stress. It should be noted that, in this scheme, the predicted phase shift duty ratios only depend on the values of $M[k-1]$ and $p_u[k-1]$.

3 Parameter mismatch efects

To refect the infuence of parameter mismatch on the output voltage in the case of $0 \le D_1 \le D_2 \le 1$, m_L and m_{C2} are defined as the mismatch ratios of the series inductor and output capacitor, respectively.

$$
m_L = L/L_a; \ m_{C2} = C_2/C_{2a} \tag{27}
$$

where *L* and C_2 are the model values; and L_a and C_{2a} are the actual values of the series inductor and output capacitor, respectively.

Assuming that the average capacitor current is equal to zero in the steady-state and substituting $i_2=i_3=v_2/R$ into Eq. [\(5\)](#page-2-1), the output voltage v_2 is obtained and discretized as:

$$
v_2[k] = \frac{Rnv_1[k]}{2fL_a} \Big(D_{2\text{opt}}[k] \big(1 - D_{2\text{opt}}[k] \big) - 0.5D_{1\text{opt}}^2[k] \Big) \tag{28}
$$

where the optimal values of $D_{1opt}[k]$ and $D_{2opt}[k]$ are obtained from Eqs. ([23\)](#page-3-2) and ([10](#page-2-5)), respectively. Simplifying Eq. ([28\)](#page-3-4) in the steady-state yields:

$$
v_2 = fRC_{2a}m_Lm_{C2}v_{2ref}/(1 - m_L + fRC_{2a}m_Lm_{C2}).
$$
 (29)

Consequently, the percentage of the steady-state error of the output voltage Δv_2 % is derived as:

Fig. 4 Comparison of the output voltage v_2 in the theoretical analysis and simulations according to changes of m_L and m_{C2}

$$
\Delta v_2\% = \frac{v_2 - v_{2\text{ref}}}{v_{2\text{ref}}} \times 100\% = \frac{m_L - 1}{fRC_{2a}m_Lm_{C2} - m_L + 1} \times 100\%.
$$
\n(30)

Similarly, the relationship between the output voltage v_2 and the mismatch ratios m_l and m_{C2} in case of $0 \leq D_2 < D_1 \leq 1$ is derived as:

$$
v_2 = \frac{fRL_aC_{2a}m_Lm_{C2}(1 - fRC_{2a}m_Lm_{C2})v_{2\text{ref}}}{L_a(1 - m_L) + fRL_aC_{2a}m_L^2m_{C2}(1 - fRC_{2a}m_{C2})}.
$$
 (31)

In this case, Δv_2 % is obtained as

$$
\Delta v_2\% = \frac{L_a(m_L - 1)(1 - \xi m_L)}{L_a(1 - m_L) + \tau m_L^2 m_{C2}(1 - \xi)} \times 100\%
$$
(32)

where $\tau = fRL_aC_{2a}$ and $\xi = fRC_{2a}m_{C2}$.

In practice, the variations of L and C_2 usually fluctuate within 20% as mentioned in Section I. Therefore, the mismatches of L and C_2 used in this study are chosen as 20%. Figure [3](#page-3-5) shows the results of Δv_2 % in the cases of $0 \le D_1 \le D_2 \le 1$ and $0 \le D_2 < D_1 \le 1$, when m_L and m_{C2} are in the range of $[0.8 \sim 1.2]$. The simulation parameters are shown in Table [1.](#page-3-6) In Fig. [3](#page-3-5), the values of Δv_2 % in both cases completely coincide. Δv_2 % has its maximum value of 0.38% at m_l = 1.2 and m_{C2} = 0.8, and its minimum value of -0.57% at $m_l = m_{C2} = 0.8$. It is worth noting that, $\Delta v_2\% = 0$ when $m_L = 1$. This means there is no steady-state error of the output voltage v_2 if *L* has a perfect match. Furthermore, the more m_L and m_{C2} differ from 1, the larger the steady-state error of v_2 .

A comparison of the output voltage v_2 in the theoretical analysis and simulations according to changes of m_L and m_{C2} is depicted in Fig. [4](#page-3-7). The output voltage v_2 in the simulation coincides with the theoretical calculation. When $m_l = m_{C2} = 0.8$ from 0.05 to 0.06 (s), the output voltage v_2 in Fig. [4a](#page-3-7) is at its farthest different from $v_{2ref} = 95$ V, which is the worst-case mismatch condition.

4 Proposed online parameter identifcation

When the parameters L and C_2 are in the mismatch condition, the predicted values in Eq. (8) (8) (8) and Eq. (12) (12) (12) move far from the actual value of the output voltage v_2 . Therefore, the actual values of L and C_2 need to be identified online to correct the obtained results. In the case of $0 \le D_1 \le D_2 \le 1$, Eq. [\(8](#page-2-3)) becomes:

$$
\delta S[k-1] + \theta Q[k-1] = v_2[k] - v_2[k-1] \tag{33}
$$

where L and C_2 are expressed through dummy parameters as:

$$
\delta = 1/LC_2, \ \theta = 1/C_2, \tag{34}
$$

and $S[k-1]$ and $Q[k-1]$ are given by:

$$
S[k-1] = \frac{nv_1[k-1]}{2f^2} (D_2[k-1] - D_2^2[k-1] - 0.5D_1^2[k-1])
$$
\n(35)

$$
Q[k-1] = -i_2[k-1]/f.
$$
 (36)

For the case of $0 \le D_2 < D_1 \le 1$, $S[k-1]$ becomes:

$$
S[k-1] = \frac{nv_1[k-1]}{2f^2}D_2[k-1](1 - D_1[k-1] - 0.5D_2[k-1]).
$$
\n(37)

In Eqs. [\(33](#page-4-1)), ([35\)](#page-4-2), and ([36\)](#page-4-3), the values of v_1 , v_2 , and i_2 are measured at the $(k - 1)$ th sampling period and serve as input data for the k^{th} sampling period. If Eq. [\(33\)](#page-4-1) is converted to matrix form, it is possible to set:

$$
Kx = h \tag{38}
$$

where:

$$
\mathbf{K} = \begin{bmatrix} S[k-1] & Q[k-1] \\ \varepsilon S[k-2] & \varepsilon Q[k-2] \\ \vdots & \vdots \\ \varepsilon^{k-3} S[2] & \varepsilon^{k-3} Q[2] \\ \varepsilon^{k-2} S[1] & \varepsilon^{k-2} Q[1] \end{bmatrix}_{(k-1)\times 2}
$$
\n
$$
\mathbf{h} = \begin{bmatrix} v_2[k] - v_2[k-1] \\ \varepsilon (v_2[k-1] - v_2[k-2]) \\ \vdots \\ \varepsilon^{k-3} (v_2[3] - v_2[2]) \\ \varepsilon^{k-2} (v_2[2] - v_2[1]) \end{bmatrix}_{(k-1)\times 1}
$$
\n(39)

and:

$$
\mathbf{x} = \begin{bmatrix} \delta \\ \theta \end{bmatrix}_{2 \times 1} . \tag{40}
$$

Matrix *K*, vector *h*, and vector *x* have sizes of $(k - 1) \times 2$, $(k-1) \times 1$, and 2×1 , respectively. The constant ε is the forgetting factor chosen in the range of $[0-1]$. If ε is too small, the noise has a greater effect on system performance possibly resulting in instability of the identifcation algorithm. Conversely, if ε is too large, the solution of the proposed algorithm largely refects old measured data, which reduces the dynamic response $[6]$ $[6]$. Since *L* and C_2 change gradually in practice, *ε* was set as 0.99 in this study.

K and *h* are not square since the number of rows are crucially greater than the number of columns. Therefore, Eq. [\(38](#page-4-4)) cannot be solved in a conventional inverse matrix. Thus, the LSA method is used to fnd the optimal solution with the LSA function $f(x)$ defined as:

Fig. 5 Flowchart of the proposed algorithm

$$
f(\mathbf{x}) = ||\mathbf{e}||^2 = ||\mathbf{K}\mathbf{x} - \mathbf{h}||^2 = (\mathbf{K}\mathbf{x} - \mathbf{h})^T (\mathbf{K}\mathbf{x} - \mathbf{h})
$$
(41)

where $e = Kx - h$ is the error vector.

After differentiating $f(x)$ with respect to x :

$$
\partial f(\mathbf{x})/\partial \mathbf{x} = 0,\tag{42}
$$

and substituting Eq. (41) into Eq. (42) (42) (42) , the following is obtained:

$$
\mathbf{x} = \left(\mathbf{K}^T \mathbf{K}\right)^{-1} \mathbf{K}^T \mathbf{h}.\tag{43}
$$

Fig. 6 Steady-state performance without and with the proposed algorithm

For the sake of convenience, Eq. ([43](#page-5-2)) is rewritten using two dummy matrices as follows:

$$
\mathbf{x} = \mathbf{U}^{-1} \mathbf{w} \tag{44}
$$

where:

$$
\mathbf{U} = \begin{bmatrix} u_{11} & u_{12} \\ u_{21} & u_{22} \end{bmatrix} = \mathbf{K}^T \mathbf{K}, \ \mathbf{w} = \begin{bmatrix} w_1 \\ w_2 \end{bmatrix} = \mathbf{K}^T \mathbf{h} \,. \tag{45}
$$

The elements of the matrix *U* and vector *w* are calculated by substituting Eq. (39) (39) into Eq. (45) (45) as follows:

$$
u_{11} = \sum_{h=1}^{k-1} \left(\varepsilon^{k-1-h} S[h] \right)^2
$$

\n
$$
u_{12} = u_{21} = \sum_{h=1}^{k-1} \left(\varepsilon^{k-1-h} \right)^2 S[h] Q[h]
$$

\n
$$
u_{22} = \sum_{h=1}^{k-1} \left(\varepsilon^{k-1-h} Q[h] \right)^2
$$

\n
$$
w_1 = \sum_{h=1}^{k-1} \left(\varepsilon^{k-1-h} \right)^2 S[h] (v_2[h+1] - v_2[h])
$$

\n
$$
w_2 = \sum_{h=1}^{k-1} \left(\varepsilon^{k-1-h} \right)^2 Q[h] (v_2[h+1] - v_2[h]).
$$

\n(46)

Fig. 7 Transient dynamic performance without and with the proposed algorithm when the load R steps down and up between 25 and 20 Ω

Fig. 8 Transient dynamic performance without and with the proposed algorithm when the reference v_{2ref} steps up and down between 95 and 100 V

Fig. 9 Transient dynamic performance without and with the proposed algorithm when the input voltage v_1 steps up and down between 100 and 105 V

Fig. 10 Photographs of the experimental setup

Fig. 11 Steady-state performance of the output voltage v_2 according to changes of m_l and m_{C2}

Fig. 12 Experimental results under initial parameter mismatches $(m_L=m_{C2}=0.8)$ without and with the proposed algorithm

From Eq. ([46\)](#page-5-4), to facilitate the implementation of the proposed algorithm in digital signal processors, these elements can be implemented as follows:

$$
u_{11}[k-1] = \varepsilon^2 u_{11}[k-2] + S^2[k-1]
$$

\n
$$
u_{12}[k-1] = \varepsilon^2 u_{12}[k-2] + S[k-1]Q[k-1]
$$

\n
$$
u_{21}[k-1] = u_{12}[k-1]
$$

\n
$$
u_{22}[k-1] = \varepsilon^2 u_{22}[k-2] + Q^2[k-1]
$$

\n
$$
w_{1}[k-1] = \varepsilon^2 w_{1}[k-2] + S[k-1] (v_{2}[k] - v_{2}[k-1])
$$

\n
$$
w_{2}[k-1] = \varepsilon^2 w_{2}[k-2] + Q[k-1] (v_{2}[k] - v_{2}[k-1]).
$$

\n(47)

Although *K* and *h* contain a great deal of data, *U* and *w* have sizes of 2×2 and 2×1 , respectively. Therefore, the calculation burden of the controller is greatly reduced by a simple inverse operation as shown in Eq. ([44\)](#page-5-5). In addition, the proposed algorithm does not require a large amount of controller memory since all of the elements of *U* and *w* are

Fig. 13 Experimental results without online parameter identifcation when load *R* steps down and up between 28 and 23 Ω

incrementally updated from previous data and the newly measured data. Thus, the proposed algorithm is suitable for low-cost digital controllers. Note that, the old measured data is less involved when *k* increases.

A fowchart of the proposed algorithm is illustrated in Fig. [5](#page-5-6). First, the values of *M* and p_u in the $(k-1)^{th}$ sampling period are calculated from the measured data from Eqs. ([25\)](#page-3-8) and ([26\)](#page-3-9). Then, a comparison is performed to calculate *S* and *Q* from Eqs. ([35\)](#page-4-2), [\(36](#page-4-3)), and ([37\)](#page-4-6). The elements of matrix *U*, vector w , and the values of δ and θ are calculated online in a simple way from previous data and the newly measured data through Eqs. (40) (40) , (44) (44) , (45) (45) , and (47) (47) . In addition, the actual values of the parameters L and C_2 are obtained by Eq. ([34\)](#page-4-8). A comparison is utilized again to calculated the optimal values of the predicted phase shift duty ratios D_1 and D_2 at the k^{th} sampling period from Eqs. [\(23](#page-3-2)), ([24\)](#page-3-3), [\(10\)](#page-2-5), and ([13\)](#page-2-12). It is worth noting that when *k* increases, the parameter identifcation process becomes more accurate, which reduces the steady-state error of the output voltage v_2 .

Fig. 14 Experimental results of the proposed algorithm when the load R steps down and up between 28 and 23 Ω

5 Simulation and experimental results

Simulation parameters are shown in Table [1](#page-3-6). Figure [6a](#page-5-7) shows the steady-state error of the output voltage v_2 when the proposed algorithm is activated under an initial parameter mismatch ($m_l = m_{C2} = 0.8$) at 0.08 (s). A steady-state error of the output voltage v_2 is observed when the parameters have mismatches. From 0.08 (s), the output voltage v_2 and the reference value almost coincide, and the steady-state error approaches zero. This is due to the fact that the values of L and C_2 are accurately identified to obtain the actual values as shown in Fig. [6b](#page-5-7) and c. In Fig. [6b](#page-5-7), the series inductor *L* approximates 60.6 μH, which is near its actual value (60 μH), while the initial value has a 20% mismatch (m_L = 0.8). For the output capacitor C_2 , the value changes from a 20% mismatch (m_{C2} =0.8) to 219 μ F, which only has a 0.45% mismatch from its actual value (220 μ F).

The transient dynamic performance of the output voltage v_2 in the presence of parameter mismatch (m_L =0.8, m_{C2} =1.2), when the load *R* changes between 25 and 20 Ω , are shown in Fig. [7](#page-6-0). When the controller operates under initial parameter mismatches, the output voltage v_2 has a steady-state error. At 0.1 (s), when the proposed algorithm

Fig. 15 Experimental results without online parameter identification when the reference v_{2ref} steps up and down between 95 and 100 V

is activated, the steady-state error is dramatically reduced, and the values of L and C_2 approach their actual values as shown in Fig. [7b](#page-6-0) and c. In addition, Fig. [7d](#page-6-0) shows the output current i_2 .

The simulation results in Fig. [8](#page-6-1) show the transient dynamics performance of the output voltage v_2 under an initial parameter mismatch (m_l = 1.2, m_{C2} = 0.8) before and after the proposed algorithm is applied when the reference v_{2ref} steps up and down between 95 and 100 V. The controller is switched to the proposed algorithm at 0.08 (s) and the effectiveness of the proposed algorithm is demonstrated.

Figure [9](#page-6-2) presents the transient dynamic performance of the output voltage v_2 when the input voltage v_1 steps up and down between 100 and 105 V under an initial parameter mismatch $(m_L = m_{C2} = 1.2)$. From 0.075 (s), the proposed algorithm is activated with online parameter identifcation, where it minimizes the steady-state error of the output voltage v_2 and provides the values of the parameters *L* and C_2 , which are almost equal to their actual values.

To evaluate the effectiveness of the proposed algorithm, an experiment was set up as shown in Fig. [10.](#page-6-3) The experimental parameters were measured by an LCR meter

Fig. 16 Experimental results with the proposed algorithm when the reference v_{2ref} steps up and down between 95 and 100 V

(Agilent) as $L=51$ µH and $C_2=219$ µF. The other parameters are shown in Table [1.](#page-3-6) Figure [11](#page-7-1) shows the steady-state performance of the output voltage v_2 according to parameter mismatches. The parameter mismatches afected the output voltage and caused the steady-state error. Moreover, the results were equal to the simulation and theoretical results shown in Fig. [4](#page-3-7). This verifes the correctness of the theoretical analysis.

Figure [12](#page-7-2) shows the experimental results of the proposed algorithm. The output voltage v_2 tracks the reference value v_{2ref} and the parameters *L* and C_2 immediately change from the initial mismatches ($m_L=m_{C2}=0.8$) to their actual values $(L=51 \mu H$ and $C_2=219 \mu F$). The experimental results are the same as the simulation results shown in Fig. [6](#page-5-7).

Experimental results under an initial parameter mismatch $(m_l=0.8, m_{C2}=1.2)$ without online parameter identification, when the load *R* steps down and up between 28 and 23 Ω , are shown in Fig. [13](#page-7-3). The steady-state error of the output voltage $v₂$ exists and slightly changes when the load *R* changes. The same scenarios were performed, and the results are shown in Fig. [14,](#page-8-1) when the proposed algorithm was applied. It can be seen that the steady-state error was signifcantly reduced.

Figure [15](#page-8-2) shows experimental results under an initial parameter mismatch (m_l = 1.2, m_{C2} = 0.8) without online parameter identification when the reference v_{2ref} steps up and down between 95 and 100 V. Due to the parameter mismatch, the output voltage v_2 cannot track v_{2ref} . This means that there is the steady-state error of the output voltage. Figure [16](#page-9-0) shows the results of the proposed algorithm with the

Fig. 17 Comparisons of transient dynamic performances: **a** DPS-PI; **b** proposed algorithm; **c** DPS-PI; **d** proposed algorithm; **e** DPS-PI; **f** proposed algorithm

same scenarios. The output voltage v_2 is always equal to v_{2ref} , which verifies the effectiveness of the proposed algorithm.

Figure [17](#page-9-1)a and b show comparisons of the experimental result obtained with the method introduced in [[5\]](#page-10-3) (DPS-PI control) and the proposed algorithm when changing v_{2ref} between 80 and 100 V, respectively. The settling times of the DPS-PI control when v_{2ref} steps up and down between 80 and 100 V are 22 (ms) and 12 (ms), respectively. This is due to the fact that, in DPS-PI control, the phase shift duty ratios are strong relative to the PI controller. Thus, even the steady-state error of the output voltage $v₂$ is mitigated, and it has low transient dynamic performance. Meanwhile, the settling times of the proposed algorithm are 2 (ms) when v_{2ref} changes. In the proposed algorithm, the PI controller is eliminated. Thus, the optimal values of the predicted phase shift duty ratios are directly derived from previous data and newly measured data by deadbeat control. Furthermore, the actual values of L and C_2 are updated online after every sampling period based on the LSA method. Therefore, when compared with the DPS-PI control, the proposed algorithm has excellent transient dynamic performance. Figure [17](#page-9-1)c and e show the transient responses of the DPS-PI control when the load *R* steps down and up between 28 and 23 Ω , respectively. Figure [17](#page-9-1)d and f show transient responses of the proposed algorithm when the load *R* steps down and up between 28 and 23 Ω , respectively. It is clear that the settling time in the DPS-PI control is very long and that the output voltage $v₂$ has dips and overshoots when the load steps down and up, respectively. Meanwhile, the proposed algorithm gives a very stable output voltage. Thus, the proposed algorithm clearly shows the excellent transient dynamic performance when changing the load.

6 Conclusions

This study presents an online parameter identifcation algorithm for DAB converters under DPS modulation with deadbeat control. The proposed algorithm signifcantly reduces steady-state error. In addition, optimally predicted phase shift duty ratios are obtained to minimize current stress using the LMM. The actual values of the series inductor and output capacitor are updated after every sampling period with the LSA method. Various scenarios were tested through simulations and experiments to show that the proposed algorithm is feasible for application in the control of DAB converters. It should be noted that the proposed idea can be extended to other phase shift modulations (SPS, EPS, and TPS) to further improve the performance of the DAB converter.

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