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Design Consideration of Bi-directional Half-Bridge Push-Pull Partial-Power-Processing Converters for Battery Energy Storage Systems

Seok-Jin Jeong[1], Nguyen-Anh Nguyen[1], Ngoc-Thao Pham[1], Jin-Su Park[1] and Sung-Jin Choi [1,*]

[1] Department of Electrical, Electronic and Computer Engineering, University of Ulsan, Ulsan 44610, Republic of Korea; hotbreak64@mail.ulsan.ac.kr (S.-J.J); nnanh1995@gmail.com (N.-A.N); ptnthao1776@gmail.com (N.-T.P); jjuu1205@mail.ulsan.ac.kr (J.-S.P)

* Correspondence: sjchoi@ulsan.ac.kr; Tel.: +82-52-259-1642

Abstract

Energy management system incorporating battery energy storage systems (BESS) is an effective way to deal with peak power demand in power system, contributing to sustainability and energy management. In this system, BESS interface converters encounter many challenges such as high efficiency, reliability and scalability. To optimize the energy conversion between BESS and the dc bus, the partial power processing (PPP) converter is one of promising methods to reduce system energy loss and increase reliability. However, implementing PPP in a BESS requires meeting a high input-to-output voltage ratio and bidirectional operation over a battery-voltage variation, which increases the design complexity. This paper proposes half-bridge push-pull converter and its design guide for that purpose. A design procedure considering system efficiency and operating principle is clearly investigated and is applied to the PPP converter operating with a 15 kW BESS. The simulation and experimental results show that the efficiency of the system reaches up to 99% with the converter efficiency of 88%, which shows that the proposed structure achieves bidirectional operation and high efficiency based on the partial power processing concept.

Keywords: Bidirectional converter, Energy Storage System (ESS), Half-bridge, Partial Power Processing, Push-pull.

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1. Introduction

With the expansion of the electric vehicle (EV) market, the rapid growth in EV energy demand is expected to increase the required capacity of charging infrastructure [1,2]. BESS has emerged as a pivotal technology for supporting grid stability, enhancing energy reliability, and facilitating the transition to a more sustainable energy future [3–5]. As a representative large-scale energy storage technology, pumped-hydro storage typically exhibits a round-trip efficiency of 75% - 85%, whereas BESS can achieve 90% - 98% [5]. By enabling the storage and dispatch of energy during periods of excess production, BESS provides critical services such as load leveling, frequency regulation, and power backup, ensuring that energy availability aligns with demand. As the scale and complexity of these systems continue to grow, there is an increasing need for high-efficiency power conversion solutions capable of handling large power ratings and meeting the stringent requirements of modern energy storage systems [6,7].

To improve the performance and efficiency of BESS, extensive research has been conducted on battery pack state estimation [8–12] and power converter control strategies

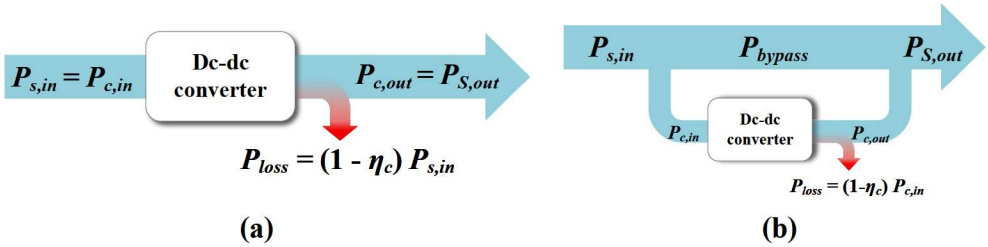

Figure 1. Conceptual diagram of power processing: (a) Full Power Processing, (b) Partial Power Processing.

[13–18]. The power converter is a central component in BESS, responsible for interfacing battery storage with the grid or load. In particular, the dc-dc converter plays a crucial role in converting the battery voltage to the required level for grid or load supply while maintaining high efficiency to minimize losses and maximize system performance [19–22]. Given the large power throughput in high-capacity BESS applications, the design of these converters must focus on minimizing conversion losses, reducing component stresses, and ensuring high reliability under dynamic operating conditions.

To address these challenges, the concept of partial power processing (PPP), shown in Fig.1, has been introduced to improve the efficiency of energy exchange between BESS and the dc grid [23–28]. In the conventional configuration in Fig.1(a), a dc-dc converter processes 100% of the power flow between the BESS and the dc grid, which is referred to as full power processing (FPP). However, the FPP concept faces several challenges: as the BESS power increases, the converter rating increases proportionally, leading to a linear rise in component cost and practical difficulty in selecting suitable components [29]. Furthermore, the dc-dc converter accounts for a significant portion of the total power loss in the BESS. In contrast, in Fig.1(b), the converter processes only a small portion of the total power flowing between the BESS and the dc grid; thus, PPP can achieve a reduced converter rating and improved efficiency compared to its FPP counterpart. Therefore, PPP can be a viable solution for downsizing power converters and improving overall system efficiency.

Recent PPP studies have mainly focused on applications with operating voltage variations, such as photovoltaic generation [30,31], wind power [32], and BESS. As mentioned earlier, PPP can enhance overall efficiency by reducing the power processed through the converter, thereby lowering conversion losses and thermal burden in high-power interfaces. However, achieving a lower power processing ratio may require a higher input-output voltage ratio than in FPP. Especially in BESS applications, a systematic design procedure is essential to ensure stable bidirectional operation across wide operating conditions.

BESS is regarded as a key target for PPP because its terminal voltage varies significantly with the charge and discharge state, while high efficiency and power density are required for high-power, large-capacity operation. Although prior studies have demonstrated the feasibility of PPP-based interfaces and reported high efficiencies and reduced processed-power fractions, systematic design procedures that guarantee stable bidirectional operation over the full battery-voltage range remain limited.

In PPP, the converter handles only a portion of the overall voltage conversion, which yields an effective input–output voltage ratio that differs from that of FPP under identical operating conditions. This effective voltage ratio can deviate significantly from that of FPP as the fraction of system power processed by the converter decreases. Based on that property, various dc-dc converter topologies have been investigated and applied for various battery applications. Granello *et al.* implemented a flyback-based battery charger operating in PPP at 5.5 kW, achieving over 99% system efficiency while the converter processed only

21% of the total system power. In addition, a design procedure for the proposed PPP topology was presented [33]. Iyer *et al.* applied a dual active bridge (DAB) converter to an EV fast-charging station using PPP, in which the converter processed 27% of the system power and its design procedure was also proposed [34]. Cao et al. developed a 15 kW rated CLLC-based PPP battery charger that reduces the processed-power fraction to near zero at nominal voltage and keeps it below 20% across most of the operating range, achieving a peak efficiency of 98.8% through a systematic decoupled design procedure[35]. Abdel-Rahim *et al.* proposed a current-fed dual inductor push-pull PPP architecture, in which 25% of the system power is processed by the converter; however, the design methodology for component and experimental hardware validation could be further investigated [36].

Among the various bidirectional PPP converter candidates, DAB is one of the most widely adopted topologies due to its symmetric circuit structure and simple operating principle [37–44], together with various control methods [45,46]. However, DAB employs a relatively large number of switching devices, which increases cost and often requires advanced control methods to achieve high performance [47]. Furthermore, as discussed earlier, reducing the fraction of system power processed by the converter can lead to a significantly increased or decreased effective input–output voltage ratio. This imbalance in the voltage ratio results in substantially higher current on one side of the converter compared to the other, thereby increasing conduction losses and degrading the overall converter efficiency and the lifetime of switching components.

To mitigate these drawbacks, the half-bridge push-pull (HBPP) structure is a viable bidirectional PPP candidate. Compared with DAB-based implementations, HBPP can reduce the number of active switches and alleviate device current stress, particularly on the secondary side, which can contribute to improved efficiency in high-power BESS interfaces. These attributes make HBPP a promising topology for PPP-based BESS applications, where efficiency and reliability are of primary importance. Nevertheless, a systematic and practical design methodology for HBPP-based bidirectional PPP converters has not yet been sufficiently investigated.

In this paper, the bidirectional PPP converter design framework is presented for BESS. The proposed approach targets applications requiring both a high voltage conversion ratio and bidirectional operation over a battery voltage range. To meet these requirements with reduced converter power rating, a HBPP PPP topology is adopted and its operating principles are systematically analyzed. The present study further completes the validation of the proposed design methodology by implementing and testing a 15 kW hardware prototype under charge and discharge conditions. Then, the main contributions of this paper are as follows:

- The design requirements and practical constraints for implementing PPP in parallel BESS (e.g., bidirectional operation, high conversion ratio, and feasible duty ratio) are identified and discussed.
- A bidirectional HBPP PPP converter is analyzed in a mode-by-mode manner, providing design-oriented insights into its steady-state operation.
- A unified design procedure is established to select duty ratio, transformer turns ratio, and passive/active components over the battery voltage operating range.
- The proposed converter and design methodology are validated through simulations and 15 kW experimental results, including efficiency and loss breakdown analysis.

2. Configuration of PPC-integrated battery energy storage systems

2.1. Operation principle of the partial power processing

As discussed in the previous section, the PPP concept indicates that the converter handles only a portion of the total system power. In other words, PPP aims to reduce or

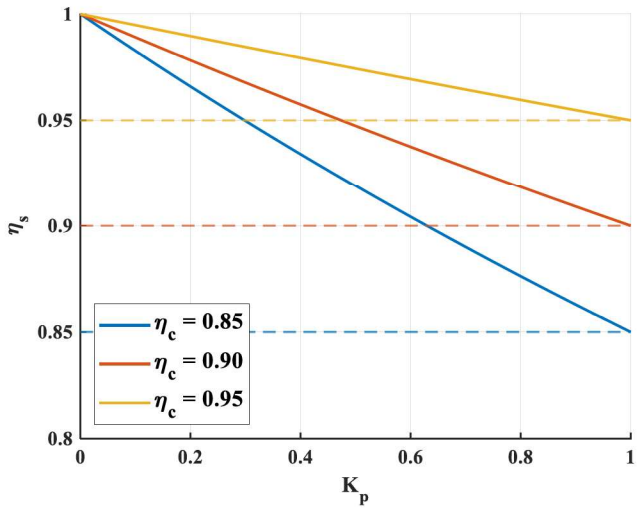

Figure 2. System efficiency vs. the power processing ratio for various converter efficiencies.

eliminate unnecessary power conversion, thereby minimizing losses in the overall power handling process. The advantages of employing the PPP concept include: (1) system efficiency improvement, (2) converter size reduction, which will be discussed in detail in the following sections.

2.1.1. System efficiency improvement

As shown in Fig. 1(a), the system output power ($P_{s,out}$) is equal to the converter output power ($P_{c,out}$) in FPP, since all the power is processed by the converter. Thus, the system loss is identical to the converter loss.

$$P_{loss,FPP} = P_{c,in} \cdot (1 - \eta_c) = P_{s,in} \cdot (1 - \eta_s) \tag{1}$$

where $P_{c,in}$ and $P_{s,in}$ are the input power of the converter and system, respectively. Therefore in FPP, the system efficiency (η_s) is also equal to the converter efficiency (η_c).

$$\eta_{s,FPP} = \frac{P_{s,out}}{P_{s,in}} = \frac{P_{c,out}}{P_{c,in}} = \eta_c \tag{2}$$

In contrast, in the case of PPP shown in Fig. 1(b), the system output power ($P_{s,out}$) can be expressed as the sum of the bypassed power (P_{bypass}) and the power processed by the converter ($P_{c,out}$), as given in (3).

$$P_{s,out} = P_{bypass} + P_{c,out} \tag{3}$$

To represent the ratio of the power processed by the converter to the power handled by the system, the power processing ratio (K_p) is defined as:

$$K_p = \frac{P_{c,out}}{P_{s,out}}. \tag{4}$$

Accordingly, $P_{c,out}$ can be expressed in terms of the power processing ratio

$$P_{c,out} = K_p \cdot P_{s,out}, \tag{5}$$

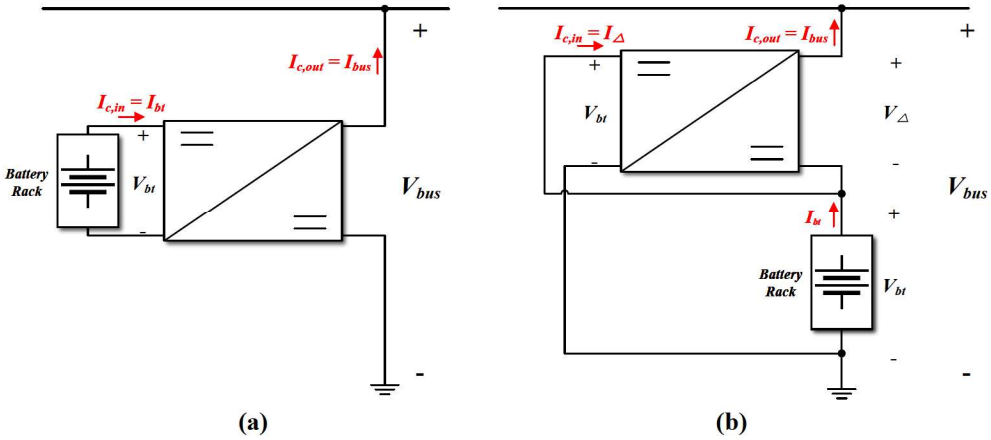

Figure 3. Block diagram of battery interface converters: (a) Full Power Processing, (b) Partial Power Processing.

and the bypassed power (P_{bypass}) can be expressed as:

$$P_{bypass} = (1 - K_p) \cdot P_{s,out}. \tag{6}$$

Since converter efficiency (η_c) is defined as the ratio of its output power to its input power as:

$$\eta_c = \frac{P_{c,out}}{P_{c,in}}, \tag{7}$$

from (4) and (7), the converter input power $P_{c,in}$ can be derived as

$$P_{c,in} = \frac{P_{c,out}}{\eta_c} = \frac{K_p \cdot P_{s,out}}{\eta_c}. \tag{8}$$

Since the overall system efficiency (η_s) is the ratio of the system's output power ($P_{s,out}$) to its input power ($P_{s,in}$), where the input power is the sum of the converter's input power ($P_{c,in}$) and the bypassed power (P_{bypass}), the following holds.

$$\eta_s = \frac{P_{s,out}}{P_{s,in}} = \frac{P_{s,out}}{P_{c,in} + P_{bypass}} \tag{9}$$

By substituting (6) and (8) into (9), the system efficiency (η_s) can be derived as a function of power processing ratio (K_p) and the converter efficiency (η_c) as follows.

$$\eta_s = \frac{P_{s,out}}{\frac{K_p P_{s,out}}{\eta_c} + (1 - K_p) P_{s,out}} = \frac{\eta_c}{K_p + (1 - K_p)\eta_c} \tag{10}$$

Therefore, from (10), system efficiency (η_s) is a function of converter efficiency (η_c) and the power processing ratio (K_p). It can be observed that, regardless of how small η_c is, the system efficiency approaches unity as K_p approaches zero. Consequently, in a PPP system, power processing ratio (K_p) can be utilized as an index to evaluate the performance of the PPP. Fig. 2 shows the effect of variations in K_p and η_c on the system efficiency η_s. When K_p is equal to unity, the converter processes the entire system power, and thus η_c becomes equal to η_s. However, when K_p becomes less than 1, meaning that the converter processes only a portion of the system power, it can be observed that the system efficiency (η_s) becomes higher than the converter efficiency (η_c).

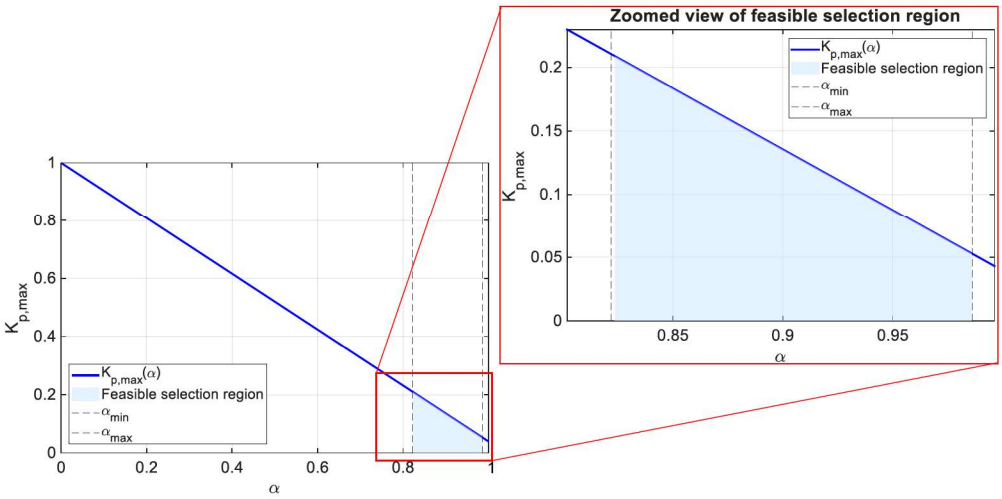

Figure 4. Evaluation of battery voltage ratio α and maximum power processing ratio $K_{p,max}$.

2.1.2. Size Reduction

Another significant advantage of employing PPP is the reduction in converter size. This can be understood through the following analysis. Fig. 3 illustrates the configurations of the battery interface converters for FPP and PPP, along with their respective current flows during battery discharge mode. The details about PPP configuration will be discussed in the following section.

From Fig. 3(b), applying Kirchhoff's Voltage Law (KVL) yields:

$$V_{bus} = V_{bt} + V_{\Delta} \tag{11}$$

where V_{Δ} is the headroom voltage processed by the PPP converter and V_{bus} is the dc bus voltage. In Fig. 3(b), power processing ratio K_p in discharging mode in (4) can be expressed as:

$$K_p = \frac{V_{\Delta} I_{bus}}{V_{bus} I_{bus}} = \frac{V_{\Delta}}{V_{bus}}. \tag{12}$$

Considering the battery voltage can vary during the operation, then K_p also varies according to the variation of the battery voltage. Therefore, K_p in this system comes to have a certain range, from $K_{p,min}$ to $K_{p,max}$. Each K_p can be expressed as:

$$K_{p,min} = \frac{V_{\Delta,min}}{V_{bus}} \tag{13}$$

and

$$K_{p,max} = \frac{V_{\Delta,max}}{V_{bus}}. \tag{14}$$

By applying (11) to (13) and (14), the above expressions can be rewritten as follows. In case of the $K_{p,min}$:

$$K_{p,min} = \frac{V_{bus} - V_{bt,max}}{V_{bus}}. \tag{15}$$

and for the $K_{p,max}$:

$$K_{p,max} = \frac{V_{bus} - V_{bt,min}}{V_{bus}} \tag{16}$$

where $V_{bt,max}$ and $V_{bt,min}$ represent the maximum battery voltage and minimum battery voltage, respectively. From (16), we can obtain the condition for whether the PPP can be satisfied within the allowable battery-voltage range. Here, for clarity, we define α as the

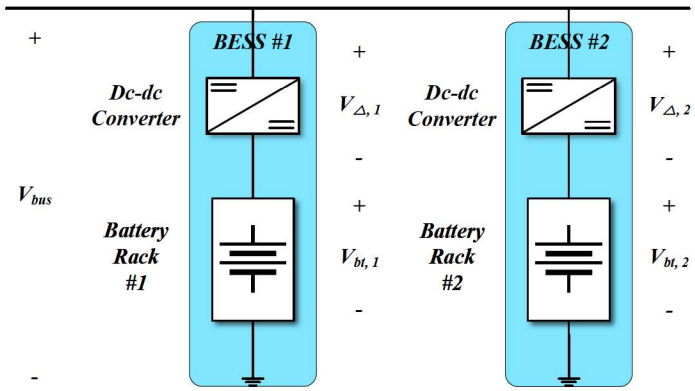

Figure 5. Parallel BESS architecture with dc-dc converter.

ratio of the maximum battery voltage to the minimum battery voltage, which are defined as:

$$\alpha = \frac{V_{bt,min}}{V_{bt,max}}. \tag{17}$$

By substituting (17) into (16), $K_{p,max}$ can be rewritten as:

$$K_{p,max} = \frac{V_{bus} - \alpha V_{bt,max}}{V_{bus}}. \tag{18}$$

Therefore, the converter power reduction ratio is determined by the battery voltage ratio α. A wider battery voltage range (a smaller α) requires a converter designed with a higher maximum power processing ratio $K_{p,max}$. Fig. 4 illustrates that when $\alpha = 0.84$, the converter must be rated for higher power to satisfy a power processing ratio exceeding 0.2. In contrast, when $\alpha = 0.96$, the required converter power rating is significantly reduced, enabling a very high system efficiency, as $K_{p,max}$ remains below 0.05.

2.2. System Configuration for Partial Power Processing

To improve the reliability and operational flexibility of the battery, a parallel BESS architecture has been researched [21,48,49]. However, voltage difference of each battery, resulting from the state of charge (SOC) imbalance, induces unintended circulating currents among the parallel units, which lead to unnecessary lifetime degradation and potential safety issues. To address these challenges, the parallel BESS architecture necessitates the integration of a dedicated dc-dc converter for each BESS unit as shown in Fig. 5.

The role of PPP in this system is the same as that of a series voltage regulator (SVR), to maintain the voltage of the BESS equal to V_{bus}, regardless of the variations in V_{bt}. In this configuration, the role of the dc-dc converter is to compensate for the voltage difference between the dc bus and the battery rack, thereby ensuring the BESS voltage equals the dc bus voltage.

As previously mentioned, to implement partial power processing, it is necessary to share either the voltage or the current. Therefore, two different connection schemes can be considered, as illustrated in Fig. 6. In Fig. 6(a), the converter is connected in parallel with the battery on one side, while its other side is connected in series between the battery and the dc bus. In this paper, according to its connection, this configuration is referred to as Battery-Parallel and DC bus-Series (BPDS).

In contrast, Fig. 6(b) shows a configuration where the dc bus is connected in parallel with the converter, with the opposite side maintaining the same series connection as in Fig. 6(a). For the same reason, this configuration is called DC bus-Parallel and Battery-

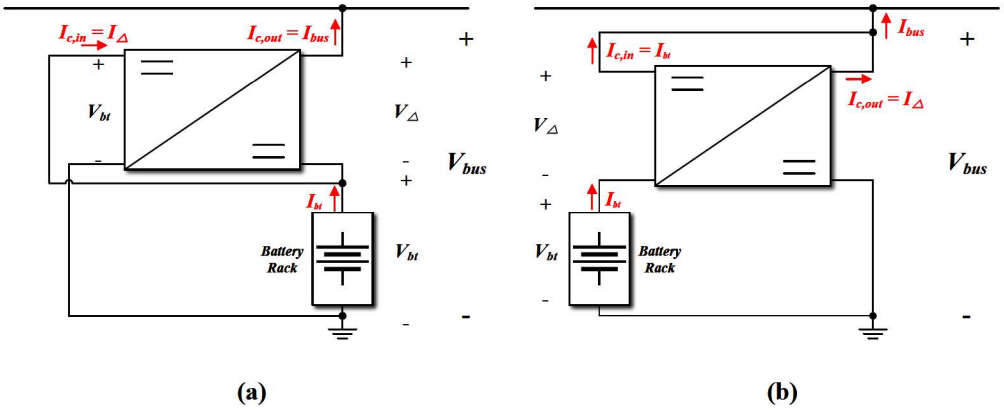

Figure 6. Candidate PPP configurations: (a) Battery Parallel and DC bus Series, (b) DC bus Parallel and Battery Scrics.

Series (DPBS). In both configurations, applying Kirchhoff's Current Law (KCL) gives the following equation.

$$I_{bus} = I_{bt} + I_\Delta \tag{19}$$

where I_Δ is the processed current handled by the PPP converter.

In both cases, the converter is able to maintain and regulate the headroom voltage (V_Δ). However, the two configurations show differences in the aspect of circulating power. Fig. 7 illustrates the power flow of converter and system during battery discharging operation[50]. When the system operates in battery discharging mode as shown in Fig. 7(a), converter receives and processes battery voltage. In this operating mode, the directions of the system power and the converter-processed power are identical. However, the power flow of discharging operation in Fig. 7(b), clearly demonstrates circulating power. Therefore, the converter draws power from the dc bus, processes it, and delivers it back to the dc bus.

In the discharging mode, K_p for the two operating modes is derived as follows:

$$K_{p,BPDS(dis)} = \frac{V_\Delta \cdot I_{bus}}{V_{bus} \cdot I_{bus}} = \frac{V_\Delta}{V_{bus}}. \tag{20}$$

$$K_{p,DPBS(dis)} = \frac{V_\Delta \cdot I_{bt}}{V_{bus} \cdot I_{bus}} = \frac{V_\Delta}{V_{bus}}(1 + \frac{I_\Delta}{I_{bus}}). \tag{21}$$

Under the same input–output voltage condition, the DPBS configuration yields a higher K_p than the BPDS configuration, as can be seen by comparing (20) and (21). Similarly, in the charging mode, K_p of BPDS is expressed as:

$$K_{p,BPDS(ch)} = \frac{V_{bt} \cdot I_\Delta}{V_{bt} \cdot I_{bt}} = \frac{I_\Delta}{I_{bt}}. \tag{22}$$

In case of the DPBS:

$$K_{p,DPBS(ch)} = \frac{V_{bus} \cdot I_\Delta}{V_{bt} \cdot I_{bt}} = \frac{I_\Delta}{I_{bt}}(1 + \frac{V_\Delta}{V_{bt}}). \tag{23}$$

Also in charging mode, DPBS configuration shows higher K_p than BPDS. Therefore, under the given conditions, configuring both the discharging and charging modes as BPDS is the most favorable option. However, due to the inherent constraints of the system interconnection, this is not feasible in practice. Consequently, one operating mode must be configured as BPDS, while the other must be configured as DPBS. Thus in this paper, the BPDS configuration is selected for battery discharging mode and DPBS for charging mode.

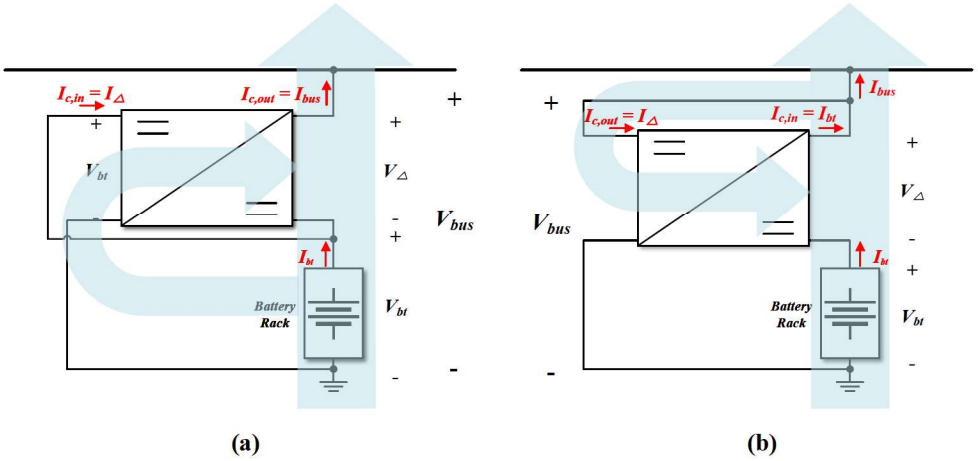

Figure 7. Power flow analysis in battery discharging mode: (a) Battery Parallel and DC bus Series, (b) DC bus Parallel and Battery Series.

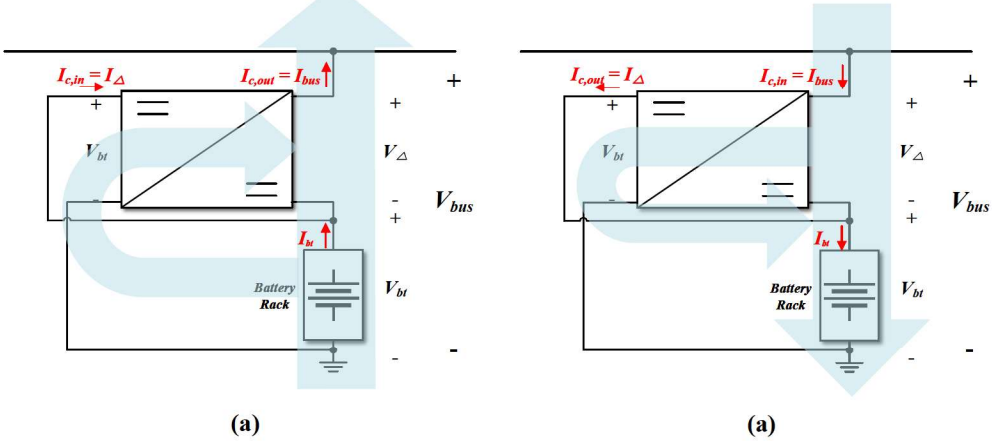

Figure 8. Power flow analysis of BPDS configuration: (a) Battery discharging mode, (b) Battery charging mode.

Fig. 8 (a) and (b) illustrates the power flow directions in the converter and the system during both discharging and charging operations of selected configuration, respectively.

3. Proposed converter topology

3.1. Required features

To achieve bidirectional power flow with PPP, the converter applied in this system needs several requirements:

- Isolated converter is preferred.
  According to [27], both isolated (e.g., DAB, flyback) and non-isolated topologies (e.g., buck-boost, SEPIC) can be employed for implementing PPP systems. However, if non-isolated topologies are applied to the configuration in Fig. 6(a), a short-circuit path is formed between the negative terminal of the converter and the battery, as illustrated in Fig. 9. Therefore, to prevent a short-circuit in this configuration, galvanic isolation of the converter output stage via a transformer is required. Furthermore, the use of a transformer facilitates achieving a high input-output voltage ratio, which will be discussed in a later section.
- High input-output voltage ratio (G_v) is essential.

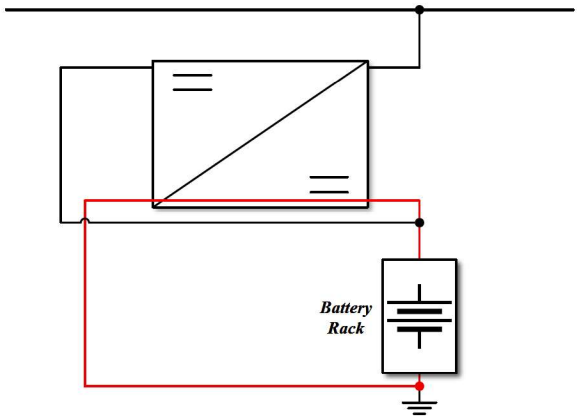

Figure 9. Illustration of the potential short-circuit path due to the common ground in non-isolated configurations.

In the PPP, the dc-dc converter demands a higher voltage gain than in the FPP. As discussed previously, Fig. 7(a) and (b) illustrate the conceptual block diagrams of a PPP-based BESS in discharging and charging mode. Considering the power flow through the converter, the converter operates in step-up mode to charge battery and in step-down mode to discharge it. In both modes, (11) and the following equation hold.

$$i_{bt} = i_{c,out} + i_{c,in}. \tag{24}$$

In the discharging mode, the voltage gain of the PPP converter in Fig. 7(b) is expressed as follows.

$$G_{v(PPP)} = \frac{V_{\Delta}}{V_{bt}} = \frac{V_{bus} - V_{bt}}{V_{bt}}. \tag{25}$$

On the other hand, in the FPP shown in Fig. 5, the voltage gain is expressed as:

$$G_{v(FPP)} = \frac{V_{bus}}{V_{bt}}. \tag{26}$$

By substituting (26) into (25), the following relationship is obtained.

$$G_{v(PPP)} = G_{v(FPP)} - 1. \tag{27}$$

Therefore, from (27), it can be proven that the dc-dc converter for PPP-based BESS requires a lower voltage gain than FPP-based BESS in discharging mode. However, in charging mode, the voltage gain is expressed as the reciprocal of (27), which exhibits a higher voltage gain compared to FPP. Considering the voltage gain requirements in both operational modes, a transformer is typically employed to achieve a high voltage conversion ratio, even though the PPP configuration is inherently a non-isolated structure.

3.2. Topology Selection

Taking into account what was mentioned earlier, the three isolated bidirectional topologies shown in Fig. 10 considered for the PPP implementation. In every topology in Fig. 10, the primary side is connected to the battery and the secondary side is placed between the dc-bus and the battery, the primary voltage, V_p, is always much higher than the secondary voltage, V_s. In Table 1, three topologies are compared in terms of various criteria. Compared to FBDAB, the other two can reduce the number of switching components by half, thereby decreasing the volume of converter. Between the remaining two topologies,

Table 1. Comparison of converter topologies

Parameter	FBDAB [51]	HBDAB [52]	HBPP
System Power [kW]	7.5	0.63	15
Converter Power [kW]	7.5	0.63	1.1
No. of Switching components	8	4	4
No. of Capacitors	2	4	3
No. of Inductors	1	1	2
No. of Transformers	1	1	1
Voltage stress (Primary switch)	High	High	High
Voltage stress (Secondary switch)	Low	Low	Medium
Current stress (Primary switch)	Low	Medium	Medium
Current stress (Secondary switch)	Medium	High	Medium

HBPP can lower the secondary side conduction loss owing to its reduced RMS current. In the case of an HBDAB, the half-bridge structure inherently imposes higher current stress on the switches compared to a full-bridge DAB of the same rating, making it unsuitable for PPP configurations that require higher current.

In contrast, the HBPP benefits from its dual-inductor push-pull structure, which reduces the current stress on the switching components and makes it more suitable for the series-connected section of a PPP configuration.

In addition, the HBPP offers the following advantages from a voltage perspective. In conventional push-pull structures of HBPP, high peak voltage is commonly applied to the switching components during switching. However, in the BPDS structure used in this paper in Fig. 8, the push-pull terminal is connected in series with the dc bus and the battery, thereby mitigating the voltage stress applied to the switching components. Considering these factors, the HBPP is selected as the most suitable topology in terms of switch count and stress.

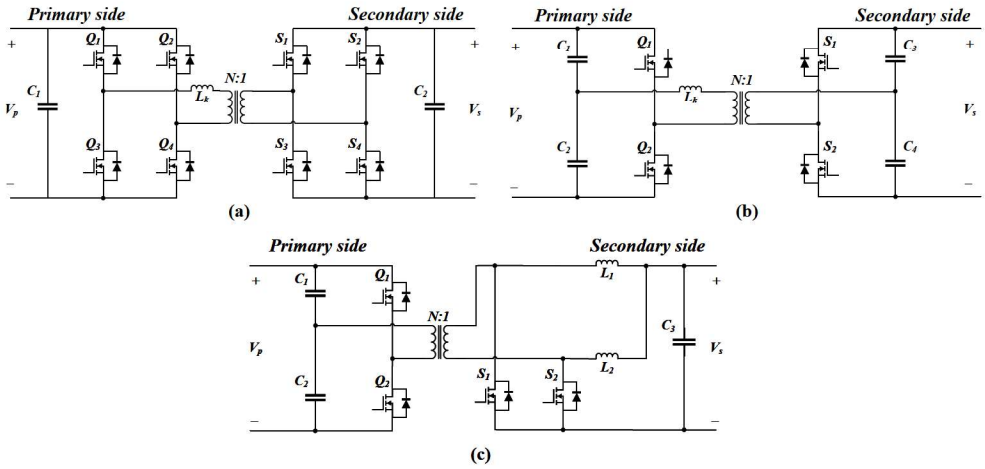

Figure 10. Proposed topology and applications: (a) Full-Bridge Dual Active Bridge (FBDAB), (b) Half-Bridge Dual Active Bridge (HBDAB), (c) Half-Bridge Push-Pull (HBPP).

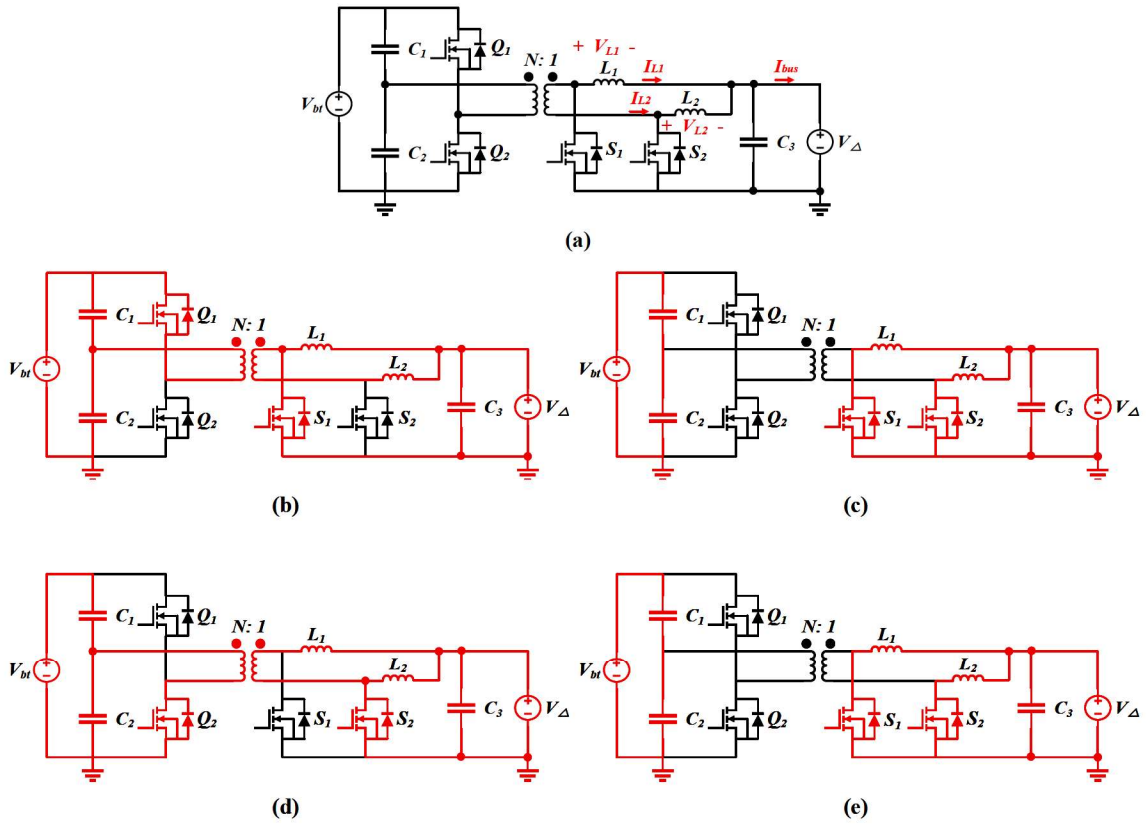

Figure 11. Analysis of the operation mode: (a) Equivalent circuit, (b) Interval 1 ($t_0 \sim t_1$), (c) Interval 2 ($t_1 \sim t_2$), (d) Interval 3 ($t_2 \sim t_3$), (e) Interval 4 ($t_3 \sim t_4$).

3.3. Operation Analysis

Fig. 11 is a circuit diagram of the proposed topology. As shown in the figure, the half-bridge side is connected to the battery V_{bt}, while the push-pull side is connected between the battery and the dc bus and the voltage is represented as V_Δ. At the push-pull side, an interleaved structure employs two inductors is applied to achieve a reduction in the output current ripple. The primary and secondary sides are also referred as the half-bridge and push-pull sides, respectively.

The converter can be operated in either step-down mode or step-up mode. In the step-up mode, the power flows from the push-pull side to the half-bridge side, whereas in the step-down mode, the power is flowing from the half-bridge side to the push-pull side. In the following analysis, the reference directions of voltage and current are defined based on the step-down mode operation, following the passive sign convention shown in Fig. 11(a). The on-off signals of each switch over time, along with the corresponding operational waveforms of the converter, are shown in Fig. 12. The detailed operating principles of each mode are described as follows.

- Interval 1 ($t_0 \sim t_1$)
  At $t = t_0$, Q_1 is turned on and S_2 is turned off while S_1 is turned on as shown in Fig. 11(b). Therefore, the voltage applied to the primary winding of the transformer is

$$V_P = -\frac{V_{bt}}{2}, \tag{28}$$

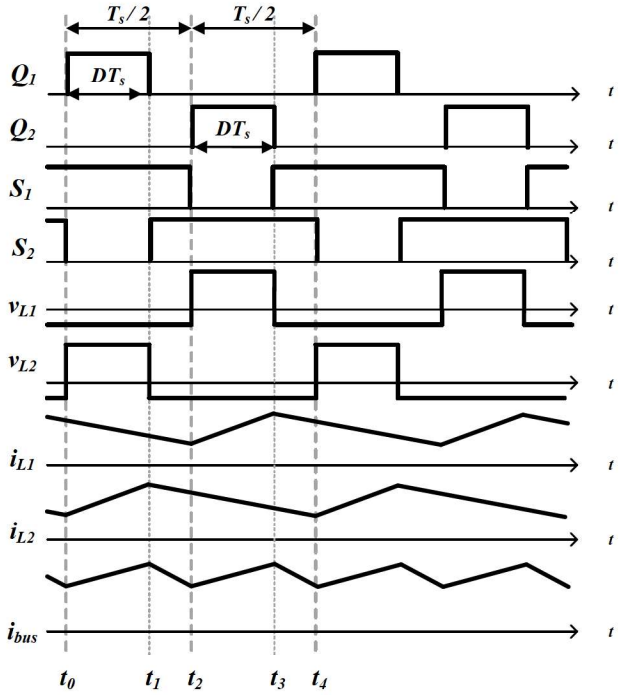

Figure 12. Switching voltage and current waveforms of the HBPP topology in step-down mode.

Thus, the voltage applied to each inductor can be expressed as

$$V_{L1} = -V_\Delta \tag{29}$$

$$V_{L2} = \frac{V_{bt}}{2N} - V_\Delta. \tag{30}$$

In step-down mode, L_1 is connected to V_Δ through S_1 and releases its stored energy, while L_2 is connected to C_1 and stores energy from V_{bt}.
In step-up mode, in contrast, L_1 stores energy through S_1 and L_2 releases the energy into V_{bt}.

- Interval 2 $(t_1 \sim t_2)$
At $t = t_1$, Q_1 is turned off to ensure the deadtime for the half-bridge and S_2 is turned on while keeping S_1 on as shown in Fig. 11(c). In other words, both push-pull side switches are turned on. Therefore, the voltage of L_1 and L_2 is given as follows.

$$V_{L1} = V_{L2} = -V_\Delta \tag{31}$$

Therefore, both inductors discharge the stored energy to V_Δ in the step-down mode, or they are charged by V_Δ in the step-up mode. Thus, there is no power flow between the primary and secondary sides via the transformer, during this interval.

- Interval 3 $(t_2 \sim t_3)$
At $t = t_2$, Q_2 is turned on and S_1 is turned off while S_2 is turned on as shown in Fig. 11(d). The operations in Interval 1 and Interval 3 are similar to each other and thus the following holds.

$$V_P = \frac{V_{bt}}{2} \tag{32}$$

$$V_{L1} = \frac{V_{bt}}{2N} - V_\Delta \tag{33}$$

$$V_{L2} = -V_{\Delta} \tag{34}$$

In step-down mode, L_1 is energized by the transformer. The power starts to flow from the primary side to the secondary side. Therefore, L_1 stores energy and i_{L1} increases. Similar to L_1 in Interval 1, L_2 releases energy to V_{Δ}.
In the step-up mode, L_1 releases energy to the primary side of the transformer, and C_2 is charged while C_1 is discharged by the primary reflected current of i_{L1}. In this mode, L_2 stores energy through S_2.

- Interval 4 $(t_3 \sim t_4)$
At $t = t_3$, Q_2 is turned off to ensure the deadtime for the half-bridge and S_1 is turned on while keeping S_2 on. It operates in a similar way as interval 2 as shown in Fig. 11(e) and the following holds.

$$V_{L1} = V_{L2} = -V_{\Delta} \tag{35}$$

Both inductors are to store energy in step-up mode operation, or release energy in step-down mode operation during this time interval. By the voltage-second balance of L_1 and L_2, the voltage step-down ratio of the converter can be defined as a function of the primary-side switch duty ratio (D) and the transformer turns ratio (N) as follows:

$$G_v = \frac{V_{LV}}{V_{HV}} = \frac{V_{\Delta}}{V_{bt}} = \frac{D}{2N}. \tag{36}$$

where D is the duty cycle of primary side switching components, Q_1 and Q_2. Since the voltage ratio is the reciprocal of (36) when the power flow reverses, increasing the transformer turns ratio N yields a reduced voltage ratio during discharge operation and an increased voltage ratio during charging.

3.4. Design Procedure

- Duty cycle (D)
The first step is to select the duty cycle of the converter. In this study, the duty cycle of the primary side switches (Q_1, Q_2) is defined as D, while the duty cycle of the secondary side switches (S_1, S_2) is controlled as $1 - D$.
- Battery voltage range ($V_{bt,min}$, $V_{bt,max}$)
Next, according to the dc bus voltage V_{bus}, the battery operating range must be determined. Assuming the converter output current (I_{bus}) is controlled to be constant during battery discharge mode, the range of K_p in the discharge mode is defined by the following equation:

$$K_{p,min} = \frac{V_{\Delta,min}}{V_{bus}} = 1 - \frac{V_{bt,max}}{V_{bus}} \tag{37}$$

$$K_{p,max} = \frac{V_{\Delta,max}}{V_{bus}} = 1 - \frac{V_{bt,min}}{V_{bus}} \tag{38}$$

Considering the voltage step-down ratio defined in (36), it must meet the following relationships:

$$V_{\Delta,min} \leq \frac{D_{min} \cdot V_{bt,max}}{2N} \tag{39}$$

and

$$V_{\Delta,max} \geq \frac{D_{max} \cdot V_{bt,min}}{2N}. \tag{40}$$

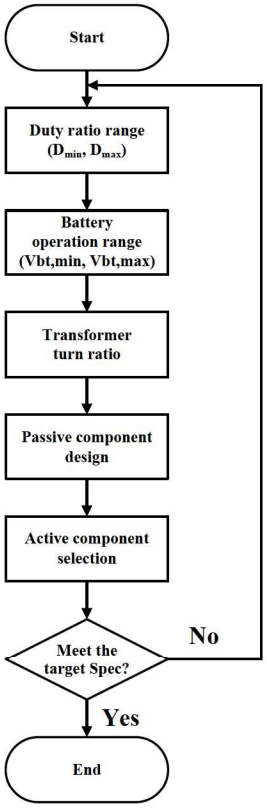

Figure 13. Design flow of proposed procedure.

Thereby, $V_{\Delta,max}$ and $V_{\Delta,min}$ can be described as follows:

$$V_{bt,max} + \frac{D_{min} \cdot V_{bt,max}}{2N} \geq V_{bus} \tag{41}$$

$$V_{bt,min} + \frac{D_{max} \cdot V_{bt,min}}{2N} \leq V_{bus}. \tag{42}$$

Therefore, by equating (41) and (42), battery voltage ratio in (17) can be rewritten.

$$\alpha = \frac{V_{bt,min}}{V_{bt,max}} = \frac{2N + D_{min}}{2N + D_{max}} \tag{43}$$

To lower $K_{p,min}$, $V_{bt,max}$ must be set close to V_{bus}. However, as indicated by (41), this requirement, combined with the D_{min} constraint, necessitates a high turn ratio (N). From (43), it is evident that as the turn ratio (N) increases, the battery voltage ratio α approaches unity. This implies that a high N significantly narrows the battery's operational voltage range, as $V_{bt,min}$ is constrained to be very close to $V_{bt,max}$. Therefore, a clear trade-off exists between the battery operating voltage range and the transformer turn ratio. If the target BESS employs a battery type whose terminal voltage varies significantly with the state of charge—such as Nickel Manganese Cobalt (NMC) or sodium-based batteries—a relatively low turn ratio N becomes essential to secure a sufficiently wide operating voltage window. In contrast, for chemistries such as Lithium Iron Phosphate (LFP), where the voltage variation over the SOC range is comparatively small, a higher turn ratio can still cover most of the usable range, while also helping reduce K_p.

- Transformer turn ratio (N)

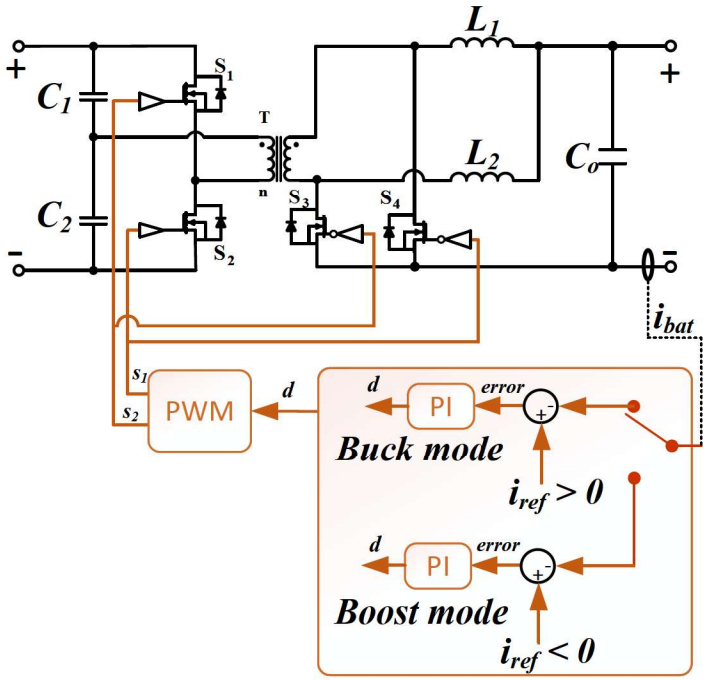

Figure 14. Control strategy of HBPP converter.

The feasible range for the transformer turn ratio (N) is determined by the constraints derived in the previous section. From the maximum battery voltage condition (39), the lower limit of N is obtained by rearranging the terms as follows:

$$N \geq \frac{D_{min} \cdot V_{bt,max}}{2 \cdot (V_{bus} - V_{bt,max})} \tag{44}$$

Similarly, from the minimum battery voltage condition (40), the upper limit of N is found:

$$N \leq \frac{D_{max} \cdot V_{bt,min}}{2 \cdot (V_{bus} - V_{bt,min})} \tag{45}$$

- Passive components design
  L_1 and L_2 are calculated by the inductor ripple current specification:

$$L_{1,2} = \frac{V_{bt} \cdot (1 - 2D)D}{2N \cdot \Delta i_{bus}} T_s \tag{46}$$

where Δi_{bus} is the ripple current of dc bus. From (46), N and T_s are fixed values, and the V_{bt} determines the value of L. Since the term $(1 - 2D)D$ reaches its maximum value at $D = 0.25$. It is advisable to design V_{bt} at $D = 0.25$ to become the midpoint of the battery operation range, V_{bt} in (46) can therefore be treated as

$$V_{bt} = \frac{V_{bt,min} + V_{bt,max}}{2}. \tag{47}$$

The values of the half-bridge side filter capacitors, C_1 and C_2, are calculated in the step-up mode operation of the converter while the value of push-pull side filter capacitor C_3 is calculated in the step-down mode operation by the capacitor voltage ripple specifications, as follows.

$$C_{1,2} = \frac{DT_s \cdot I_{bus}}{\Delta v_{c1,c2} \cdot 4N} \tag{48}$$

Table 2. BESS specifications and electrical grid parameters

Parameter	Symbol	Value
DC Bus Voltage	V_{bus}	380 [V]
Battery Voltage	V_{bt}	$350 \sim 360$ [V]
Headroom Voltage	V_{Δ}	$20 \sim 30$ [V]
Switching frequency	f_{sw}	100 [kHz]
Transformer turn ratio	N	2
Inductance	L_1, L_2	100 [uH]
Capacitor (Primary)	C_1, C_2	33 [uF]
Capacitor (Secondary)	C_3	100 [uF]
MOSFET (Primary)	Q_1, Q_2	C3M0075120K
MOSFET (Secondary)	S_1, S_2	IMW65R027M1H

$$C_3 = \frac{V_{bt}(1-2D)D}{32NL \cdot \Delta_{v_{c3}}} T_s^2 \tag{49}$$

where $\Delta v_{c1,c2}$ and Δv_{c3} represent the voltage ripple of the capacitors C_1, C_2, and C_3, respectively and I_{bus} is the total current of the push-pull side denoted in Fig. 11(a), which is described as

$$i_{bus} = i_{L1} + i_{L2} + i_{C3}. \tag{50}$$

- Active components design
  The drain-to-source voltage stresses for the primary ($V_{ds,pri}$) and secondary ($V_{ds,sec}$) sides are given by (51) and (52), respectively:

$$V_{ds,pri} = V_{bt} \tag{51}$$

$$V_{ds,sec} = \frac{V_{bt}}{2N}. \tag{52}$$

  Assuming the current ripple is negligible, the RMS currents for the primary ($I_{rms,Pri}$) and secondary ($I_{rms,Sec}$) sides are expressed as (53) and (54), respectively:

$$I_{rms,pri} = \frac{I_{bus}\sqrt{D}}{2N} \tag{53}$$

$$I_{rms,sec} = \frac{I_{bus}}{2}\sqrt{1+2D}. \tag{54}$$

  Therefore, the switching devices for both sides must be selected with voltage and current ratings that provide a sufficient margin above these calculated stresses (the voltage and the RMS current) to ensure reliable operation. The entire design flow is illustrated in Fig. 13.

3.5. Loss Breakdown

To analyze the power loss of the converter, the losses of the transformer and inductors are assumed to be negligible. Therefore, in this section, the total converter power loss is approximated as the power loss of the MOSFETs. The MOSFET losses consist of conduction loss, switching loss, output capacitance C_{oss} loss, and body diode loss, as described in [53]. The MOSFET conduction loss is caused by the drain-to-source current flowing through

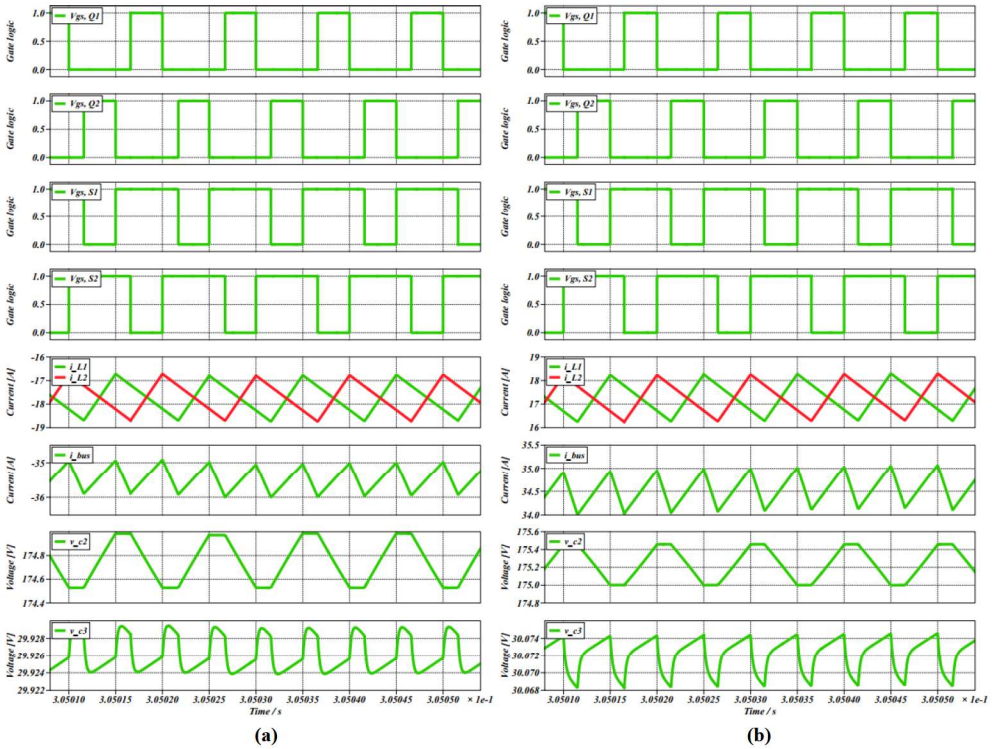

Figure 15. Simulation waveform of the proposed topology: (a) Battery charging mode, (b) Battery discharging mode.

the on-state channel resistance during the conduction interval. The conduction loss is calculated as

$$P_{cond} = I_{ds}^2 \cdot R_{ds(on)} \cdot D \cdot n_{fet} \tag{55}$$

where I_{ds} is the drain-to-source current, $R_{ds(on)}$ is the on-state resistance, D is the duty cycle, and n_{fet} is the number of MOSFETs. The switching loss is determined by the total energy dissipated during the turn-on and turn-off transitions. The average switching power loss is expressed as

$$P_{sw} = V_{ds} I_{ds} \cdot (t_{on} + t_{off}) \cdot f_{sw} \cdot n_{fet} \tag{56}$$

where V_{ds} is the drain-to-source voltage, t_{on} and t_{off} are the turn-on and turn-off times of the MOSFET, and f_{sw} is the switching frequency. The C_{oss} loss represents the energy dissipated during the charging and discharging of the MOSFET output capacitance in each switching cycle and is given by

$$P_{Coss} = E_{oss} \cdot f_{sw} \cdot n_{fet} \tag{57}$$

where E_{oss} is the output capacitance energy loss per switching event, which can be obtained from the device datasheet. The body diode loss is the power dissipated when the intrinsic body diode conducts current, typically during dead-time intervals or reverse current operation. This loss is caused by the forward voltage drop of the diode and is calculated as

$$P_{Diode} = V_F I_{ds} \cdot D_{diode} \cdot n_{fet} \tag{58}$$

where V_F is the diode forward voltage and D_{diode} is the fraction of time during which the diode conducts. Finally, the total MOSFET power loss is calculated as

$$P_{loss,total} = P_{cond} + P_{sw} + P_{Coss} + P_{Diode}. \tag{59}$$

4. Design Implementation and Validation

4.1. Simulation

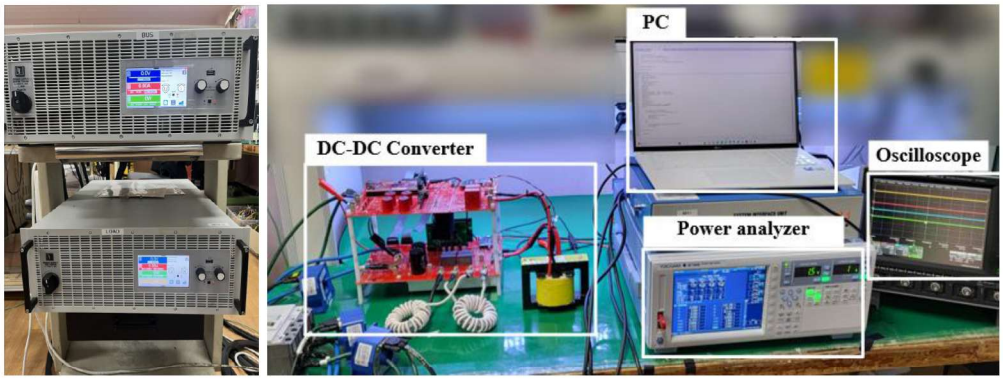

Figure 16. Hardware configuration: (a) bidirectional power supplies, (b) Overall view of converter hardware setup.

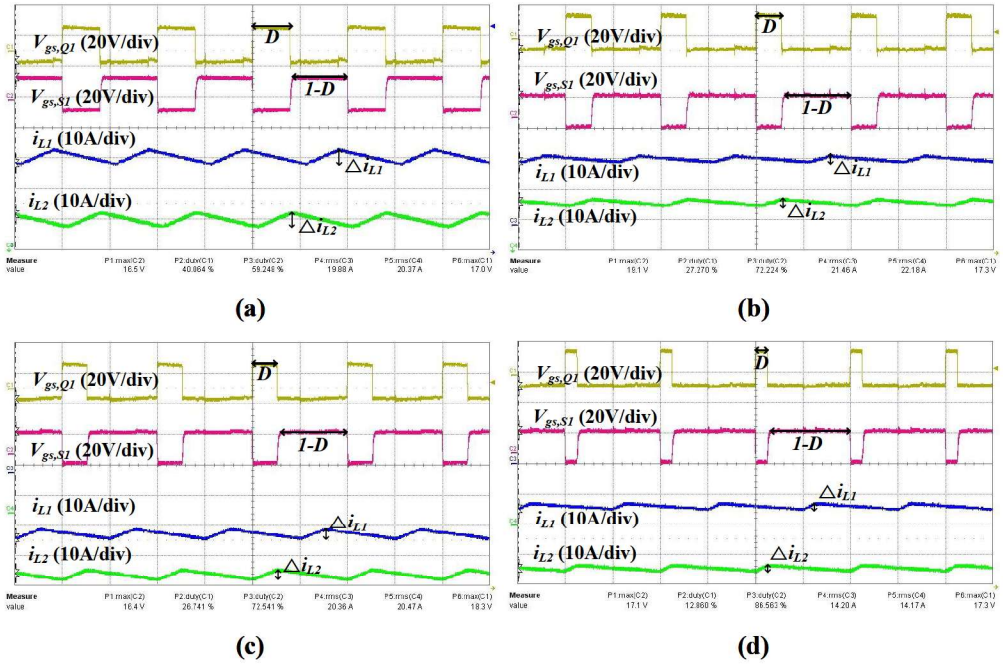

Figure 17. Converter operation waveforms: (a, b) Discharging at V_{bt} 350 V and 360 V, (c, d) Charging at V_{bt} 350 V and 360 V.

To verify the proposed design approach for the 15 kW partial-power-processing (PPP) system, a HBPP converter was designed. The duty ratio D was constrained to the range of 10% to 45%, reflecting the duty-cycle limitation of the half-bridge topology, and the battery voltage range was specified as 350 - 360 V. Based on these specifications, the transformer turns ratio N was determined using (45) and was required to be less than 2.625. Accordingly, the nearest feasible value, $N = 2$ was selected. For an operating bus current of I_{bus} = 35 A, the inductances L_1 and L_2 were each designed as 100 uH to limit the current ripple to below 5%. Furthermore, to constrain the voltage deviation ΔV_Δ and limit the battery-side voltage ripple to 0.5%, the capacitors C_3 and C_1, C_2 were designed as summarized in Table 2.

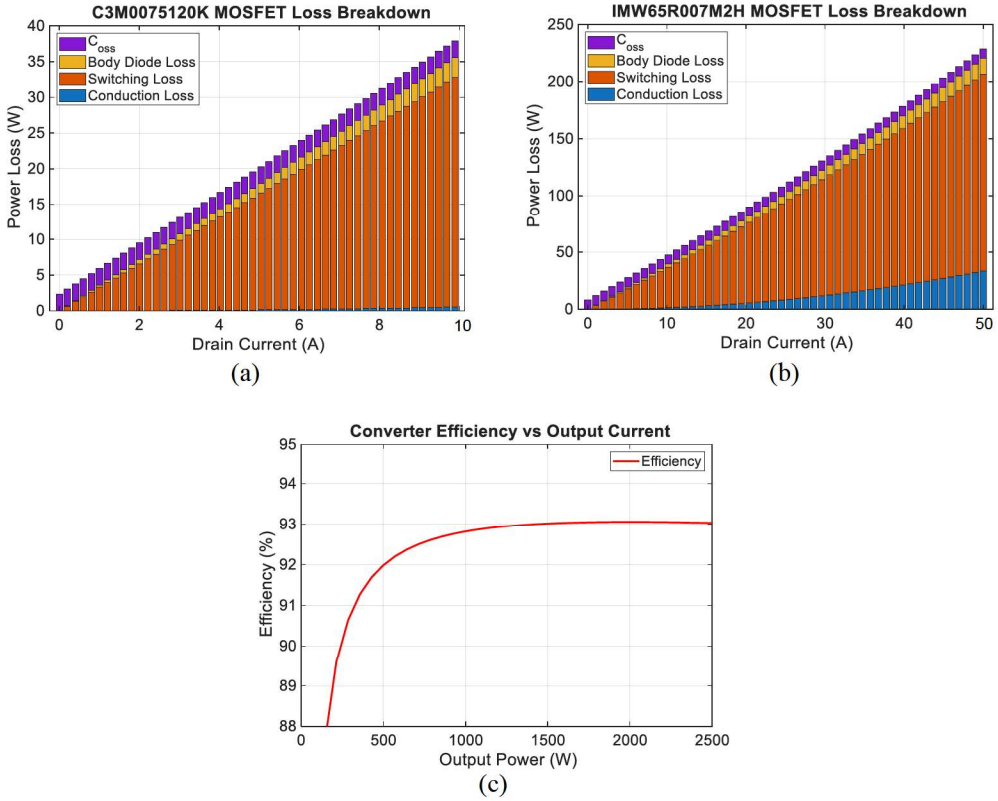

Figure 18. Loss breakdown analysis: (a) Primary switches using C3M0075120K, (b) Secondary switches using IMW65R007M2H, and (c) HPBB converter efficiency.

The operation of the designed converter was first verified through PLECS simulation[54]. As shown in this figure, two separate PI controllers were designed based on the converter modeling approach presented in [53].

In buck mode, when energy is transferred from the high-voltage side to the low-voltage side, the reference current I_{ref} is set to a positive value. Conversely, in boost mode, when energy flows from the low-voltage side to the high-voltage side, the reference current I_{ref} is assigned a negative value. The converter was operated under constant current (CC) control with $I_{ref} = \pm$ 35 A across all voltage ranges, based on the control strategy shown in Fig. 14. Here, I_{ref} is the reference current used to regulate I_{bus} at a constant level.

Fig. 15 illustrates the simulation waveforms. The parameters used in the simulation are listed in Table 2. To limit the Δi_{bus} to less than 1.2 A, L_1 and L_2 were designed to be 100uH. The simulation results confirm this, showing a measured Δi_{bus} of approximately 1.07 A. The capacitors C_1, C_2 and C_3 were designed using (48) and (49), respectively. The maximum voltage ripple was designed to be 0.5% of the V_{bt} for C_1 and C_2, and 0.05% of the V_Δ for C_3. The simulation confirmed that $\Delta_{V_{c1}}$ was approximately 0.31% and $\Delta_{V_{c3}}$ was under 0.03%, thus satisfying the design requirements.

4.2. Experimental validation

Fig. 16(b) shows the prototype converter, along with the test environment used for its evaluation. Two bidirectional power supplies shown in Fig. 16(a) are used as the battery and dc bus. Fig. 17 displays the primary waveforms of the converter during operation in a 35 A constant current (CC) mode. The measurements encompass the gate-source signals of switching components Q_1 and S_1, the current of L_1 and L_2, respectively. In more detail, the

Table 3. Summary of key parameters under different V_{bt} condition.

V_{bt} [V]	**350**	**355**	**360**
Battery power [W]	12,935	12,375	12,828
Converter power [W]	1,081	769	741
K_p	0.08	0.06	0.06
$V_{ds,sec(peak)}$ [V]	88.21	89.5	90.67
$I_{d,sec(peak)}$ [A]	37.11	34.622	35.94
L_1 & L_2 [µH]		100	

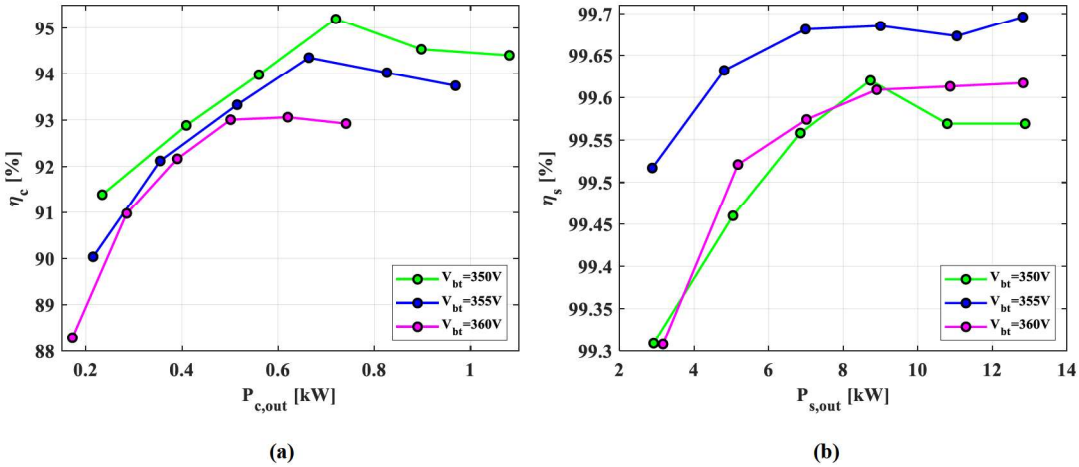

Figure 19. Measured efficiency in discharging mode: (a) Converter, (b) System.

overall operation waveforms of battery charging mode in Fig. 17(a) and battery discharging mode in Fig. 17(b) are similar to each other, with the direction of i_{L1} and i_{L2} inversed.

Unlike the simulation, which assumes a relatively ideal environment, the hardware validation stage showed some voltage drops in both the dc bus and the battery. This effect is largely influenced by the resistance of the wiring used to connect the dc bus and the battery to the converter, with each wire having a resistance of approximately 0.1 Ω. Including these additional voltage drops in (36), the I_{bus} achievable in the simulation stage may exceed the duty range in the actual hardware experiment, making it unattainable. Considering this, the maximum I_{bus} during operation was limited to 35 A in hardware verification stage.

Fig. 18 presents the loss breakdown analysis using the C3M0075120K MOSFET on the high-voltage side and the IMW65R007M2H MOSFET on the low-voltage side. The simulation results indicate that the primary-side switches experience high voltage stress but relatively low current conduction, resulting in comparatively low power loss. The maximum power loss on the high-voltage side is 37.9 W at the 2.5 kW operating condition, as shown in Fig. 18(a). In contrast, the low-voltage-side MOSFETs experience significantly higher current stress, leading to substantially higher power loss. As shown in Fig. 18(b), the maximum loss on the low-voltage side reaches 228.7 W at the 2.5 kW load condition. Based on these results, the overall converter efficiency is estimated to reach approximately 93% at full load.

Fig. 19 illustrates the efficiency of converter and system with the various battery voltage under the constant V_{bus}. While the maximum efficiency of the converter is approximately 95.2% at $P_{c,out}$ = 720 W, the system efficiency remained above 99.3% across

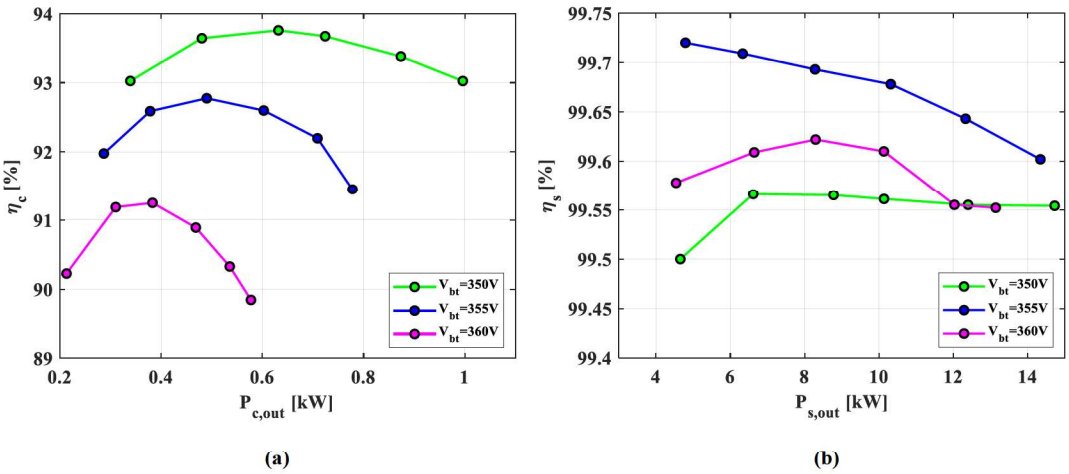

Figure 20. Measured efficiency in charging mode: (a) Converter, (b) System.

the entire operating range. A similar trend is observed in the charging mode shown in Fig. 20; while the converter efficiency peaks at approximately 93.7% at $P_{c,out}$ = 630 W, the system efficiency consistently remains above 99%. From Fig. 19(a), although the converter efficiency (η_c) at V_{bt} = 360 V is the lowest among the tested conditions, the power processing ratio K_p at this voltage is the lowest also. As a result, the overall system efficiency (η_s) shown in Fig. 19(b) remains comparable to that at V_{bt} = 350 V. Similar behavior is observed in the charging mode results of Fig. 20. At V_{bt} = 360 V, converter efficiency again reaches its minimum; however, due to the relatively low K_p, the system efficiency at this voltage becomes comparable to that of the V_{bt} = 350 V. However, the system efficiency at V_{bt} = 360 V still remains lower than that at V_{bl} = 355 V. This suggests that both the power processing ratio K_p and the converter efficiency must be jointly considered to achieve higher system efficiency.

Fig. 21 presents error analysis plot of the theoretical efficiency against the empirically measured efficiency in battery discharging mode in (a) and charging mode operation in (b). The theoretical system efficiency was calculated using (10), where the K_p was calculated based on (22). When calculating system efficiency η_s, measured converter efficiency η_c from the power analyzer is used. Even though the measured system efficiency and the theoretical system efficiency differ by only a small margin up to 0.3%, it was confirmed that two values are very similar to each other.

Table 3 presents the key operating parameters of the proposed converter under varying battery voltage conditions, from 350 V to 360 V. As the battery voltage varies within this range, the peak current of the secondary side MOSFET remains relatively stable, with values of 37.11 A, 34.622 A and 35.94 A, respectively. This current behavior demonstrates that the proposed power handling strategy prevents excessive semiconductor stress under constant power operating conditions. Furthermore, the inductance of L_1 and L_2 is fixed at 100 uH for all operating points, ensuring the same current ripple characteristic across the entire voltage range. This design choice allows for a fair comparison of device stress and loss distribution, as variations in current ripple and switching dynamics are minimized.

5. Conclusions

This study investigated the design consideration of bidirectional partial power processing (PPP) converters for battery energy storage systems (BESS), focusing on achieving high system efficiency while reducing converter size and power handling requirements. By analyzing the characteristics of PPP-based architectures, the half-bridge push-pull (HBPP)

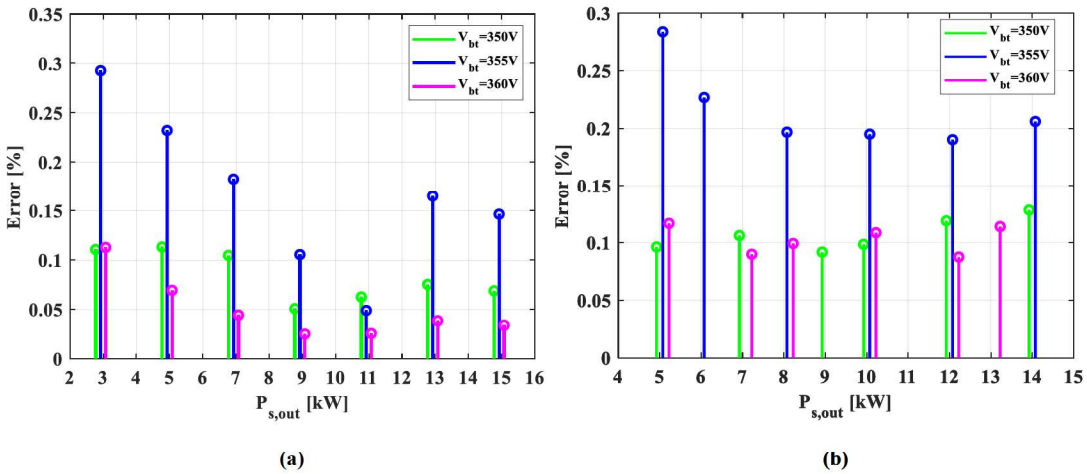

Figure 21. Error analysis of theoretical and measured system efficiency: (a) Battery charging mode, (b) Battery discharging mode.

structure was selected as a suitable topology due to its reduced conduction loss, minimized device stress and favorable current characteristics on the secondary side. A detailed operational analysis was provided, including interval-based switching behavior and voltage gain derivation, and a systematic design procedure was established to guide the selection of the duty ratio, transformer turn ratio, and passive and active components under practical battery voltage conditions.

The feasibility and performance of the proposed design were validated through simulation and hardware experiments under an 15 kW BESS hardware test bed. This prototype successfully demonstrated stable bidirectional power flow and achieved a peak system efficiency exceeding 99.4%, confirming the beneficial impact of PPP in reducing processed power and improving overall energy conversion performance. Although the converter efficiency remained below 91% at partial load, the experimental results verified that the overall system efficiency is significantly enhanced due to the small power processing ratio, in accordance with the analytical expectations. Minor discrepancies between simulation and experimental current limits were attributed to parasitic resistance and minimum duty constraints, indicating areas for hardware refinement.

The analysis and results of this work highlight the practical value of PPP-based converter architectures for next-generation energy storage systems where high efficiency, modular scalability, and reduced converter rating are essential. Future research will focus on optimizing soft-switching conditions, extending the design methodology to higher power or higher frequency operation. The proposed converter can also be investigated within grid-connected parallel BESS architectures using partial power processing, including the development of advanced control strategies. Furthermore, extending the concept to hybrid ESS configurations that integrate additional storage elements—such as hydrogen fuel cells—offers another promising direction. Finally, system-level evaluation of long-term reliability and large-scale parallel operation remains essential for further improving the practicality of the proposed HBPP-PPP topology.

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