Design Considerations of Asymmetric Half-Bridge for Capacitive Wireless Power Transmission

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***Abstract*—Capacitive power transfer has an advantage in the simplicity of the energy link structure. So, the conventional phase -shift full bridge sometime is not always the best choice because of its complexity and high cost. On the other hand, the link capacitance is usually very low and requires high-frequency operation, but, the series resonant converter loses zero-voltage switching feature in the light load condition, which makes the switching loss high especially in CPT system. The paper proposes a new low-cost topology based on asymmetric half-bridge to achieve simplicity as well as wide zero voltage switching range. The design procedure is presented, and circuit operations are analyzed and verified by simulation.**

Keywords—Zero voltage switching, capacitive wireless power transfer, asymmetric half-bridge

I. Introduction

Nowadays, wireless power transfer is widely applied in electric vehicles, internet of thing devices, light-emitting diode, and biomedical application [1]. The inductive wireless power transfer (IPT) has been accepted with successful implementations. Recently, the capacitive wireless power transfer (CPT) has been proposed as the solution to replace the IPT systems as shown in Fig. 1. It uses electric fields instead of magnetic fields, to transfer energy through metal barriers without significant power losses. The advantage of CPT is the reduction of the cost and weight of energy coupler structure. Among various topology available in CPT systems [2], [3], [4], phase-shift full-bridge is usually regarded as the most suitable topology, because it can control the magnitude and frequency of the primary voltage. However, it requires four power switches and gate drivers, which makes the system complex and expensive. On the other hand, in order to achieve ZVS, the operating frequency should be tied to the inductive region which is placed above the resonant frequency. So, the gain curve is heavily dependent on the load, which makes the control difficult. Furthermore, it only steps down the voltage gain and thus cannot cover the wide input voltage variations.

To overcome these problems, a new half-bridge structure incorporating a buck-boost is proposed as shown in Fig. 2. The output voltage can be regulated by the duty ratio control that can achieve a wide input range. The proposed structure provides wide zero-voltage-switching (ZVS) by adding the parallel inductance, L_p, and operates in a resonant mode where the control becomes easy. Furthermore, the boost operation is possible. In this paper, the operating principle is presented with operation mode and zero voltage switching analysis.

II. Proposed Topology

Figure 2 shows the proposed topology, where two active switches, S_1 and S_2, are driven by asymmetrical pulse-width-modulated (APWM) gating pulses, and the floating capacitor, C_{cr}, together with the parallel inductor, L_P, forms a buck-boost configuration [5]. Therefore, the average voltage of the capacitor and the peak-to-peak current in the parallel inductor can be derived as

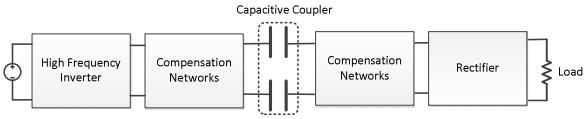

Fig. 1. Typical structure of a CPT systems.

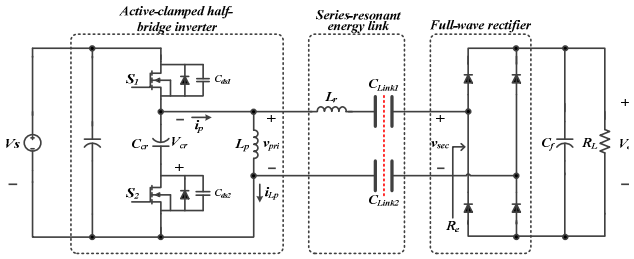

Fig. 2. Proposed topology.

$$V_{cr} = \frac{D}{1-D} V_s \tag{1}$$

and

$$\Delta L_P = \frac{TD}{L_p} V_s . \tag{2}$$

Because the proposed topology is controlled by a PWM gating signal at the resonant frequency, f_o, and mostly operated in the high quality factor of the resonance, the primary voltage waveform, $v_{pri}(t)$, is expressed by the Fourier series, and only the fundamental component can be considered for simplicity. Thus, the magnitude of the fundamental voltage is well approximated by

$$v_{pri,f}(t) = \frac{2V_s}{\pi(1-D)} \sin(\pi D), \tag{3}$$

where

$$f_o = \frac{1}{2\pi\sqrt{L_r (C_{link1} \parallel C_{link2})}}. \tag{4}$$

Since the buck-boost converter and the half-bridge [5] are merged together, it is clear that the output voltage can be regulated directly by changing the duty ratio of S_1 and the dc voltage gain is given by

$$\frac{V_o}{V_s} = \frac{\sin(\pi D)}{2(1-D)} \le \frac{\pi}{2}. \tag{5}$$

Figure 3 shows that the voltage gain of the proposed topology is wide in comparison with the conventional half-bridge. However, since the switching voltage stress increases as the voltage gain increases, the maximum allowable duty should be limited.

III. Operation Analysis

The operation analysis for each time interval in Fig. 4 is shown as follows.

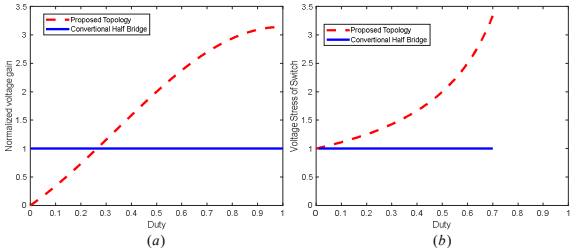

Fig. 3. (a) The voltage normalized gain (b)The switching voltage stress normalized by input voltage.

Stage 1 [$t_0 < t < t_1$]: The switch S_1 is turned ON while the switch S_2 is OFF. The current in L_P is charged as (6), the drain-to-source voltage of switch S_2 reaches its maximum value as (7), and the primary voltage, v_{pri}, becomes the same as the input voltage, V_s.

$$i_{L_p}(t) = \frac{V_s}{L_p}(t - t_0) + i_{L_p}(t_0) \tag{6}$$

$$V_{cds2}(t_0) = \frac{V_s}{1 - D} \tag{7}$$

Stage 2 [$t_1 < t < t_2$]: It starts when the switch S_1 is turned OFF while the switch S_2 is still OFF. The energy stored in the inductors, L_p, and L_r, charge the parasitic output capacitor of S_2 while the output capacitor of S_1 is discharged, which makes the ZVS possible.

Stage 3 [$t_2 < t < t_3$]: It starts when the switch S_2 is turned ON while the switch S_1 is OFF. At $t=t_2$ the parasitic output capacitor of S_2 is fully discharged. Thus, S_2 turns ON in ZVS condition, the drain-to-source voltage of switch S_1 reaches its maximum value as in (8) and the current flowing in L_p, C_{cr}, and L_r are summed to be zero as in (9).

$$v_{cds1}(t_3) = \frac{V_s}{1 - D}, \tag{8}$$

$$i_{L_p}(t) + i_{L_r}(t) + i_{cr}(t) = 0\,. \tag{9}$$

Stage 4 [$t_3 < t < t_4$]: It starts when the switch S_2 is turned OFF while S_1 is OFF. In this stage, the energy stored in the inductors L_p and L_r is used to charge the parasitic output capacitor of S_2 and discharge the output capacitor of S_1. Thus, the ZVS can be achieved.

IV. Zero Voltage Switching Condition

This section discusses the ZVS condition in the proposed method. The ZVS occurs while the parasitic output capacitor of the switch is initially at zero before the switch turns on [6]. Considering the total charge in C_{ds1} and C_{ds2}, which is given by

$$q_{sw} = (C_{ds1} + C_{ds2})\frac{V_s}{1 - D}\,. \tag{10}$$

This amount of charge needs to be displaced during the dead-time, t_d, to satisfy the ZVS. The maximum amount of charge is the total charge in L_p that can be expressed as follows.

$$q_{L_p} = \frac{\theta_d}{\omega}\left(\frac{V_s}{\omega L}(\theta_d - 2\pi D) + i_{L_p}(-\pi D)\right), \tag{11}$$

where

$$\theta_d = \frac{2\pi}{T} t_d\,. \tag{12}$$

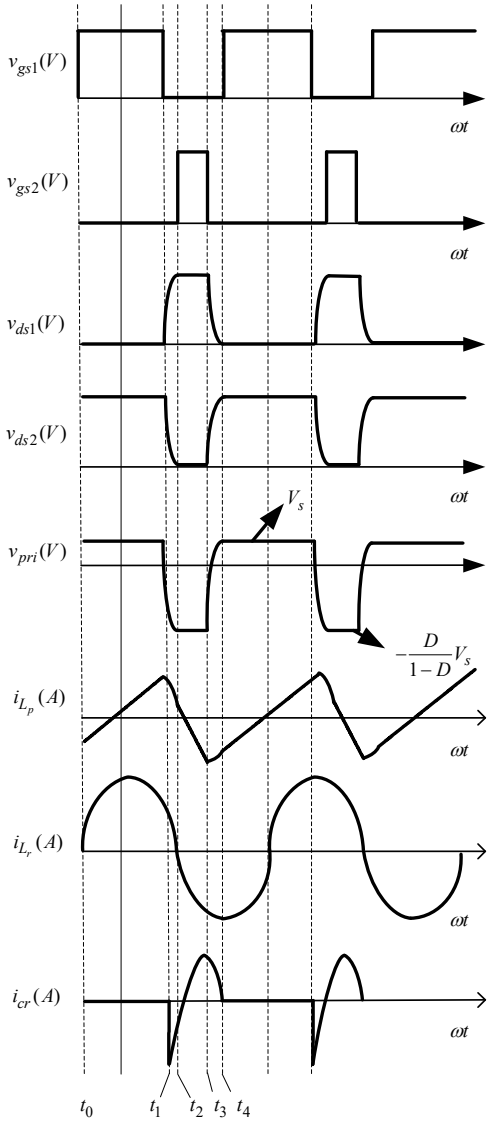

Fig. 4 Steady-state waveform (D > 0.5)

TABLE I
SIMULATION PARAMETERS

Parameter	Value
V_s	$100V$
V_o	$115V$
$Duty$	0.5
f_o	$141kHz$
L_p	$246uH$
$C_{ds1} = C_{ds2}$	$240\,pF$
C_{cr}	$0.11uF$
L_r	$1407uH$
C_{link}	$1.8nF$
C_f	$10uF$
R_L	200Ω
t_d	$300ns$

To satisfy ZVS, the condition of $q_{L_p} \geq q_{sw}$ should be met, and is given by

$$\frac{\theta_d}{\omega}\left(\frac{V_s}{\omega L}(\theta_d - 2\pi D) + i_{Lp}(-\pi D)\right) \geq (C_{ds1} + C_{ds2})\frac{V_s}{1-D}. \quad (13)$$

V. Simulation Results

The proposed topology is verified by the simulation in PSIM. Table I shows parameters of simulation. The ZVS condition is achieved as shown in Fig. 5. The values from the simulation are almost same as the theoretical calculation. The waveforms of the current in the parallel inductor and the current of the clamp capacitor match well with operation analysis in section II.

VI. Conclusion

This paper proposes an asymmetry half-bridge topology for capacitive wireless power transmission. Since it has the features of the wide voltage gain, less active component, simple gate driving, and wide ZVS range, it is expected to further strengthen the merits of CPT over IPT system.

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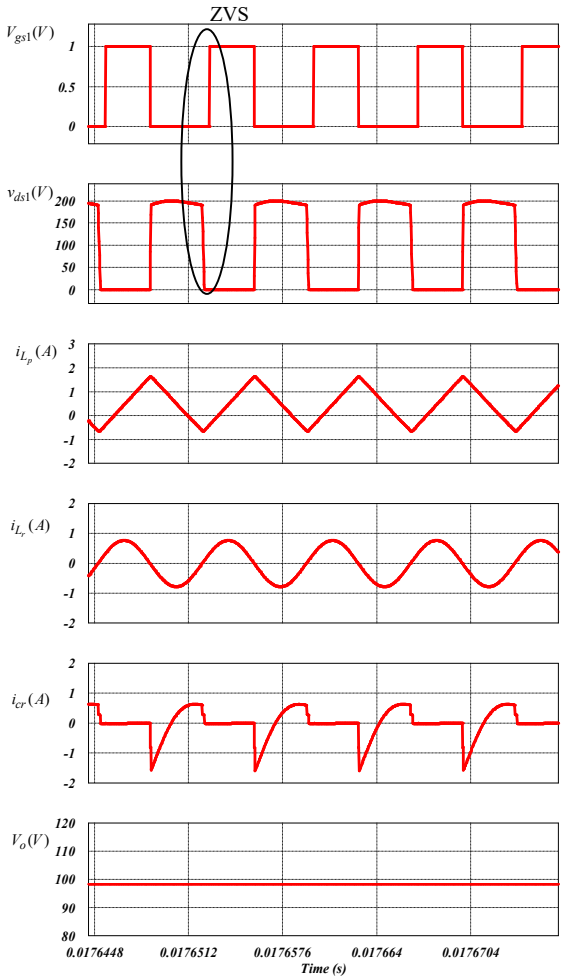

Fig. 5. Simulation Results

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