Single-Stage PWM Converter for Dual-Mode Control of Capacitive Wireless Power Transmission

Chae-Ho Jeong
School of Electrical Engineering
University of Ulsan
Ulsan, Republic of Korea
e-mail:cogh6253@mail.ulsan.ac.kr

Hee-Su Choi
Silicon Mitus Inc.
Seongnam, Republic of Korea
e-mail:sky911020@naver.com

Sung-Jin Choi
School of Electrical Engineering
University of Ulsan
Ulsan, Republic of Korea
e-mail:sjchoi@ulsan.ac.kr

***Abstract*—In capacitive wireless power transfer system, effective capacitance of the energy link between the transmitter and receiver changes according to variations in separation distance or degree of alignment in electrodes, which would modify the resonant frequency and degrade the system performance. To compensate for such a change, it is necessary to track the resonance frequency. In this case, frequency control scheme cannot be used for the output voltage regulation. Conventionally, additional DC/DC converter has been adopted in the front of the transmitter or in the back of the receiver for this regulation purpose; however, it increases system complexity and decreases power efficiency. This paper proposes a new single stage topology that can achieve output voltage regulation as well as resonant frequency tracking. By combining asymmetric pulse width modulation scheme with a buck-boost converter, the output voltage is regulated by duty cycle control and the energy link variation can be compensated by frequency control, which is suitable for the wireless power transfer system in practical user scenario. Furthermore, as the proposed circuit uses only two additional components, the transmitter circuit is compact. For verification, the proposed circuit has been tested by a 50W prototype hardware.**

Keywords—DC-DC converter, wireless power transfer, PWM control, frequency control

I. INTRODUCTION

Recently, wireless power transfer technology is becoming attractive in wearable devices and e-vehicles. Having a cost effectiveness of manufacturing, capacitive power transfer technology is actively researched [1]. Capacitive power transfer (CPT) utilizes the capacitance between the two parallel plates and the transmitter circuit generates high frequency displacement current through the energy link structure. To increase the power transferability, the capacitive reactance should be canceled out by inductive matching network to drive circuit near resonant frequency and increase the power factor of the circuit [2],[3]. However, when the link capacitor is misaligned, the resonant frequency of the system shifts due to the varying link capacitance as shown in Fig 1. Thus, it is necessary to adjust the operating frequency to compensate the variation of capacitance. Therefore, it is clear that conventional frequency control methods for CPT system [4], [5] are not enough to regulate output voltage when misalignment occurs as above. In other words, in order to consider both the misalignment of the link capacitor and the load change in the CPT system, there is a need for a method capable of both the resonant frequency tracking and the output voltage regulation.

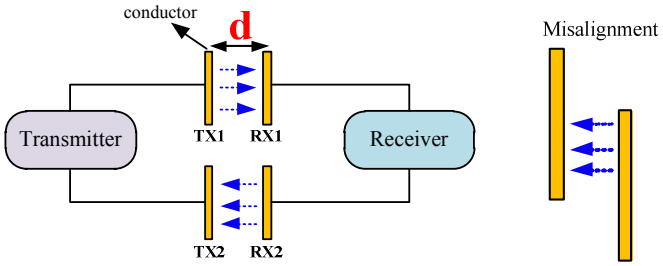


Fig. 1. Change in link capacitance due to misalignment

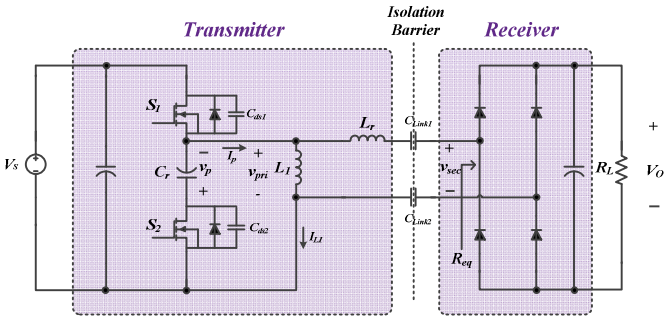


Fig. 2. Proposed topology

In this paper, a new half-bridge structure incorporating buck-boost is proposed as shown in Fig. 1 in order to mitigate this problem. The output voltage can be regulated by the duty ratio control and the resonance frequency tracking control maximizes the power transferability even in a link capacitance change. The proposed structure provides zero-voltage-switching (ZVS) condition in the entire duty ratio range by the parallel inductance (L_1), and link capacitance are canceled out by the series resonant inductance (L_r). Furthermore, with an integrated transformer, L_1 and L_r can be merged into a single magnetic component, which simplifies the circuit parts for the wireless power transfer. In this paper, the operating principle is presented with theoretical mode analysis, and feasibility of the idea is proved by a 50W prototype hardware test.

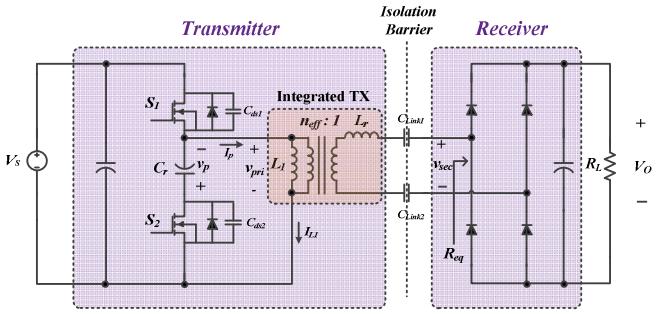


Fig. 3. Proposed topology with an integrated transformer

II. PROPOSED TOPOLOGY

Figure 2 shows the proposed topology, where two active switches, S1 and S2, are driven by asymmetrical pulse-width-modulated (APWM) gating pulses, and the floating capacitor Cr together with the parallel inductor L_1 forms a buck-boost configuration[6]. The duty ratio of S_2 is gated complementary to S_1 with a dead time to prevent shoot through of the switches.

Figure 3 shows another representation of the proposed circuit, where two inductors are configured as a single integrated transformer, where L_1 is used to drive the system in ZVS condition and L_r resonates with link capacitors as shown in (1). The integrated transformer has the advantage of simplifying the transmitter, and the values of the inductors L_1 and L_r are derived from (2) and (3) respectively.

$$f_{sw} = f_o = \frac{1}{2\pi\sqrt{L_r(C_{link1} \parallel C_{link2})}} \tag{1}$$

$$L_1 = \frac{L_m}{k^2} \tag{2}$$

$$L_r = (1 - k^2)L_2 \tag{3}$$

where L_m is the transformer magnetizing inductance and L_2 is the secondary side self-inductance of the transformer.

Figure 4 shows steady-state operating waveforms. Here, the average value of the floating capacitor voltage V_p is expressed by (4) and the output voltage is thus given as (5) by fundamental harmonic approximation.

$$V_p = \frac{D}{1 - D} V_s \tag{4}$$

$$V_o = \frac{8V_p \sin(\pi D)}{n_{eff}\pi^2} \tag{5}$$

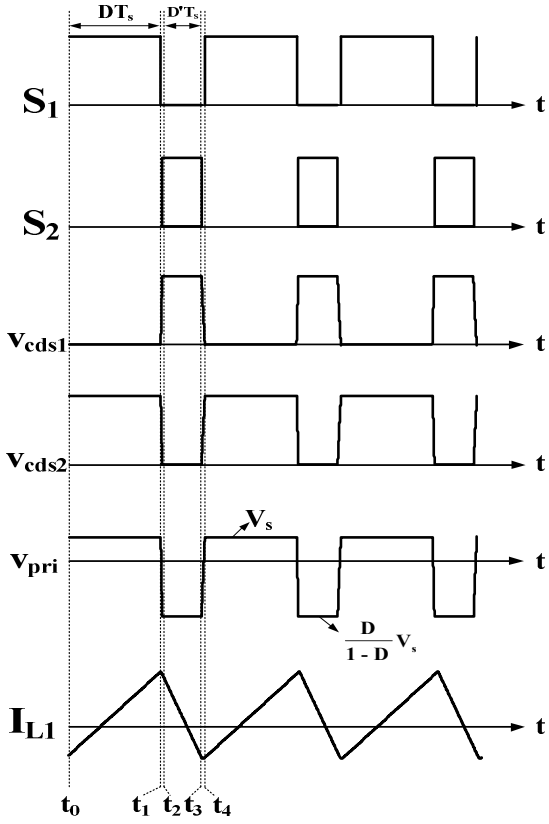


Fig. 4. Steady-state waveform (D>0.5)

$$n_{eff} = \frac{kN_p}{N_s} \tag{6}$$

Where n_{eff} is the effective turn ratio of the integrated transformer, N_p and N_s are the number of primary and secondary turns, respectively, and k is the transformer coupling coefficient. Since buck-boost converter and half bridge [7] are merged together, it is clear that the output voltage can be regulated directly by change the duty ratio of S_1.

The operation analysis for each time interval in Fig. 4 is as follows.

Mode 1 [$t_0 < t < t_1$]: Mode 1 starts when the switch S_1 is turned ON while the switch S_2 is OFF. The current of L_1 is expressed by (7), and the drain-to-source voltage of switch S_2 is equal to (8), and the primary voltage v_{pri} is the same as the input voltage V_s.

$$i_{L1}(t) = \frac{V_s}{L_1}(t - t_0) + i_{L1}(t_0) \tag{7}$$

$$V_{cds2} = \frac{V_s}{1 - D} \tag{8}$$

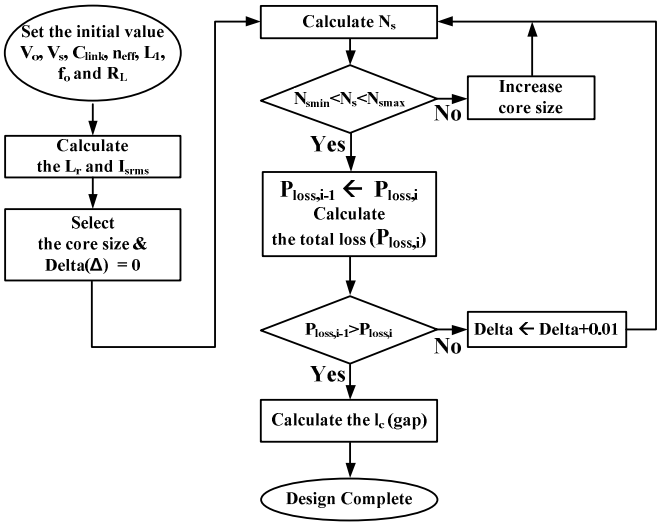


Fig. 5. Integrated transformer design procedure

Mode 2 [t_1 < t <t_2]: Mode 2 starts when the switch S_1 is turned OFF while the switch S_2 is still OFF. The energy stored in the inductor L_1 is used to remove the voltage on the parasitic output capacitor of S_2, C_{ds2}, which makes the ZVS possible. Meanwhile, v_{pri} and i_{L1} are given by (9) and (10), respectively.

$$v_{pri}(t) = V_{cds2}(t_1)\cos\frac{1}{\sqrt{2}}\omega_r(t - t_1) + \frac{i_{L1}(t_1)}{\sqrt{2}Z_o}\sin\frac{1}{\sqrt{2}}\omega_r(t - t_1) - V_p \quad (9)$$

$$i_{L1}(t) = i_{L1}(t_1)\cos\frac{1}{\sqrt{2}}\omega_r(t - t_1) + \sqrt{2}Z_o v_{pri}(t_1)\sin\frac{1}{\sqrt{2}}\omega_r(t - t_1) \quad (10)$$

where Z_o and ω_r are represented by the resonance characteristic between L_1 and C_{ds2} as

$$Z_o = \sqrt{\frac{C_{ds2}}{L_1}}, \quad (11)$$

$$\omega_r = \sqrt{\frac{1}{L_1 C_{ds2}}}. \quad (12)$$

Mode 3 [t_2 < t <t_3]: Mode 3 starts when the switch S_2 is turned ON while the switch S_1 is OFF. Before turning on S_2, the drain-to-source voltage has already been discharged to zero by the mode 2 operation, S_2 turns ON in ZVS condition, and the current flowing in L_1 is as follows.

$$i_{L1}(t) = -\frac{V_p}{L_1}(t - t_2) + i_{L1}(t_2) \quad (13)$$

Mode 4 [t_3 < t <t4]: Mode 4 starts when the switch S_2 is turned OFF while S_1 is OFF. In this state, the energy stored in the inductor L_1 is used to remove the energy of the parasitic output capacitor of S_1. The v_{pri} voltage is given by (14) and the i_{L1} current is given by (15).

$$v_{pri}(t) = V_{cds2}(t_3)\cos\frac{1}{\sqrt{2}}\omega_r(t - t_3) + \frac{i_{L1}(t_3)}{\sqrt{2}Z_o}\sin\frac{1}{\sqrt{2}}\omega_r(t - t_3) - V_p \quad (14)$$

$$i_{L1}(t) = i_{L1}(t_3)\cos\frac{1}{\sqrt{2}}\omega_r(t - t_3) + \sqrt{2}Z_o v_{pri}(t_3)\sin\frac{1}{\sqrt{2}}\omega_r(t - t_3) \quad (15)$$

From the operational analysis given above, the component design procedure can be derived. The parallel inductance L_1 must be selected to meet the ZVS condition. By the analysis of the ZVS condition, the value of L_1 should be designed within the range of (16).

$$L_1 \le \frac{D(1 - D)T_{dead}}{4f_{sw}(C_{ds1} + C_{ds2})} \quad (16)$$

After selecting the L_1 value, the C_r value is selected according to (17). The design method of the integrated transformer used in this paper is shown in Fig. 5 and is based on the previous researches in [8]-[10].

$$\frac{1}{2\pi\sqrt{C_r L_1}} << f_o \quad (17)$$

III. Proposed Dual-mode Contorl Scheme

In practical applications of wireless power transfer systems, resonant link capacitance cannot always be perfectly aligned. In order to maintain the transferability even when the link capacitance becomes smaller than the perfectly aligned condition due to the misalignment between the transmitter and the receiver, frequency control is required to compensate for the increased resonant frequency and the operating frequency should be adjusted to be above the resonant frequency to achieve ZVS condition of the main inverter switches. In this case, because the output voltage is strongly dependent on the load resistance, it should be regulated by additional control method other than frequency control, such as primary dc link adjustment by front-end converter or secondary dc voltage regulation by receiver-side converter, all of which increases the system complexity and degrade the overall power efficiency of the system. Furthermore, the output voltage should be sensed across the isolation barrier, which sometimes requires wireless data communication to send the information back to the primary side. The proposed topology has the advantage of satisfying the ZVS condition even at the resonant frequency. Thusly it is possible that the output voltage is independent of the load resistance and can be estimated through the

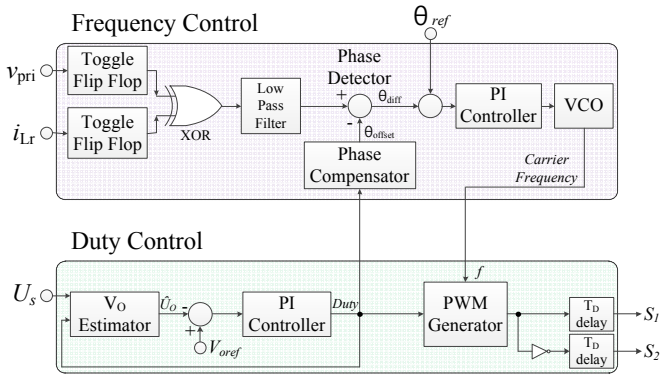


Fig. 6. Dual-mode control scheme

information on the primary side by Eqs. (4) and (5). It means that both frequency control and duty control can be applied simultaneously and independently. To maximally utilize the features, this paper also proposes dual-mode control, where frequency control only tracks the resonant frequency shift and duty control is dedicated to the output voltage regulation.

Figure 6 is the dual-mode control block diagram. The frequency control section controls the operating frequency through the phase-locked loop (PLL) using the phase difference between the primary voltage, v_{pri} and the inductor current, i_{Lr} of the resonant circuit. The PI (proportional integral) controller operates so that the phase difference, Θ_{diff} between the primary voltage and the inductor current becomes zero to tracks the resonant frequency, where the controlled frequency is that the output of the voltage-controlled oscillator (VCO). The additional blocks like two toggle flip-flops and the phase compensator are used for eliminating possible malfunction of PLL block, which may occur when the two input waveforms are asymmetric.

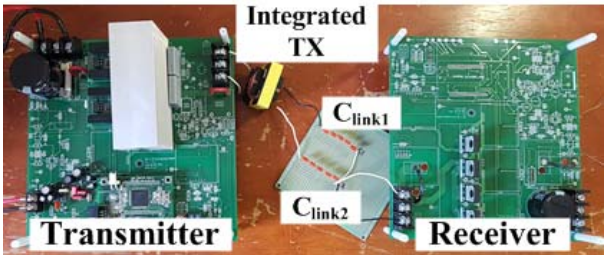
Meanwhile, the duty control section utilizes the dc input voltage of the inverter and the carrier frequency generated from the frequency control blocks. The V_o estimator implements Eq. (5), and the output is regulated by the additional PI controller. The output of the controller and the carrier frequency generate the PWM gate signal, and the TD delay blocks provide the dead time for ZVS operation of the main inverter switches.

IV. Verification of the Proposed Topology

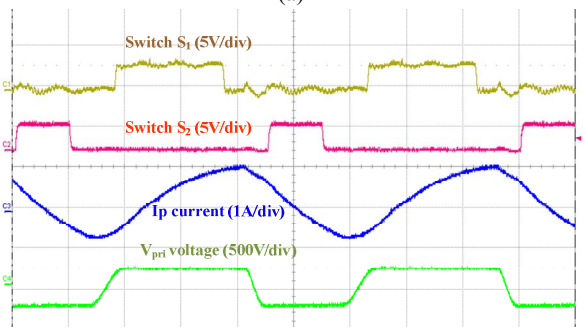
To verify the feasibility of the proposed topology, a prototype system was designed and implemented with the proposed scheme in Fig. 3 The target specifications are Po=50W, R_L=200Ω(100V/0.5A), Clink 1, 2=2nF, and V_s= 180V. Fig. 7(a) shows a photograph of the prototype hardware. Instead of a capacitive link structure, two film capacitor banks with C_{link1}=2.13nF and C_{link2}=2.08nF have been formed. For the integrated transformer, an EI4035S core was chosen. Table 1 shows the transformer design specifications and measurement results of the integrated transformer. The transformer parameters were measured with an LCR meter (Agilent 4263B). For the half-bridge inverter and the full-wave rectifier, MOSFET (Cree, C3M0065090D) and diode (Cree, C3D16060D) were adopted, respectively. Fig. 7(b) shows the hardware waveforms, which show that two switches are

TABLE I
Design Spec. & Measurement Results
of the Integrated Transformer

design specification	
core type	EI4035S
effective turn ratio (n_{eff})	1.5
# of turns (pri.)	80
# of turns (sec.)	54
winding separation(s_w)	3mm
core gap (l_c)	11mm
wire size (pri. & sec.)	0.08/40 litz
relative permeability	2400 (PL-7)
measurement results	
resonant inductor(L_r)	175.02uH
magnetizing inductor(L_1)	126.6uH
effective turn ratio (n_{eff})	1.78



(a)



(b)

Fig. 7. Experimental results
(a) photograph of the hardware
(b) hardware waveforms (500ns/div)

operating in ZVS operation. The switching frequency is 446KHz, the output voltage is controlled to 100V by duty control, and the output power is 50W with the system overall efficiency of 87.7%.

V. Conclusion

This paper proposes a new dually controllable drive topology for capacitive wireless power transmission. It has the advantage that the output voltage can be regulated by adjusting the duty ratio with the operating frequency automatically tune to the resonant frequency, so power transferability is maintained even with variations in separation or alignment of the energy link structures. Furthermore, the output voltage regulation is achieved through the primary input voltage sensing, which removes the circuitry required for feedback sensing across an isolation barrier in wireless power system. It is expected that such a single stage structure will further contribute to simplification and miniaturization of the overall

wireless power system because it can eliminate extra dc/dc converter for dc link control. The operation of the proposed topology has been verified with a 50W hardware with duty cycle control. In the subsequent work, the fully working dual-mode control will be incorporated into the hardware.

REFERENCES

[1] L. Huang, A.P. Hu, A. Swain, “A Resonant Compensation Method for Improving the Performance of Capacitively Coupled Power Transfer,” IEEE Energy Conversion Congress and Exposition (ECCE), pp. 870-875, 2014.

[2] F. Lu, H. Zhang, H. Hofmann and C. Mi, "A Double-Sided LCLC-Compensated Capacitive Power Transfer System for Electric Vehicle Charging," in IEEE Transactions on Power Electronics, vol. 30, no. 11, pp. 6011-6014, Nov. 2015.

[3] B. Luo, R. Mai, Y. Chen, Y. Zhang and Z. He, "A voltage stress optimization method of capacitive power transfer charging system," 2017 IEEE Applied Power Electronics Conference and Exposition (APEC), Tampa, FL, USA, 2017, pp. 1456-1461.

[4] H. S. Choi, J. Y. Park and S. J. Choi, "Analysis and control of capacitive-coupled wireless power transmission system," 2015 15th International Conference on Control, Automation and Systems (ICCAS), Busan, 2015, pp. 1005-1009.

[5] P. Si, A. P. Hu, S. Malpas and D. Budgett, "A Frequency Control Method for Regulating Wireless Power to Implantable Devices," in IEEE Transactions on Biomedical Circuits and Systems, vol. 2, no. 1, pp. 22-29, March 2008.

[6] Myeong-Hwan, Yu (2006). "A New Piezoelectric Transformer Driving Topology for Universal Input PWM Control AC/DC Adapter", Master's Thesis, Seoul National University, Seoul, Korea 75pages.

[7] I. H. Cho, Y. D. Kim and G. W. Moon, "A Half-Bridge LLC Resonant Converter Adopting Boost PWM Control Scheme for Hold-Up State Operation," in IEEE Transactions on Power Electronics, vol. 29, no. 2, pp. 841-850, Feb. 2014.

[8] Ray Ridley, “Magnetics Core Losses,” APEC Industry session on Magnetics, Mar. 2016.

[9] S. De Simone, C. Adragna and C. Spini, “Design Guideline for Magnetic Integration in LLC Resonant Converters,” International Symposium on Power Electronics, pp.950-957, 2008.

[10] Xi Nan and C. R. Sullivan, “An Improved Calculation of Proximity-Effect Loss in High-Frequency Winding of Round Conductors,” IEEE PESC, vol. 2, pp. 853-860, June 2003.