Energy Conversion
Circuit Laboratory

Novel Battery Interface Converter with Bi-directional Current Flow utilizing Partial Power Processing

Seok Jin Jeong[1], Ngyuen-Anh Nguyen[2], Mwangi Andrew Ngini[3], Sung-Jin Choi[4]*
Dept. of Electrical, Electronic and Computer Engineering
University of Ulsan, Ulsan, South Korea
[1]hotbreak64@mail.ulsan.ac.kr [2]nnanh1995@gmail.com [3]nginiandrew79@gmail.com [4]sjchoi@ulsan.ac.kr

***Abstract*—This paper introduces a novel battery charging system utilizing a Partial Power Processing (PPP) converter to enhance system efficiency and reduce the power processed by the converter. Unlike the conventional full power processing methods, the proposed topology—combining a half-bridge on the primary side and a push-pull on the secondary side—processes only a fraction of the system power, enabling bidirectional power flow for both step-up (charging) and step-down (discharging) modes for various applications. A 2.5 kW prototype converter for a 25kWh battery was designed and simulated to validate the approach. Simulation results demonstrate system efficiency exceeding 99.5%, with the converter operating at an efficiency around 95%.**

***Index Terms*—Partial Power Processing, Battery application, Converters, Simulation, Bidirectional Power Flow**

I. Introduction

Lithium-ion batteries are crucial for powering a wide range of portable or mobile devices, from smartphones to electric vehicles (EVs), and can store surplus energy from the power grid or electrified transportation systems during operation. Also, power sharing between batteries of different devices is utilized in applications such as smartphones. Thus, high-voltage and high-power applications necessitate consideration of the efficiency, reliability, scalability, and safety of DC-DC converters.

In battery-powered applications, the battery undergoes repeated charging and discharging cycles to sustain system functionality. During this process, DC-DC converters are essential to prevent battery from over-charging and over-discharging. Over the years, numerous studies have been carried out in various domains to address these issues. For instance, a 1MW DC-DC converter is required to interface with a 1MWh battery system for an electric propulsion vessel [1] or 500kW bi-directional DC-DC converter for battery energy storage system is studied for railway DC feeder system in [2]. In large-scale systems, employing a single converter to handle the entire power demand can lead to significant challenges in terms of efficiency, reliability, and thermal management, primarily due to the increased size of the converter. To overcome these limitations, multi-module converter systems—where multiple converters share the power processing load—have been actively investigated. In [3], a multi-module system consisting of eight converters was implemented to configure a 200 kW converter system for an ultrafast EV charger. Additionally, in [4], a modular multilevel cascade converter with a 500 kW rating was developed for battery energy storage systems (BESS). Multi-level converter-based systems also share similar challenges with single converter systems in large-scale applications, since the total converter capacity equals the system capacity.

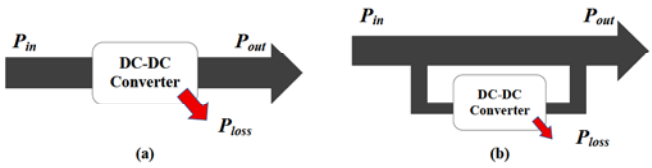

Fig. 1. Comparison of two power processing methods: (a) Full Power Processing, (b) Partial Power Processing

To alleviate this burden, by Partial Power Processing (PPP), it is possible to reduce the power handled by the converter relative to the total power processed by the system. PPP refers to a method where the converter processes only a fraction of the total system power, with the remaining current flowing through a bypass path [5]. For simplicity, we refer to the traditional power processing method as Full Power Processing (FPP). As illustrated in Fig. 1, since power loss occurs only in the portion of the power processed by the converter, the overall system experiences reduced power loss, and the converter volume can also be reduced compared to a FPP system. Numerous studies have been carried out to enable the application of PPP in a wide range of systems such as PV generation [6], EV charging station [7], Energy Storage System(ESS) [8], etc.

In this paper, a battery-interfacing converter utilizing Partial Power Processing (PPP) and its design in terms of size and efficiency is investigated. The remainder of this paper is organized as follows. Section II introduces the system consideration of

This research was supported by the Ministry of Trade, Industry & Energy (MOTIE), Korea Institute for Advancement of Technology (KIAT) through the Encouragement Program for The Innovation Cluster Development of Region (P0025291) and the National Research Foundation of Korea (NRF) grant funded by the Korea government (MSIT) (RS-2023-00240194).

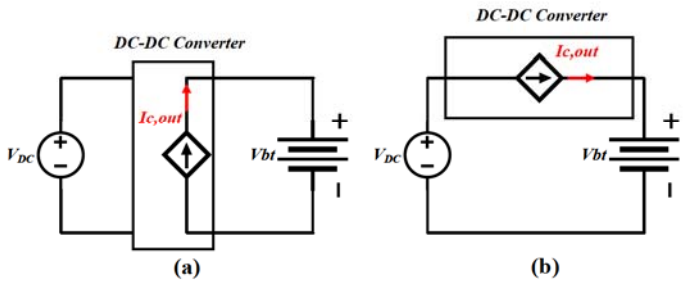

Fig. 2. Battery charging method: (a) conventional method, (b) proposed method

Partial Power Processing. Section III presents the analysis of the converter topologies and operating modes for the PPP. Section IV provides simulation results and discussion. Finally, Section V concludes this paper.

II. System Analysis for Partial Power Processing

A. Converter Size and Efficiency Consideration

Figure 2 illustares two different battery charging method, Fig. 2(a) is the conventional way (FPP) and Fig. 2(b) is proposed method (PPP). In both cases, the battery is charged with the same power as (1).

$$P_{bt} = V_{bt} \cdot I_{c,out} \tag{1}$$

From the perspective of converter output power, in the conventional charging method, the voltage applied to the converter is equal to the battery voltage, thus the converter output power capacity is given by (2).

$$P_{c,out(FPP)} = V_{bt} \cdot I_{c,out} \tag{2}$$

By the way, in the case of Fig. 2(b), the voltage applied to the converter is equal to the difference between the DC input voltage and the battery voltage, and thus the converter output power capacity is given as (3).

$$P_{c,out(PPP)} = (V_{DC} - V_{bt}) \cdot I_{c,out} \tag{3}$$

By comparing (2) and (3), it is expected that applying PPP makes it possible to reduce the power handling capacity of the converter under the same charging condition.

In a PPP structure, the converter's processed power ratio (K_p), which can serve as a performance parameter, is defined in this paper as

$$K_p = \frac{P_{c,out}}{P_{s,out}} \tag{4}$$

where $P_{c,out}$ is the converter output power and $P_{s,out}$ is the system output power.

Within the PPP, losses occur only for the power processed by the converter. Therefore, the system efficiency η_s can be derived as shown in the following equation.

$$\eta_s = \frac{P_{s,out}}{P_{s,in}} = \frac{P_{s,out}}{P_{c,in} + P_{s,bypass}} \tag{5}$$

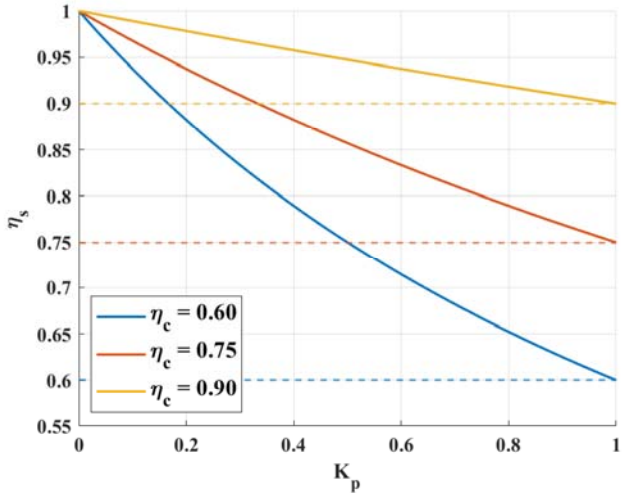

Fig. 3. Variation of η_s as a function of K_p

In the above equation, $P_{c,in}$ denotes the converter input power, while $P_{s,bypass}$ represent the system power not processed by the converter. By expressing each term with respect to the $P_{s,out}$, it can be rewritten as follows.

$$P_{s,bypass} = \frac{(1 - K_p) \cdot P_{s,out}}{\eta_{bypass}} \approx (1 - K_p) \cdot P_{s,out} \tag{6}$$

$$P_{c,in} = \frac{K_p \cdot P_{s,out}}{\eta_c} \tag{7}$$

It can be considered that $P_{s,bypass}$ is the system power processed by a dummy converter, which efficiency is almost 1. By substituting (6) and (7) into (5), (8) can be derived.

$$\eta_s = \frac{\eta_c}{(1 - K_p)\eta_c + K_p} \tag{8}$$

where η_c is the converter efficiency and η_s is the system efficiency. Fig. 3 illustrates the variation in system efficiency as a function of K_p.

The downsizing of the converter using the PPP approach can be un derstood through the following analysis. When the converter operates in constant current control mode, considering the variation in battery voltage, the maximum power in the Full Power Processing (FPP) configuration occurs when the battery is fully charged, as expressed by the (9).

$$P_{c,out(FPP),max} = V_{bt,max} \cdot I_{c,out} \tag{9}$$

In contrast, in the PPP configuration, the maximum power occurs when the battery state of charge is at its minimum, and it can be expressed as in (10).

$$P_{c,out(PPP),max} = (V_{DC} - V_{bt,min}) \cdot I_{c,out} \tag{10}$$

If the value given by (9) is greater than that of (10), it indicates that the converter capacity can be reduced using PPP compared to FPP. Therefore, downsizing the converter through PPP is valid when K_p satisfies the following condition.

$$\frac{1}{1 + \alpha} > K_p \tag{11}$$

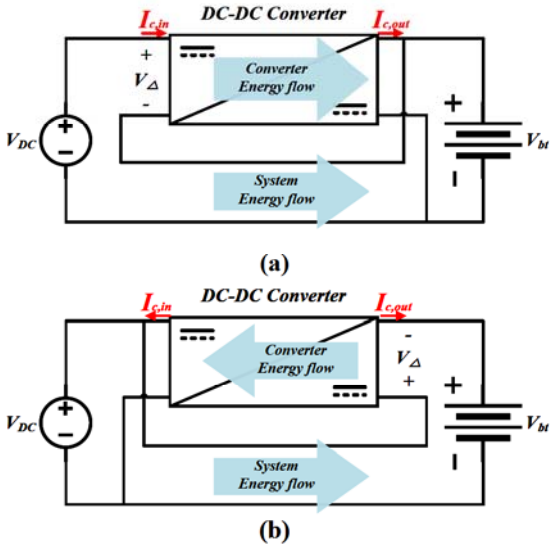

Fig. 4. PPP Configurations during battery charging operation: (a) ISOP structure, (b) IPOS structure.

Here, α denotes the ratio of the maximum to the minimum battery voltage during operation, and it is defined as follows:

$$\alpha = \frac{V_{bt,min}}{V_{bt,max}}. \tag{12}$$

As an example, consider a Li-ion battery cell whose voltage ranges from 2.5 V to 4.2 V. According to (11), converter downsizing becomes feasible when $K_p < 0.63$, which corresponds to the operating region where $V_{DC} \leq 6.76\,\text{V}$. Based on (8), it is observed that if K_p is less than 1, η_s is higher than η_c. Thus, the PPP concept is an effective solution for downsizing converter and improving system efficiency.

B. PPP Configuration

According to [5], the PPP configuration is seperated into two: Input-Parallel Output-Series (IPOS) and Input-Series Output-Parallel (ISOP). Same as in Fig. 2, the DC bus is connected to the input of the converter, and the battery is connected to its output. Each configuration can be represented as shown in Fig. 4.

In each configuration, the direction of power flow in both the system and the converter is illustrated in Fig. 4. Under the assumption that V_{DC} is always greater than V_{bt}, the input voltage polarities of the ISOP and IPOS converters must be opposite to satisfy this condition. Consequently, while the power flow direction of the converter aligns with that of the system in the ISOP configuration, it is reversed in the IPOS configuration. Therefore, the ISOP configuration exhibits a positive K_p, whereas the IPOS configuration has a negative K_p.

Various implementations of the IPOS and ISOP configurations are reviewed in [12]. To compare the performance of each configuration, the static voltage gain of the system, G_v, can be used, as demonstrated in [13]:

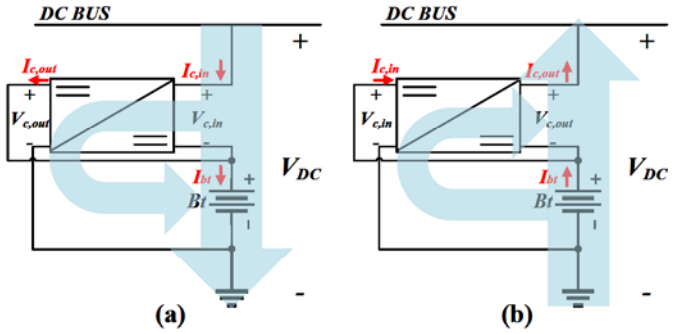

Fig. 5. Battery charging and discharging system based on Partial Power Processing (PPP): (a) power flow during charging, (b) power flow during discharging

$$G_v = \frac{V_{bt}}{V_{DC}} \tag{13}$$

In this paper, it is assumed that G_v is always less than 1. According to [12], when the voltage gain G_v is low, the ISOP configuration is more commonly employed. Compared to the IPOS configuration under the same condition, ISOP can achieve a lower K_p, making it more advantageous for maintaining high system efficiency. Therefore, the ISOP structure shown in Fig. 4(a) is adopted in this study.

C. Operating Modes

This converter operates in charging and discharging modes. Fig. 5(b) illustrates the power flow direction in charging mode, where the input voltage of the converter ($V_{c,in}$) is derived as follows:

$$V_{c,in} = V_{DC} - V_{bt} \tag{14}$$

The converter supports bidirectional power flow, charging and discharging modes. The power flow during charging is illustrated in Fig. 5(a). The input voltage of converter is $V_{c,in}$ and output is V_{bt}. It can be seen from (14) that V_{bt} is greater than $V_{c,in}$. Therefore, the converter operates in step-up mode during the charging process. When the voltage described in (14) is applied to the converter, it regulates the output current amplitude according to a predefined reference. The total current applied to the battery is derived as

$$I_{bt} = I_{c,out} + I_{c,in} \tag{15}$$

where $I_{c,out}$ is the current from the converter's primary side, and $I_{c,in}$ is the current into the converter's secondary side, which is equal to the DC bus current. Hence, the converter efficiency during charging is calculated using (14) and (15), and is given by:

$$\eta_{c,charge} = \frac{P_{c,out}}{P_{c,in}} = \frac{V_{bt} \cdot I_{c,out}}{V_{c,in} \cdot I_{c,in}} \tag{16}$$

During discharging, the power flow is reversed relative to the charging mode, as illustrated in Fig. 5(b). In this case, since the converter input voltage ($V_{c,in} = V_{bt}$) is usually designed

TABLE I
COMPARISON OF TWO TOPOLOGIES

Category	Topology	
	DAB	*HB-PP*
Inductor	1	2
Capacitor	2	3
Transformer	1	1
Switching Component	8	4
Voltage Stress (Primary switch)	100%	100%
Voltage Stress (Secondary switch)	100%	200%
Current Stress (Primary switch)	100%	200%
Current Stress (Secondary switch)	100%	100%

to be higher than the output voltage ($V_{c,out}$), the converter operates in step-down mode. Following a similar approach to (14), (15), and (16), the corresponding expressions for voltage, current, and efficiency during discharge can be derived as:

$$V_{c,out} = V_{DC} - V_{bt} \tag{17}$$

$$\eta_{c,discharge} = \frac{V_{c,out} \cdot I_{c,out}}{V_{bt} \cdot I_{c,in}} \tag{18}$$

III. Proposed Topology and Mode of Operation Analysis

A. Power stage topology consideration

In the proposed PPP structure mentioned in Section II, the one side of the converter voltage is fixed to V_{bt} and the voltage applied to the converter is determined by the difference between the DC bus voltage and the battery voltage, ranging from $V_{\Delta,min}$ to $V_{\Delta,max}$, defined as:

$$V_{\Delta,min} = V_{DC} - V_{bt,max} \tag{19}$$

$$V_{\Delta,max} = V_{DC} - V_{bt,min}. \tag{20}$$

The maximum voltage gain required by the converter in both the FPP and PPP approaches can be expressed as follows.

$$M_{v(FPP),max} = \frac{V_s}{V_p} = \frac{V_{DC}}{V_{bt,min}} \tag{21}$$

$$M_{v(PPP),max} = \frac{V_s}{V_p} = \frac{V_{DC} - V_{bt,min}}{V_{bt,min}} = M_{v(FPP),max} - 1 \tag{22}$$

By comparison, it is confirmed that the converter in the PPP requires a wider voltage gain than in the FPP.

Therefore, achieving PPP operation for battery interfacing system imposes several requirements on the converter, 1) including a high input-output voltage ratio, 2) bidirectional power flow capability, and 3) a wide control range to meet the battery voltage variation. To meet these requirements, converter topologies such as the Dual Active Bridge (DAB) and Half-Bridge Push-Pull (HB-PP) can be considered. Although a bidirectional flyback converter can also be considered, it is primarily used in applications at the few-hundred-watt level, and is therefore not suitable for the current application. Two converter topologies are presented in Fig 6 and compared in Table I. According to the comparison, HB-PP topology can reduce the number of switcing components by half compared to DAB and is superiorfor low primary voltage and high secondary output application. Based on that point, HB-PP topology is considered in this paper.

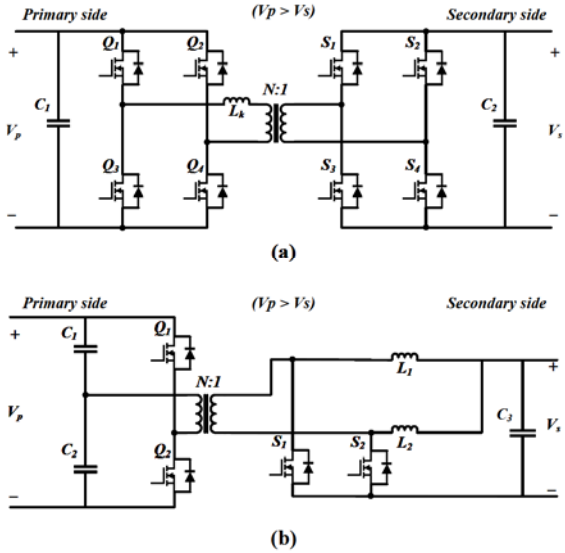

Fig. 6. Proposed topology and applications: (a) Dual Active Bridge (DAB), (b) Half-Bridge Push-Pull (HB-PP)

B. Operating Mode Analysis

In the HB-PP converter in Fig. 6(b), half-bridge side is connected to the battery, while the push-pull side is connected across the voltage difference between the DC bus and the battery (V_Δ). For convenience, the half-bridge side is referred to as the primary side and the push-pull as the secondary side. By placing dual inductor in the push-pull side, a reduction of current ripple is achieved [9]. The topology is driven by a combination of four switching pulses, and the overall operation consists of a total of four time intervals. In each time interval, only two switches are simultaneously turned on. The equivalent circuit of the proposed topology is presented in Fig. 7, switching pulses and the corresponding voltage and current waveforms for each interval are shown in Fig. 8. The operation of the converter can be separated into step-down mode and step-up mode. However, the following operation mode analysis applied to both mode of operations. In the step-up mode, L_1 and L_2 are connected to the input side and function as boost inductors, whereas in the step-down mode, the inductors are connected to the output side. This distinction characterizes the mode of operation. The reference directions of voltage and current are defined based on the buck mode operation, following the passive sign convention.

1) Interval 1 $[t_0, t_1]$*:* At $t = t_0$, Q_1 and S_1 are turned on. Therefore, the voltage applied to the primary winding of the transformer is

$$V_P = -\frac{V_{bt}}{2}. \tag{23}$$

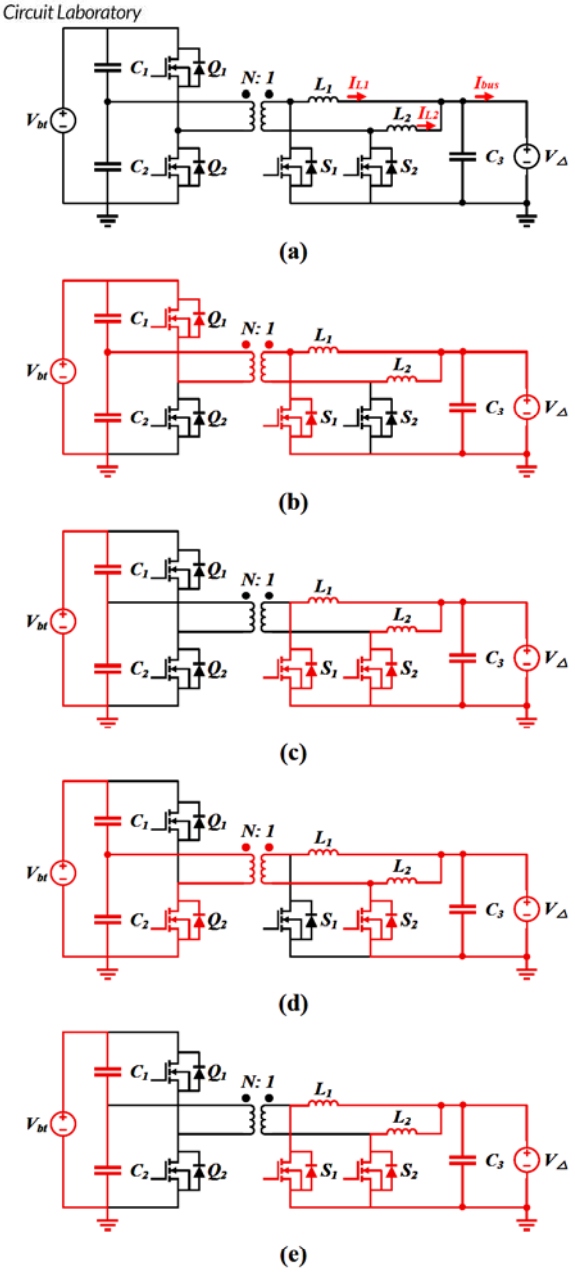

Fig. 7. Operation analysis of the proposed topology: (a) Equivalent circuit, (b) Interval 1 ($t_0 \sim t_1$), (c) Interval 2 ($t_1 \sim t_2$), (d) Interval 3 ($t_2 \sim t_3$), (e) Interval 4 ($t_3 \sim t_4$).

The voltage of each inductor can be expressed as

$$V_{L1} = -V_\Delta \tag{24}$$

$$V_{L2} = \frac{V_{bt}}{2N} - V_\Delta. \tag{25}$$

In step-down mode, L_1 is connected to the V_Δ through S_1 and releases its stored energy, while L_2 is connected to C_1 and stores energy from the V_{bt}.

In step-up mode, in contrast, L_1 stores energy through S_1 and L_2 releases the energy to V_{bt}.

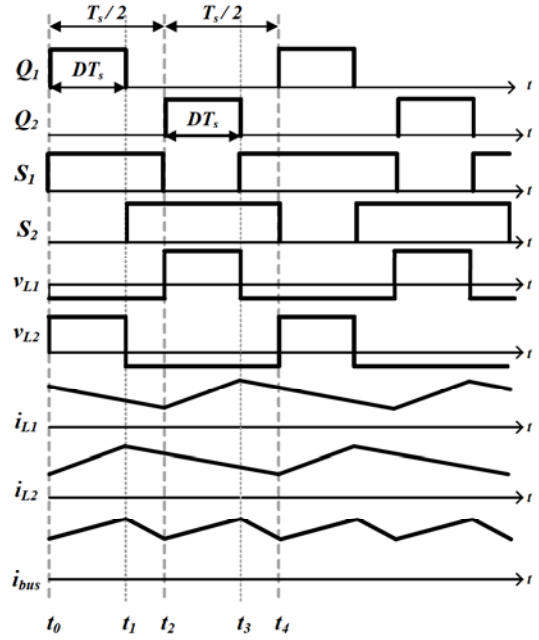

Fig. 8. Switching voltage and current waveforms of the HB-PP topology in step-down mode.

2) Interval 2 $[t_1, t_2]$*:* At $t = t_1$, Q_1 is turned off to ensure the deadtime for the half-bridge, S_2 is turned on while keeping S_1 on. In other words, both push-pull side switches are turned on. Therefore, the voltage of L_1 and L_2 are discharged by V_Δ as follows.

$$V_{L1} = V_{L2} = -V_\Delta \tag{26}$$

There is no power flow between the primary and secondary side via the transformer, during this interval.

3) Interval 3 $[t_2, t_3]$*:* At $t = t_2$, S_1 is turned off while Q_2 and S_2 are turned on. The operation in Interval 1 and Interval 3 are similar and thus the following holds.

$$V_P = \frac{V_{bt}}{2}. \tag{27}$$

$$V_{L1} = \frac{V_{bt}}{2N} - V_\Delta \tag{28}$$

$$V_{L2} = -V_\Delta \tag{29}$$

In step-down mode, L_1 and C_2 are connected by transformer, the power starts to flow from the primary side to the secondary side. Therefore, L_1 stores energy and i_{L1} increases. Similar as L_1 in Interval 1, L_2 releases energy to V_Δ .

In the step-up mode, L_1 releases energy to the primary side of the transformer, and C_2 is charged, C_1 is discharged by the reflected current i_{L1} on the primary side. In this mode, L_2 stores energy through S_2.

4) Interval 4 $[t_3, t_4]$*:* At $t = t_3$, Q_2 is turned off to the deadtime for the half-bridge and S_1 is turned on while keeping S_2 on and it operates in the similar way as Interval 2.

$$V_{L1} = V_{L2} = -V_\Delta \tag{30}$$

TABLE II
SIMULATION PARAMETERS

Parameter	Value	Description
V_{DC}	400 V	DC bus voltage
$V_{bt,min}$	360 V	Minimum Battery voltage
$V_{bt,max}$	380 V	Maximum Battery voltage
P_s	25 kW	System power
P_c	2.5 kW	Maximum Converter power
K_p	0.1	Power ratio
L_1, L_2	200 μH	Inductor
C_1, C_2	30 μF	Half bridge Capacitor
C_3	6 μF	Push Pull Filter Capacitor
f_s	100 kHz	Switching frequency
N	1.4:1	Transformer turn ratio
I_{bus}	62.5 A	Average DC bus current
I_L	31.25 A	Average inductor current
Δi_{bus}	2%	Maximum DC bus current ripple
$Q_{1,2}$	-	IMZC120R012M2H
$S_{1,2}$	-	IMW65R007M2H

Both inductors are to store energy in step-up mode operation, and release energy in step-down mode operation during this time interval.

C. Design Procedure

The voltage gain of the step-up mode is obtained by applying voltage-second balance to the inductors.

$$M_v = \frac{V_{bt}}{V_{c,in}} = \frac{2N}{D} \tag{31}$$

L_1, L_2 are calculated by the inductor ripple current specification:

$$L_{1,2} = \frac{\frac{V_{bt}}{2N} - 2V_{\Delta}}{\Delta i_{bus}} DT_s \tag{32}$$

The values of the half-bridge filter capacitors, C_1 and C_2, are calculated under step-up mode operation of the converter while the push-pull filter capacitor C_3 is calculaed at step-down mode operation by the capacitor voltage ripple specifications, as follows.

$$C_{1,2} = \frac{DT_s \cdot i_{bus}}{4N \cdot \Delta v_{c1,c2}} \tag{33}$$

$$C_3 = \frac{(1-D)D}{16NL \cdot \Delta v_{c3}} v_{bt} T_s^2 \tag{34}$$

Δi_L denotes the current ripple of inductors L_1 and L_2, where $\Delta v_{c1,c2}$ and Δv_{c3} represent the voltage ripple of the capacitors C_1, C_2, and C_3, respectively and I_{bus} is total current of push-pull side, which is described as

$$i_{bus} = i_{L1} + i_{L2} + i_{C3}. \tag{35}$$

Considering the variation in the battery voltage, the turn ratio N should be selected such that it satisfies the more restrictive of the two conditions expressed in (36) and (37).

$$\frac{D_{max} \cdot V_{bt,min}}{2 \cdot (V_{DC} - V_{bt,min})} \geq N \tag{36}$$

$$\frac{D_{min} \cdot V_{bt,max}}{2 \cdot (V_{DC} - V_{bt,max})} \geq N \tag{37}$$

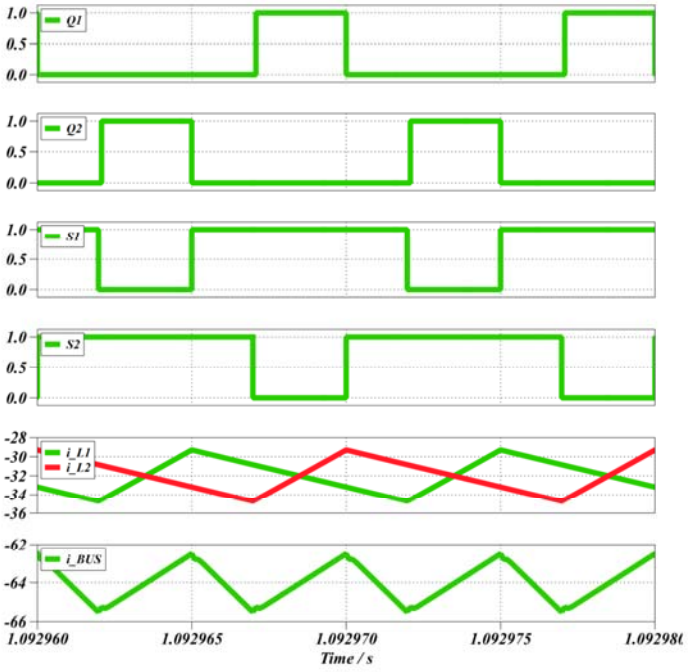

Fig. 9. Simulation waveforms at battery charge mode

In the proposed topology, the maximum duty cycle D_{max} is limited to 0.45 to ensure the dead time on the half-bridge. The minimum duty cycle, D_{min}, on the other hand, is set to 0.05 in consideration of gate drive requirements.

IV. SIMULATION RESULT

A simulation was conducted by the simulation software PLECS to verify the effectiveness of the proposed approach. In this simulation, the converter was configured to operate under constant current(CC) control mode of I_{bus}. Taking into account the variations in battery pack voltage, the K_p was set to 0.1 at the minimum battery voltage to ensure appropriate control stability. The remaining simulation parameters are listed in Table II.

At this time, the simulation was conducted under the condition that the battery voltage was at its minimum value, which is $V_{bt} = 360V$ and DC bus current $I_{bus} = 62.5A$. Fig. 9 illustrates the CC-mode operation waveform in step-up mode and Fig. 10 shows the step-down mode operation.

To limit maximum Δi_{bus} less than 2%, L_1 and L_2 are calculated with the minimum V_{bt} and the maximum D. According to (32), both L_1 and L_2 are selected as $200\mu H$. Similarly, $C_{1,2}$ and C_3 are selected as $30\mu F$ and $6\mu F$, respectively, to limit the maximum Δv_c to less than 1%. Q_1 and Q_2 are modeled using IMZC120R012M2H, while S_1 and S_2 are modeled as IMW65R007M2H. Each $R_{DS,on}$ of MOSFET are $25m\Omega$ and $6.7m\Omega$, respectively.

In Fig. 11, the voltage and current of the system at battery charge mode are represented. From the perspective of efficiency, the converter efficiency calculated in the step-up mode

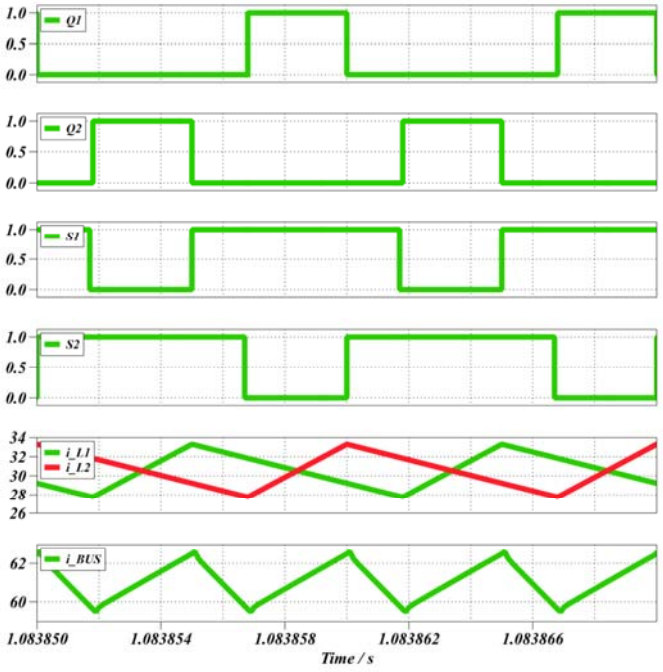

Fig. 10. Simulation waveforms at battery discharge mode

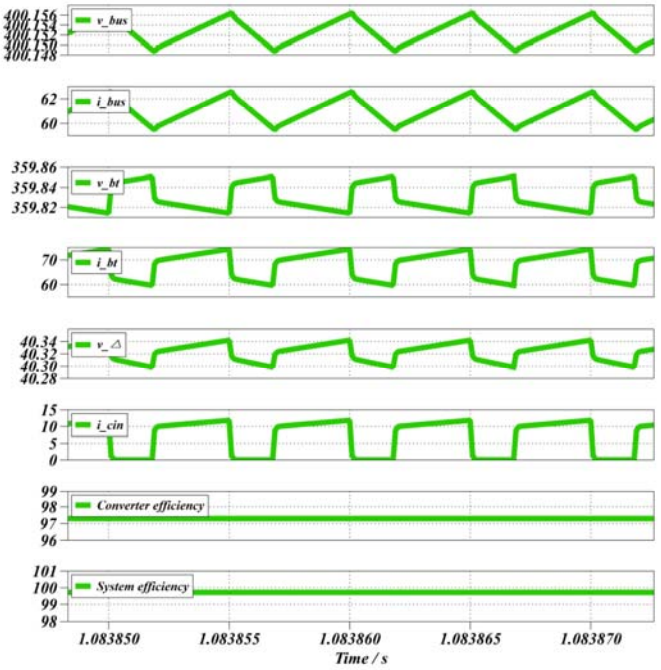

Fig. 12. Voltage, current, efficiency at battery discharge mode

was approximately 95%, whereas the overall system efficiency was confirmed to be around 99.5%.

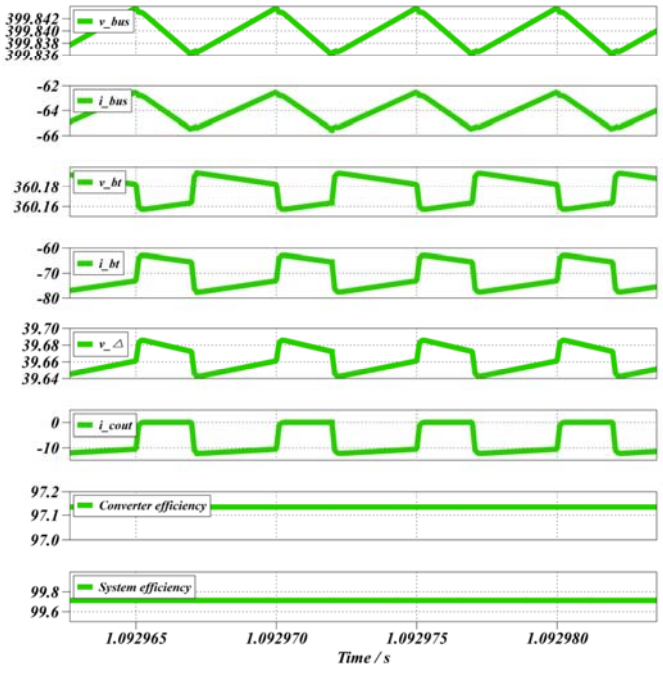

Fig. 11. Voltage, current, efficiency at battery charge mode

Similarly, in the step-down mode, the converter and system efficiencies were observed to be 95% and 99.5%, respectively, as shown in Fig. 12. These results are consistent with those calculated using (8).

V. Conclusion and Future Work

This paper presents a Partial Power Processing (PPP) converter for battery interfacing applications, aimed at improving system efficiency and reducing size of the converter. The basic fundamentals of PPP are introduced, and the operating principles of the proposed topology are analyzed. Simulation results demonstrate that the system efficiency exceeds 99.5%, while the converter itself achieves an efficiency of approximately 95%, processing only 10% of the total system power. In future work, an optimal design procedure for magnetic components tailored to specific system requirements will be addressed.

References

[1] Y. R. Kim *et al.*, "Comprehensive design of DC shipboard power systems for pure electric propulsion ship based on battery energy storage system," *Energies*, vol. 14, no. 17, pp. 5264, 2021.

[2] Z. Li *et al.*, "Development of DC/DC converter for battery energy storage supporting railway DC feeder systems," *IEEE Trans. Ind. Appl.*, vol. 52, no. 5, pp. 4218–4224, 2016.

[3] M. ElMenshawy and A. Massoud, "Hybrid multimodule DC-DC converters for ultrafast electric vehicle chargers," *Energies*, vol. 13, no. 18, pp. 4949, 2020.

[4] N. Kawakami *et al.*, "Development of a 500-kW modular multilevel cascade converter for battery energy storage systems," *IEEE Trans. Ind. Appl.*, vol. 50, no. 6, pp. 3902–3910, 2014.

[5] J. Anzola *et al.*, "Review of architectures based on partial power processing for DC-DC applications," Tech. Rep. ART-2020-118596, 2020.

[6] Y. D. Kwon *et al.*, "Partial power processing DC/DC MPPT converters in solar PV applications: Overview of architectures," in *Proc. IEEE 13th Int. Symp. Power Electron. Distrib. Gener. Syst. (PEDG)*, 2022.

[7] K. Sundararaman, P. Alagappan, and R. Elavarasu, "Partial processing converters for charging electric vehicles," in *Proc. 2021 Int. Conf. Advances Electr., Comput., Commun. Sustainable Technol. (ICAECT)*, 2021.

[8] J. S. Artal-Sevil *et al.*, "Partial power processing architecture applied to a battery energy storage system," in *Proc. IEEE Veh. Power Propuls. Conf. (VPPC)*, 2020.

[9] De Aragao Filho *et al.*, "A comparison between two current-fed push-pull DC-DC converters-analysis, design and experimentation," in *Proc. Int. Telecommun. Energy Conf. (INTELEC)*, 1996.

[10] D. Wu *et al.*, "Modeling and analysis of partial power concept for data center application," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, 2024.

[11] B. Ejaz *et al.*, "A comprehensive review of partial power converter topologies and control methods for fast electric vehicle charging applications," *Electronics*, vol. 14, no. 10, pp. 1928, 2025.

[12] O. Gsous *et al.*, "Review of DC-DC Partial Power Converter Configurations and Topologies", *Energies*, vol.17, no. 6, pp. 1496, 2024.

[13] P. Granello *et al.*, "Revisiting the Partial Power Processing Concept: Case Study of a 5-kW 99.11% Efficient Flyabck Converter-Based Battery Charger", *IEEE Trans. Transp. Electrif.*, vol. 8, no. 3. pp. 3934, 2022.