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# Novel Dynamic Resistance Equalizer for Parallel-Connected Battery Configurations

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**Abstract:** As the number of parallel battery connections in an energy storage system is increased to extend the energy capacity and second-life batteries are actively adopted, the battery is more prone to cell inconsistency issues. The difference in the internal impedance and the mismatched state-of-charge accelerates the self-balancing effect between the parallel branches to reduce cell utilization and eventually results in harmful effects, both to the lifetime and to the safety of the batteries. However, conventional methods only partially mitigate the parallel inconsistency issue. This paper proposes a dynamic resistance equalizer for parallel-connected battery configurations to improve equalization performance. The optimal design procedure is also presented to minimize the power loss and equalization time. The overall performance is experimentally verified by a sequence of tests for a Li-ion battery in a 2S-4P configuration. The experimental results show that the proposed method dissipates less external power loss than the fixed resistor equalizer and less internal loss than the conventional sequencing method. When both total loss and balancing performance are considered together, as the number of series connections increases, the merits of the proposed method stand out. This is verified by additional hardware-in-the-loop tests, presenting a fascinating feature for most practical battery applications.

**Keywords:** battery equalization; design optimization; dynamic resistance equalizer (DRE); state-of-charge (SOC); second-life battery energy storage system (SL-BESS)

## 1. Introduction

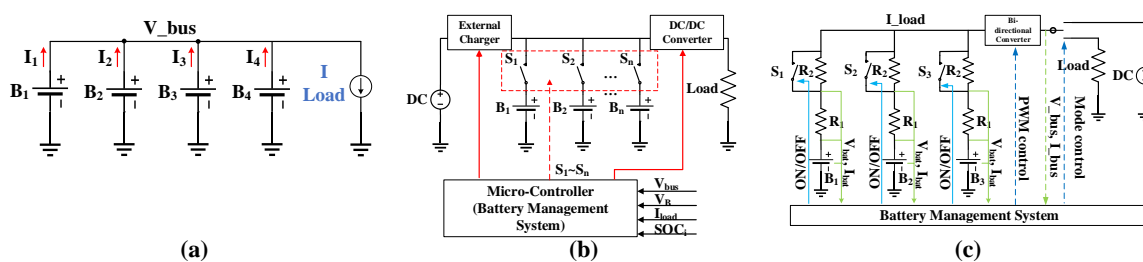
In an effort to prevent climate change, the transportation industry is becoming increasingly electrified [1,2]. However, the battery packs of electric vehicles (EV) have a limited lifespan and usually need to be replaced when the state-of-health decreases to 70–80% [3]. Although some disassembling and recycling procedures have been proposed, as in [4,5], it is not yet economically feasible. Meanwhile, the second-life battery energy storage system (SL-BESS) is a promising solution to re-use the retired battery packs [6]. However, the difference in the internal impedance, capacity, and electrical characteristics between cells—so-called cell-inconsistency—becomes more serious in the second-life battery application.

In most energy storage systems, like EV or SL-BESS, battery cells are connected in series to reach the operating voltage specification. However, due to the imbalance in the electrochemical impedance, cell-inconsistency issues arise, and thus, various cell-balancing techniques for the series-connected battery cells have been developed, which can be classified into passive and active techniques [7,8]. Due to energy dissipation, passive cell-balancing methods have low efficiency and speed [9], but are cost-effective and less complex compared to active methods. On the contrary, active techniques employ a switched inductor [10], a switched capacitor [11], or a dc-dc converter [12] to ensure better equalization performance and efficiency.

Nowadays, due to the strong demand for higher battery capacities in the market, some manufacturers are working on larger format cells, while there are also requirements for an increased number of parallel connections. For example, the Nissan Leaf EV consists of two cells in parallel [13], the Chevrolet Volt plug-in hybrid EV utilizes three parallel-connected cells [14], and an energy storage system for a data center has a much larger number of battery cells connected in series and parallel [15].

Many researchers have reported that cell-inconsistency in parallel battery configurations can cause serious problems, as in the series case. If the open-circuit voltages of the batteries are different, there are continuous currents flowing across branches to balance the terminal voltage of parallel connection even in idle mode, when the battery is not exchanging any energy with the external source or load, which is called the self-balancing effect. Because the internal impedance of the battery is small, the amplitude of the self-balancing current is large and generates additional cell-heating and accelerates the battery aging. The different voltage drops in the different internal impedances make an unequal equilibrium open-circuit voltage in the battery cells in parallel, which eventually causes the unbalanced SOC even after the self-balancing process. As a result, when the paralleled battery is charged or discharged without any cell balancing scheme, it could cause the over-charging or over-discharging problems [16–19]. The experiments in [20] show that the battery is internally shorted during the over-discharge process in the parallel configuration.

Conventionally, the simplest method to prevent this issue is cell-binning or screening by measurements, which allows only cells with similar characteristics to be connected, as in Figure 1a. However, it requires an additional step of classification but does not always guarantee good performance, since the impedance of the cells tends to drift further, especially in SL-BESS applications [21]. As an alternative, sequencing switches can be attached to equalize the SOC (as in Figure 1b) [22–24], where the switching decision is made based on the SOC information of the cells. However, continuously pulsating currents increase the internal power loss inside batteries. On the other hand, Kuo et al. [25] proposed a passive method to distribute the currents evenly using a fixed balancing resistor, as in Figure 1c. However, this mechanism neither provides equalization performance nor cell utilization when the initial conditions of the battery cells are substantially different. The most serious problem related to this method is the considerable power dissipation in the balancing resistors.

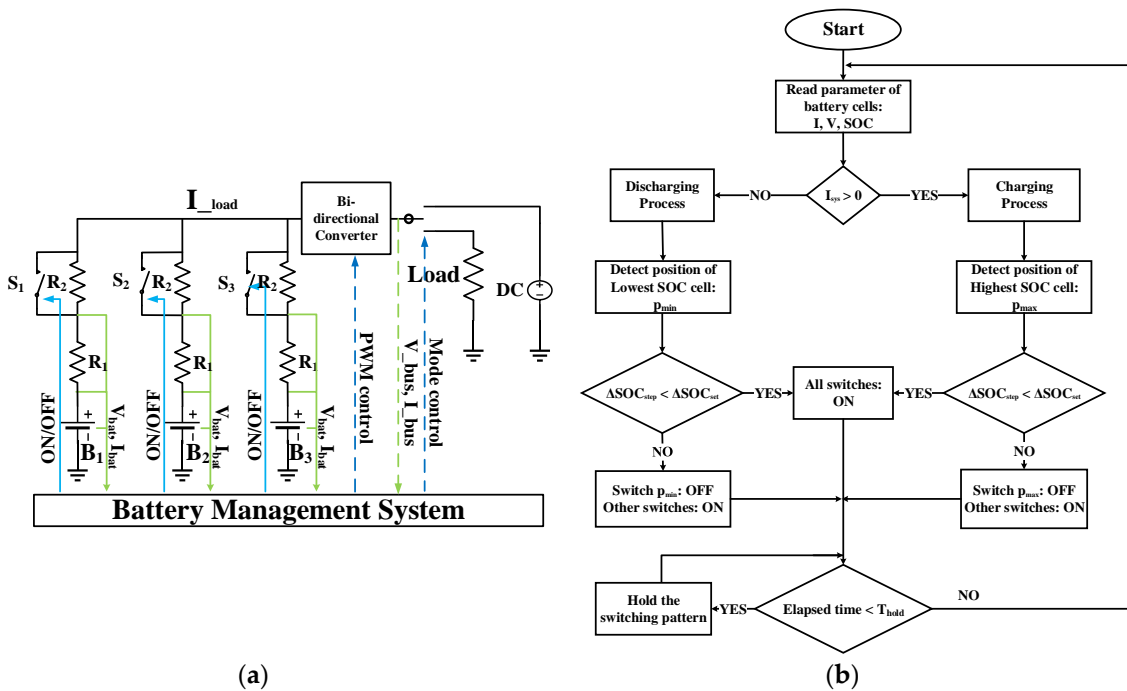


**Figure 1.** Conventional methods: (a) directly-connected; (b) state-of-charge (SOC)-based sequencing method; (c) fixed-resistor method.

While the conventional methods only partially mitigate the problem, this paper proposes a novel equalizer for the parallel-connected battery configuration to provide a viable and acceptable way to solve the inconsistency issue. Since the basic concept was originally presented in [26], we have extended it by appending operational analysis, design optimization, and more experimental verification in this paper. The equalizer topology is described in Section 2, analysis of the operation and the optimal design guidelines are suggested in Section 3, verification is presented in Section 4, and conclusions are made in Section 5.

## 2. Proposed Equalizer

The proposed circuit in Figure 2a utilizes two resistors and one switch per branch to construct a dynamic resistance equalizer (DRE). The bi-directional converter is used to regulate the output of the battery system in discharging mode or charge the battery cells in charging mode. By controlling the switches,  $S_1$ ,  $S_2$  and  $S_3$ , the effective series impedances of the branches are adjusted to control the current flow in each branch. The switching decision is made based on the SOC level of the cells which can be estimated by various reported estimation methods [27]. In this paper, a Coulomb counting is used to estimate the SOC where the equalization resistor  $R_1$  concurrently serves as a current sensor. However, other SOC estimation methods can be merged into this topology. The flowchart of the equalization algorithm is shown in Figure 2b, where the switching decision is different for the charging and discharging processes:



**Figure 2.** Proposed method: (a) dynamic resistance equalizer topology; (b) flowchart of the equalization.

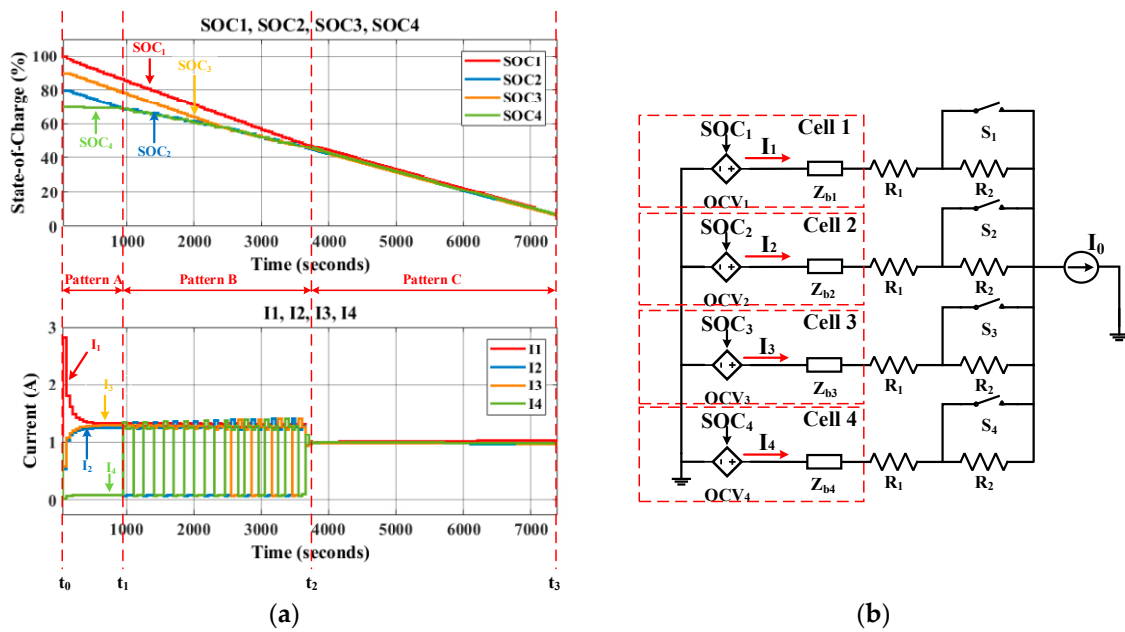
The operation process is divided into multiple equalization cycles with a period of  $T = T_m + T_{hold}$ , where  $T_m$  is the required time to measure the cell parameters for SOC estimation and  $T_{hold}$  is the holding time to keep the switching pattern. During  $T_m$ , according to the current direction, the battery management system (BMS) detects whether the process is in the discharging or charging mode, the SOC comparison algorithm identifies the lowest SOC cell (in case of the discharging mode),  $p_{min}$ , or the highest SOC cell (in case of the charging mode),  $p_{max}$ , and the maximum SOC difference (MSD) is calculated to make the switching decision. If the MSD is higher than a pre-defined value,  $\Delta SOC_{set}$ , the corresponding switch in the highest SOC cell (in charging mode) or the lowest SOC cell (in discharging mode) is turned off while the other switches are kept on. As a result, the impedance of the chosen branch becomes higher than the others, which reduces its branch current. By discharging/charging the battery cells with such a controlled branch impedance, the SOC of the cell are step-by-step equalized. When the MSD becomes lower than  $\Delta SOC_{set}$ , all switches are turned on to distribute the current evenly and minimize the power loss in balancing resistor. The switching pattern is held during  $T_{hold}$  before another equalization cycle starts.

### 3. Equalization Process Analysis and Design Optimization

#### 3.1. Equalization Process Analysis

Obviously, there is a trade-off between the equalization performance and the power loss in the equalization resistor, both of which are dependent on the design of  $R_1$  and  $R_2$ . To analyze the power loss and the equalization performance of the DRE, an example of four parallel-connected batteries in the discharging mode with load current,  $I_0$ , is illustrated in this section. It should be noticed that the behavior of the equalizer in the charging mode is similar.

The process starts with an initial pre-defined SOC and stops when one of the cells becomes fully discharged. The initial setup in this case study are  $SOC_1 > SOC_3 > SOC_2 > SOC_4$  and the impedances of the battery cells are set to be different from each other. Depending on the initial SOC of the cells, the control algorithm in Section 2 drives the switches into one of three switching patterns at each equalization cycle, which are illustrated in Figure 3a: pattern A which performs suppressive balancing ( $t_0 - t_1$ ), pattern B which performs sequential balancing ( $t_1 - t_2$ ), or pattern C which triggers direct low-impedance balancing ( $t_2 - t_3$ ).



**Figure 3.** Operation of dynamic resistance equalizer (DRE): (a) discharging process of four parallel-connected battery cells; (b) modeling of the dynamic resistance equalizer.

During pattern A, the current is unevenly distributed to equalize the SOCs of cells. According to the algorithm, the switches #1, #2, and #3 are turned on while the switch in branch #4 (the lowest SOC cell) is kept off to suppress the current flow. The impedances of the individual branches are calculated by (1), where  $Z_{bm}$  is the internal impedance of the cells ( $m = 1, 2, 3, 4$ ) and  $R_{d\_on}$  is the on-resistance of the MOSFET switch. Therefore, the individual branch current is obtained as (2) by applying Kirchhoff's law to the model in Figure 3b, where the  $OCV_m$  ( $m = 1, 2, 3, 4$ ) is the open-circuit voltage of the battery cell and  $I_0$  is the load current.

$$\begin{cases} Z_1 = Z_{b1} + R_1 + \frac{R_{d\_on}R_2}{(R_{d\_on}+R_2)} \\ Z_2 = Z_{b2} + R_1 + \frac{R_{d\_on}R_2}{(R_{d\_on}+R_2)} \\ Z_3 = Z_{b3} + R_1 + \frac{R_{d\_on}R_2}{(R_{d\_on}+R_2)} \\ Z_4 = Z_{b4} + R_1 + R_2 \end{cases} \quad (1)$$

$$\begin{cases} Z_1 I_1 - Z_2 I_2 = OCV_1 - OCV_2 \\ Z_1 I_1 - Z_3 I_3 = OCV_1 - OCV_3 \\ Z_1 I_1 - Z_4 I_4 = OCV_1 - OCV_4 \\ I_1 + I_2 + I_3 + I_4 = I_0 \end{cases} \quad (2)$$

The SOCs of the cells are updated once in the unit equalization cycle, so the sampling period is  $T$  and the SOC levels of the battery cells are calculated by (3):

$$SOC_m(k) = SOC_m(k-1) - \frac{I_m(k-1)T}{Q} \quad (3)$$

where  $Q$  is the full capacity of the cells,  $I_m$  is the  $m^{th}$  branch currents and  $SOC_m$  is the state-of-charge of the  $m^{th}$  cell ( $m = 1, 2, 3, 4$ ), and  $k$  is the number of unit cycles. Pattern A is terminated when the SOCs of the two lowest SOC cells (or highest SOC cells in charging mode), cell #4 and #2 in this case study, become equal. The termination time,  $t_1$ , is calculated by (4), where  $k_{t1}$  is the required number of sampling steps before the termination of pattern A. The average power loss during pattern A in the equalizer circuit is calculated by (5), where  $P_m(k) = Z_m I_m^2(k-1)$  is the power loss of the individual branch at each step  $k$ .

$$t_1 = k_{t1}T \quad (4)$$

$$P_{int1\_avg} = \frac{\sum P_m(k)}{k_{t1}} \quad (5)$$

In pattern B, only the switch of the highest SOC cell (cell #1) is kept on while all other switches perform the sequential switching pattern as in Figure 4. The average currents in branches #2, #3, and #4 are calculated by (6), where  $I_{max}$  and  $I_{min}$  are the maximum and the minimum branch currents at  $t_1$ , and the current on branch #1 shows the maximum value,  $I_{max}$ . Pattern B lasts from  $t_1$  to  $t_2$  when the SOCs of all cells are equalized within a threshold level, so the termination of this pattern can be regarded as the end of an active equalization process. The termination time,  $t_2$ , is estimated by (7). It is also possible to calculate the average power loss in branch #1 by (8) while the power losses in the other branches are obtained by (9).

$$I_{m\_avg} = \frac{2I_{max} - I_{min}}{3} \quad (6)$$

$$t_2 = Q \frac{SOC_{highest}(t_1) - SOC_{lowest}(t_1)}{I_{max} - I_{m\_avg}} + t_1 \quad (7)$$

$$P_{1\_int2} = Z_1 I_{max}^2 \quad (8)$$

$$P_{2\_int2} = P_{3\_int2} = P_{4\_int2} = \frac{2Z_{on}I_{max}^2 + Z_{off}I_{min}^2}{3} \quad (9)$$

During pattern C, all branch switches are kept on to incur low resistance passive balancing. The total discharge time,  $t_3$ , which indicates the end of discharge mode, is calculated by (10). The currents of each branch are calculated by (11) and the power losses during this duration are calculated by (12). Kindly note that the impedances of branches ( $Z_1, Z_2, Z_3, Z_4$ ) in pattern C become the sum of battery impedance and  $R_1$ , which almost equal each other.

$$t_3 = Q \frac{\sum_{m=1}^N SOC_{m\_init}}{I_0} \quad (10)$$

$$\begin{cases} Z_1 I_1 - Z_2 I_2 = 0 \\ Z_1 I_1 - Z_3 I_3 = 0 \\ Z_1 I_1 - Z_4 I_4 = 0 \\ I_1 + I_2 + I_3 + I_4 = I_0 \end{cases} \quad (11)$$

$$P_{1\_int3} = P_{2\_int3} = P_{3\_int3} = P_{4\_int3} = Z_{on}I_{int3}^2 \quad (12)$$

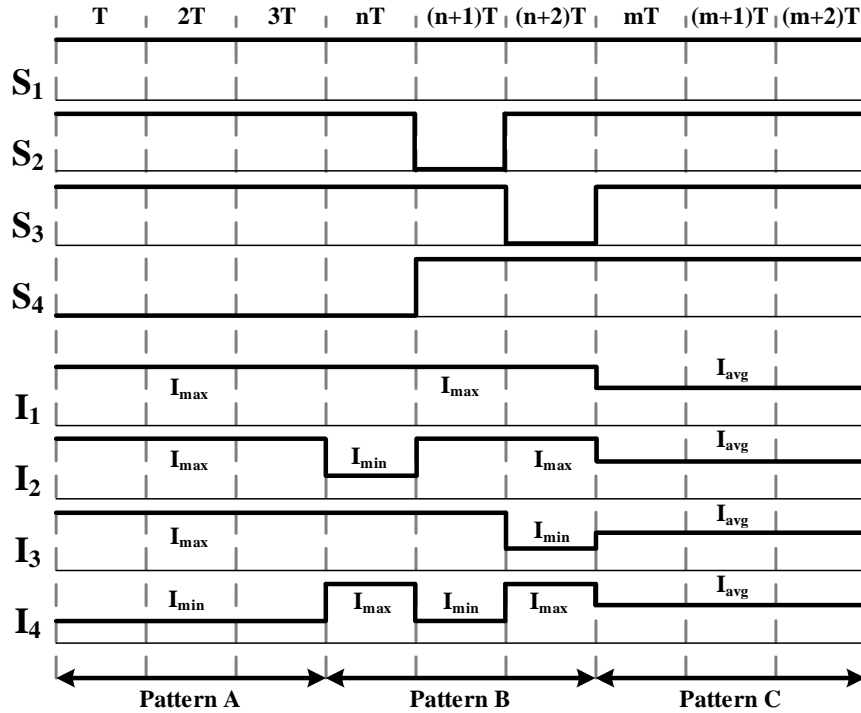


Figure 4. Typical switching patterns and corresponding branch currents.

Considering the overall process, the total external power loss in the balancing resistor and the total average current in each branch are calculated by (13), and (14), respectively. To evaluate the performance of the equalizer, the degree of SOC equalization (DoSE), which is defined by (15), is introduced in this paper, where a unity DoSE means perfect equalization while null DoSE stands for no equalization.  $\Delta SOC_{initial}$  is the SOC difference between the highest and the lowest cell at the initial time and  $\Delta SOC_{final}$  is the SOC difference between the highest and the lowest cell at  $t_3$ . Besides,  $I_{highest\_cell}$  is the average current of the highest SOC cell, and  $I_{lowest\_cell}$  is the average current of the lowest SOC cell. Another performance index is the equalization speed, which is determined by the equalization time,  $t_2$ .

$$P_{loss} = \frac{P_{int1}t_1 + P_{int2}(t_2 - t_1) + P_{int3}(t_3 - t_2)}{t_3} \quad (13)$$

$$I_{m\_avg} = \frac{I_{m\_int1}t_1 + I_{m\_int2}(t_2 - t_1) + I_{m\_int3}(t_3 - t_2)}{t_3} \quad (14)$$

$$DoSE = \frac{\Delta SOC_{initial} - \Delta SOC_{final}}{\Delta SOC_{initial}} = \frac{(I_{highest\_cell} - I_{lowest\_cell})t_3}{\Delta SOC_{initial}} \quad (15)$$

### 3.2. Design Optimization

Among the equalization performance indices, the total power loss and the equalization speed have a trade-off relationship. Thus, the value of the equalization resistors,  $R_1$ , and  $R_2$ , should be carefully chosen to satisfy the constraints below:

$$\Delta I < \Delta I_{max} \quad (16)$$

$$I_1 + I_2 + \dots + I_n = I_0 \quad (17)$$

$$R_1 < R_2; \quad R_{1min} < R_1 < R_{1max}; \quad R_2 > R_{2min} \quad (18)$$

where  $\Delta I$  and  $\Delta I_{max}$  are the current difference between branches and its maximum allowable value,  $I_0$  is the charging or discharging current,  $R_{1min}$  and  $R_{1max}$  are the upper and lower boundary of  $R_1$ , and  $R_{2min}$  is the lower boundary of  $R_2$ , respectively.

Finally, the optimal design procedure is suggested in 5 steps. Even though the design case of four modules is illustrated here as an example, this procedure can be adapted to any number of parallel connections with various characteristics.

- **Step 0: Initial assumption**

The four branches have an equal capacity (2000 mA) but different in SOCs ( $SOC_{init1,2,3,4} = 100\%, 80\%, 90\%, 70\%$ ). The internal impedance of the batteries is considered to be equal to  $R_b = 70 \text{ m}\Omega$ , according to the manufacturer's datasheet in [28]. The load current is set to constant 4 A and the unit equalization cycle time is 5 s.

- **Step 1: Determine  $R_{1min}$**

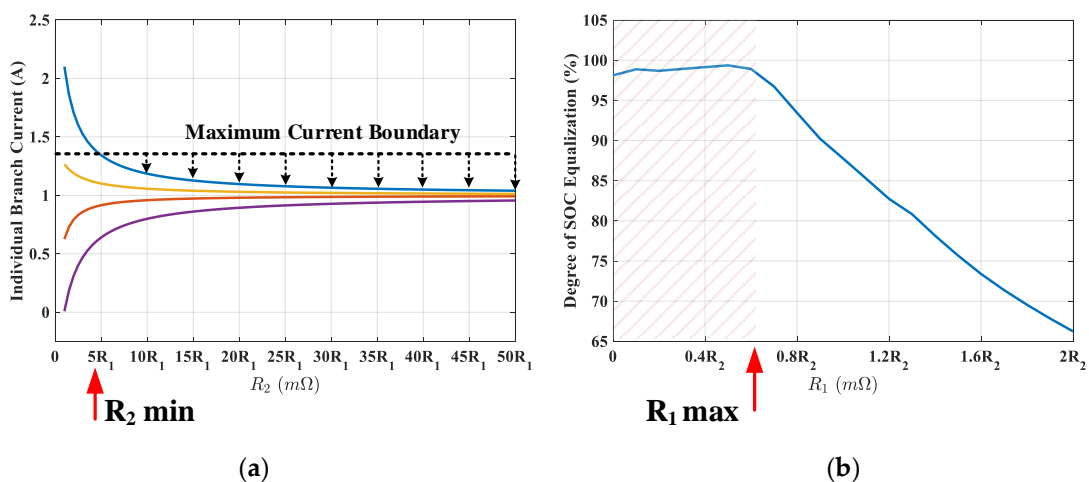
Even after the SOCs of the cells are equalized, the different internal impedance makes the different branch currents. In pattern C, the value of  $R_1$  determines such a final current difference between branches. However, because the battery impedance is inaccessible without off-line measurement, the value of  $R_1$  is chosen to be approximate to the internal impedance of battery in the datasheet ( $R_{1min} \approx 70 \text{ m}\Omega$ ).

- **Step 2: Determine  $R_{2min}$  from the initial current difference.**

At time  $t_0$ , the current sharing ratio is dependent on the ratio of  $R_2$  to  $R_1$  by (1) and (2). By fixing the value of  $R_1$  at  $R_{1min}$ , the initial current difference changes according to  $R_2$ . To protect every cell from overloading, a boundary current is set and  $R_{2min}$  is obtained from Figure 5a.

- **Step 3: Determine  $R_{1max}$  from the DoSE requirement.**

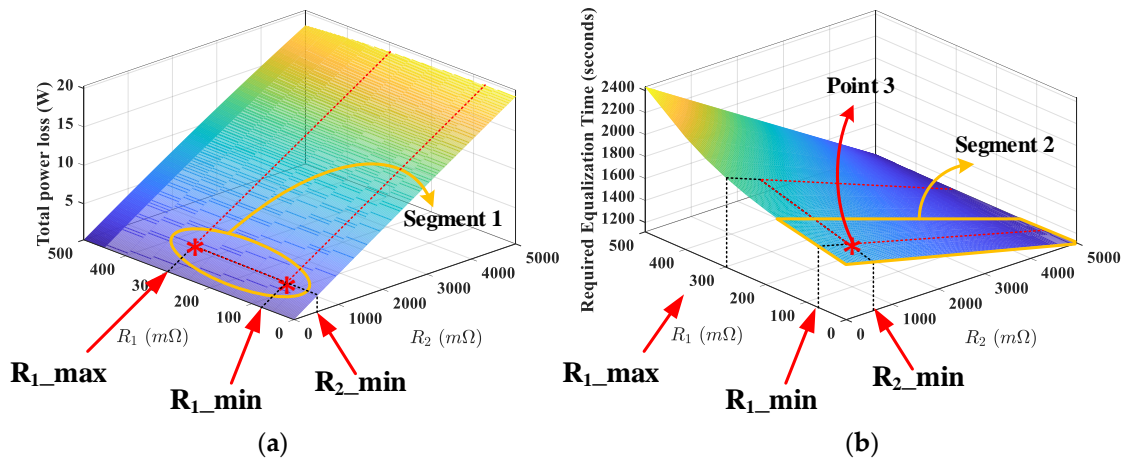
The ratio of  $R_1$  to  $R_2$  also affects the DoSE. The overall DoSE of the system is plotted with the various ratios of  $R_1$  to  $R_2$  as shown in Figure 5b, where  $R_{1max}$  can be determined to maintain the high DoSE index.



**Figure 5.** Design plots for the balancing resistors: (a) maximum initial current difference vs.  $R_2$ ; (b) overall DoSE vs.  $R_1$ .

- **Step 4: Choose  $R_1$  and  $R_2$  by considering the total power loss and the equalization time.**

Finally, the total power loss according to  $R_1$  is calculated by (13) and illustrated in Figure 6a. Similarly, the time to achieve the equalization,  $t_2$ , is calculated by (7) and plotted in Figure 6b. Depending on the design scenario, the values of  $R_1$  and  $R_2$  are chosen as follows:



**Figure 6.** Performance indices according to design scenario: (a) total power loss vs.  $R_1$  and  $R_2$ ; (b) required equalization time vs.  $R_1$  and  $R_2$ .

**Scenario 1:** If the power loss is the only consideration, the value of  $R_1$  and  $R_2$  are obtained by Figure 6a, where the segment 1 is the possible solution ( $R_{1min} \leq R_1 \leq R_{1max}$  and  $R_2 = R_{2min}$ ). However, the equalization time becomes longer and one branch must work with a higher current until equalization is achieved.

**Scenario 2:** If the equalization speed is the only consideration, the value of  $R_1$  and  $R_2$  are chosen by Figure 6b, where the segment 2 is the possible solution ( $R_1 = R_{1min}$  and  $R_2 > R_{2min}$ ). As  $R_2$  increases, the power loss becomes very high as a trade-off.

**Scenario 3:** To balance the trade-off between the equalization speed and the power loss, the intersecting point 3 between segment 1 and segment 2 is the optimal solution, where  $R_1 = R_{1min}$  and  $R_2 = R_{2min}$ .

## 4. Verification

### 4.1. Experiment Setup

To verify the performance of the DRE, a prototype of a 2S4P battery configuration is implemented. In this paper, 2S4P denotes a structure of battery connection where two cells are connected in series as a branch and then paralleled in four. In the equalizer circuit, a pair of two back-to-back MOSFETs serves as an ideal switch. The hardware components are listed in Table 1. To measure the SOC of each battery cell, MAX17205G fuel gauges are used and the switching patterns are generated by a microcontroller. The branch currents are observed using a Hioki LR8402-20 data logger, a dc power supply is used to charge the battery, and the PLZ153WH electric load serves as a constant current load. The unit equalization cycle time is set to 5 s. Finally, the measured data from the fuel gauges and data logger are plotted by MATLAB software.

**Table 1.** Component list.

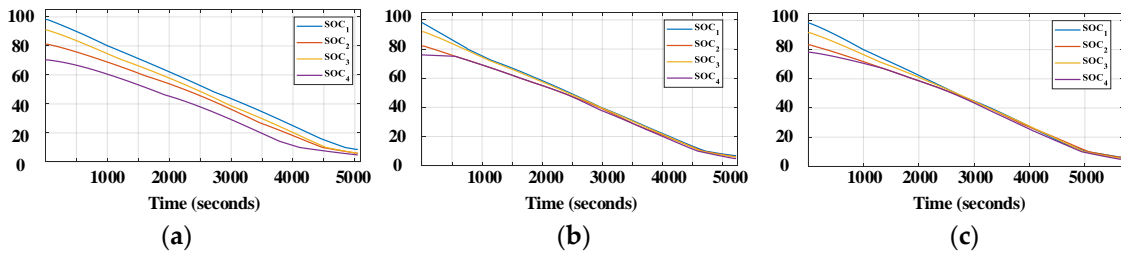
Component	Part Number	Quantity
Switches	IRF8313PbF	4
Gate driver	TC4429	4
Opto-coupler	4N25	4
Fuel gauge	MAX17205G	4

### 4.2. Performance Optimization by Different Design Scenario

To assess the feasibility of the suggested optimal design procedure, three design scenarios from step 4 of Section 3.2 are implemented. The values of the equalization resistors and the initial SOC



conditions of the cells are chosen as shown in Table 2. The SOC profile of the discharging process is tested and presented in Figure 7. In scenario 1, when the value of  $R_2$  is arbitrarily chosen as slightly larger than  $R_1$  to minimize the power loss in the balancing circuit, poor DoSE performance can be achieved as shown in Figure 7a. On the contrary, the design in scenario 2, which is optimized for the speed, and scenario 3, which is optimized for both the speed and power loss, show better DoSE performance. The termination time of the equalization,  $t_2$ , in scenario 2 is smaller than that in scenario 3 (Figure 7b,c), which means that the equalization speed of DRE is higher as  $R_2$  becomes much larger than  $R_1$ .



**Figure 7.** Discharging mode–SOC of branches: (a) design scenario 1 ( $R_1 = 0.1 \Omega$ ,  $R_2 = 0.33 \Omega$ ); (b) design scenario 2 ( $R_1 = 0.1 \Omega$ ,  $R_2 = 1 \Omega$ ); (c) design scenario 3 ( $R_1 = 0.1 \Omega$ ,  $R_2 = 0.5 \Omega$ ).

**Table 2.** Design scenario and performance comparisons.

	Scenario 1	Scenario 2	Scenario 3
$\Delta SOC_{initial}$ (%)	30	30	30
$\Delta SOC_{final}$ (%)	5	<1	<1
$R_1$ & $R_2$ ( $\Omega$ )	0.1 & 0.33	0.1 & 1	0.1 & 0.5
DoSE (%)	83.3	>98	>98
$t_2$ (s)	N/A	2300	2500
$\sum P_{loss\_external}$ (W)	1.57	3.59	1.96

The results in Table 2 show that both scenarios 2 and 3 have the same DoSE performance (>98%) while scenario 1 shows a lower performance (83.33%). Although the equalization speed of scenario 2 is lightly faster than scenario 3, the difference is trivial. Based on the recorded experimental results, the power loss on the equalization resistor and switches of the proposed method is calculated by (19) and compared in Table 2:

$$P_{loss\_external} = \sum_{m=1}^N \frac{1}{t_3} \int_0^{t_3} i_m^2(t) Z_m(t) dt \quad (19)$$

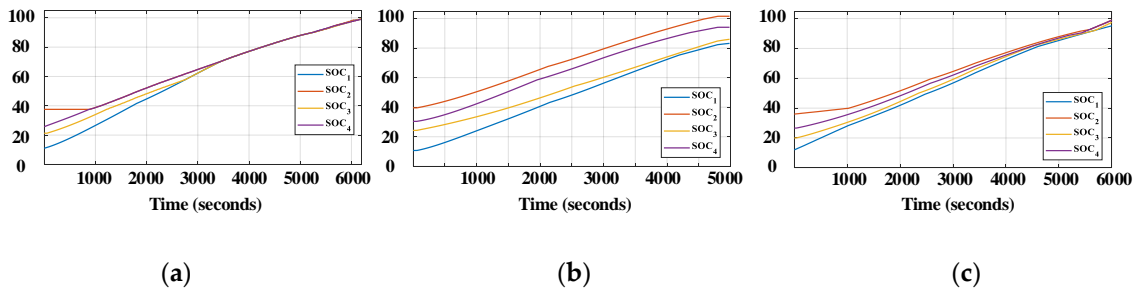
where  $i_m(t)$  is the measured current of each branch, the impedance of branches is calculated by  $Z_m(t) = R_1 + R_{d,on} || R_2$  (when the switch is turned on) or  $Z_m(t) = R_1 + R_2$  (when the switch is turned off),  $R_1$  and  $R_2$  are the equalization resistance, and  $R_{d,on}$  is the on-resistance of the switch. Scenario 3 shows half the loss of scenario 2, which is slightly higher than scenario 1 in the power loss in the balancing resistor. It means that scenario 3 is the optimal design from the perspective of both power loss and equalization speed.

#### 4.3. Equalization Performance of Different Methods in 2S4P Configuration

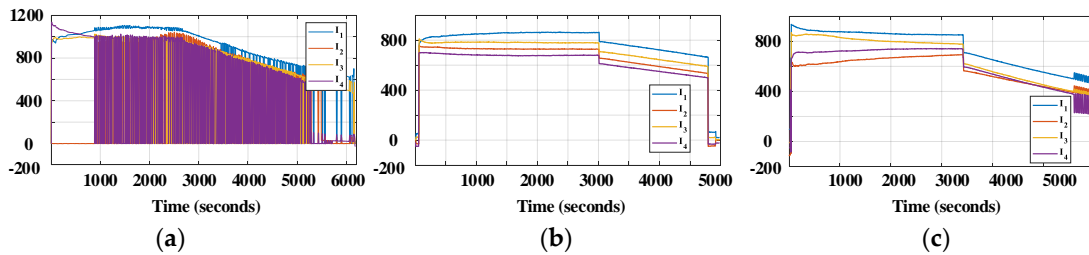
The experiments are performed on the cells with the parameter in Section 3.2. During both charging and discharging mode, the proposed method is compared with the conventional methods: SOC-based sequencing in Figure 1b and the fixed-resistor method in Figure 1c.

In charging mode, the battery system is charged by the 3 A/8.4 V CC-CV method and the initial SOC of the cells are  $SOC_{init1,2,3,4} = 15, 40, 20, 30\%$ . Similarly, the battery cells are discharged by a constant current of 4 A with different initial SOC ( $SOC_{init1,2,3,4} = 100, 80, 90, 70\%$ ) in discharging mode.

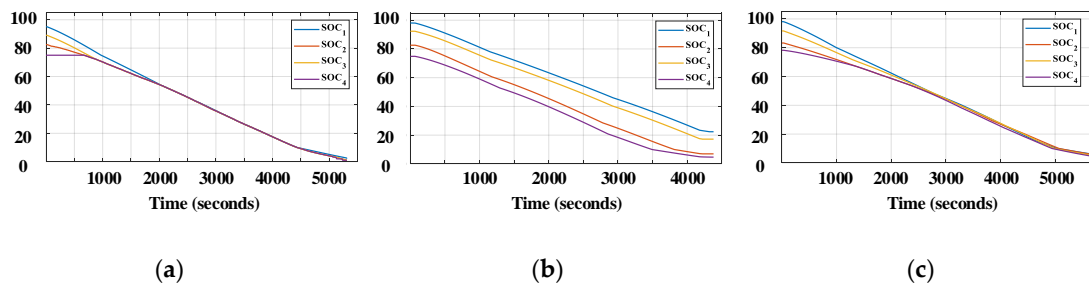
The equalization resistor of the proposed method is chosen as scenario 3 in Table 2 after the design optimization process, while the equalization resistor of the fixed-resistor method is chosen as  $1 \Omega$ . The experiment is stopped when any battery branch reaches 100% of the SOC during charging mode, or less than 5% of SOC during discharging mode. The SOC and currents of the battery branch are shown in Figures 8 and 9 for charging mode, and Figures 10 and 11 for discharging mode, respectively. Finally, the equalization performance indices are calculated and compared in Table 3 based on the experimental results.



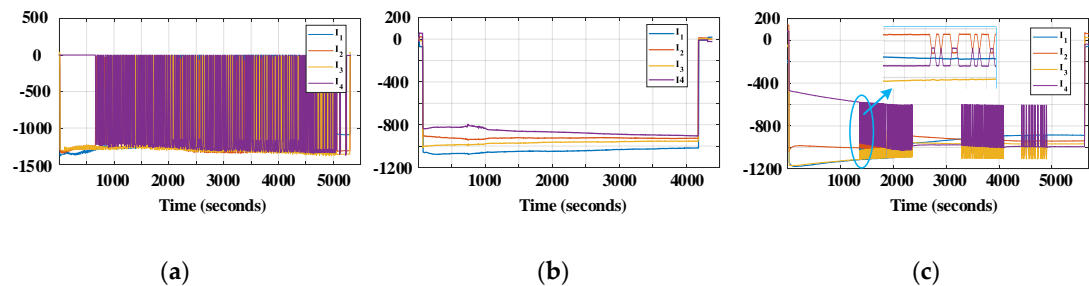
**Figure 8.** Experimental results of charging mode for 2S4P configuration—SOC of branches: (a) SOC-based sequencing method; (b) fixed-resistor method; (c) proposed method.



**Figure 9.** Experimental result of charging mode for 2S4P configuration—branch currents: (a) SOC-based sequencing method; (b) fixed-resistor method; (c) proposed method.



**Figure 10.** Experimental result of discharging mode for 2S4P configuration—SOC of branches: (a) SOC-based sequencing method; (b) fixed-resistor method; (c) proposed method.



**Figure 11.** Experimental result of discharging mode for 2S4P configuration—branch currents: (a) SOC-based sequencing method; (b) fixed-resistor method; (c) proposed method.

**Table 3.** Equalization performances comparison.

Mode	Performance Index	Fixed-Resistor Method	Proposed Method	SOC Sequencing Method
Charging mode	DoSE (%)	40	98	98
	$t_2$ (seconds)	N/A	4500	3400
Discharging mode	DoSE (%)	46	98	98
	$t_2$ (seconds)	N/A	2500	2000

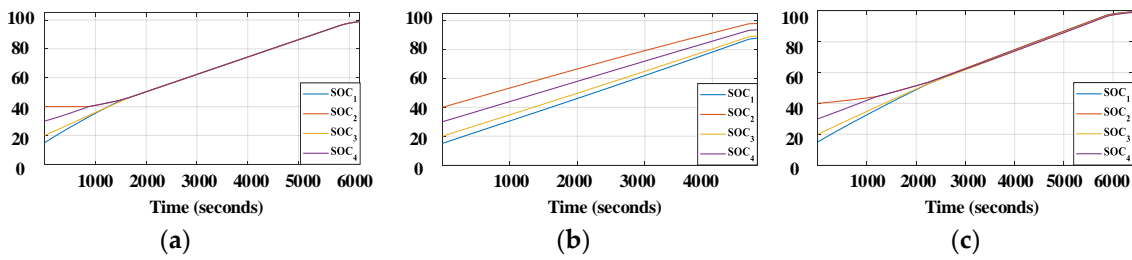
The SOC profiles in Figure 8 (charging mode) and Figure 10 (discharging mode) show that both the SOC-sequencing and the proposed method have the almost equivalent SOC equalization performance: although the equalization speed of the SOC-sequencing method is higher than that of the proposed method, the DoSE indices of both are similar. It means that all branches can be almost fully charged or fully discharged. On the contrary, the DoSE index of the fixed-resistor method is low and the operation process is forced to stop before all cells are fully charged or discharged (Figures 8b and 10b).

According to the current profiles in Figures 9b and 11b, the conventional fixed-resistor method maintains the continuous current during both charging and discharging mode. On the contrary, the SOC-sequencing method creates the pulsating branch current waveform as in Figures 9a and 11a, due to the control algorithm. As a result, the current increases the internal power loss of the battery cell, which is regarded as harmful to battery lifetime [29,30].

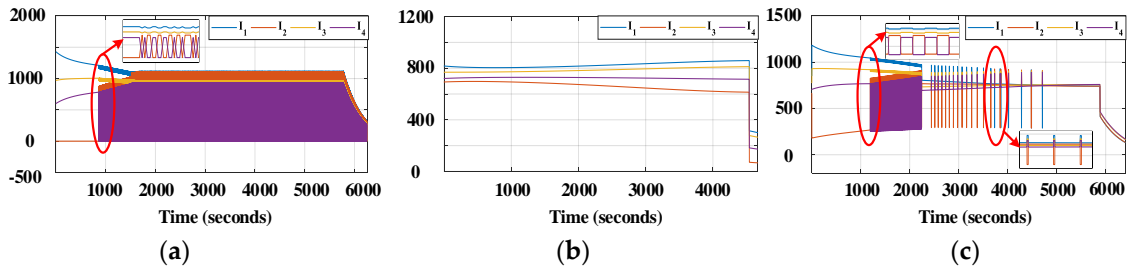
With the optimal design, the proposed method appropriately reduces the pulsation of the current during both the charging and discharging modes, as in Figures 9c and 11c. As a result, the RMS currents of battery branches are also decreased, which reduces the internal power loss of battery. Further investigation on the impact of pulsating current is presented in Section 4.4. Additionally, three switching patterns can be identified in Figure 11c according to the operating analysis in Section 3.1. During pattern A, battery cell #4 is discharged with the lowest current until its SOC is equalized with cell #2. During pattern B, the algorithm alternately turns the switches in branches #2, #3, and #4 off and on to maintain the SOC equalization until the SOC of all cells are equalized. After equalization is achieved within a certain level, the pattern C starts to turn all the switches on so that the load demand is distributed almost evenly between branches. After the SOC becomes mismatch again, patterns A and B are repeated to recover the equalization status.

#### 4.4. Efficiency Assessment of Different Methods in Various Configuration

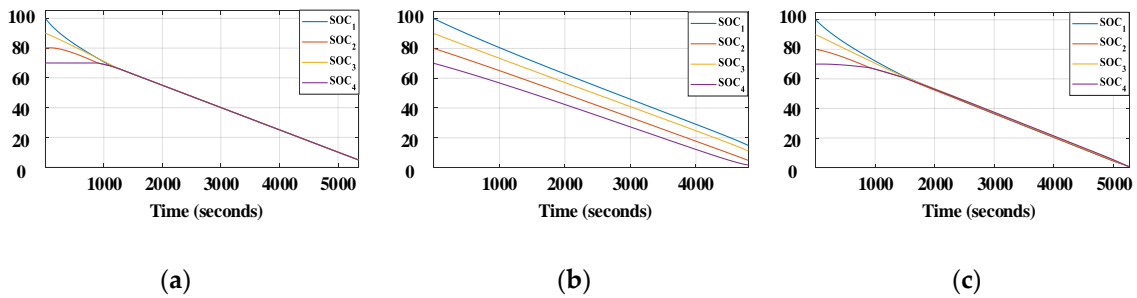
In order to assess the efficiency of the proposed method in a real application where the series connection in parallel branches becomes large, the hardware in the loop (HIL) simulation of the proposed and conventional methods are implemented into 2S4P, 4S4P, and 8S4P battery configurations. The initial status of the battery branches and experiment setups are similar to Section 4.3. In order to check the feasibility of the HIL test, the 2S4P battery configuration is tested firstly and compared with the real hardware experimental results. The SOC and current profiles of the 2S4P battery configuration are illustrated in Figures 12 and 13 for charging mode, and Figures 14 and 15 for discharging mode, respectively. When compared with the experimental results in Section 4.3, the HIL simulation results are similar. Thus, the HIL simulation is reliable to assess the performance of balancing techniques in various battery configurations.



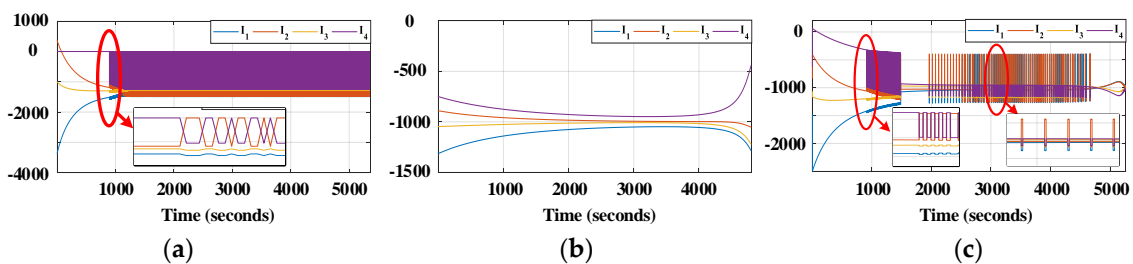
**Figure 12.** Hardware in the loop (HIL) simulation of charging mode for 2S4P configuration–SOC of branches: (a) SOC-based sequencing method; (b) fixed-resistor method; (c) proposed method.



**Figure 13.** HIL simulation of charging mode for 2S4P configuration–branch currents: (a) SOC-based sequencing method; (b) fixed-resistor method; (c) proposed method.



**Figure 14.** HIL simulation of discharging mode for 2S4P configuration–SOC of branches: (a) SOC-based sequencing method; (b) fixed-resistor method; (c) proposed method.



**Figure 15.** HIL simulation of discharging mode for 2S4P configuration–branch currents: (a) SOC-based sequencing method; (b) fixed-resistor method; (c) proposed method.

Power losses in the balancing systems can be decomposed into two different factors: the external power loss in the equalizer circuit and the internal power loss inside the battery. The external power losses of both the proposed and the SOC-sequencing method are calculated by (19) while it is calculated by (20) in the conventional fixed-resistor method, where  $I_{m\_rms}$  are the RMS current of the individual branch,  $R$  is the value of the equalization resistor.

$$P_{loss\_external} = \sum_{m=1}^N I_{m\_rms}^2 R \quad (20)$$

Similarly, the total internal power loss of battery is calculated by (21), where  $R_b$  is the internal DC impedance of battery (70 mΩ) which is provided in the datasheet [28].

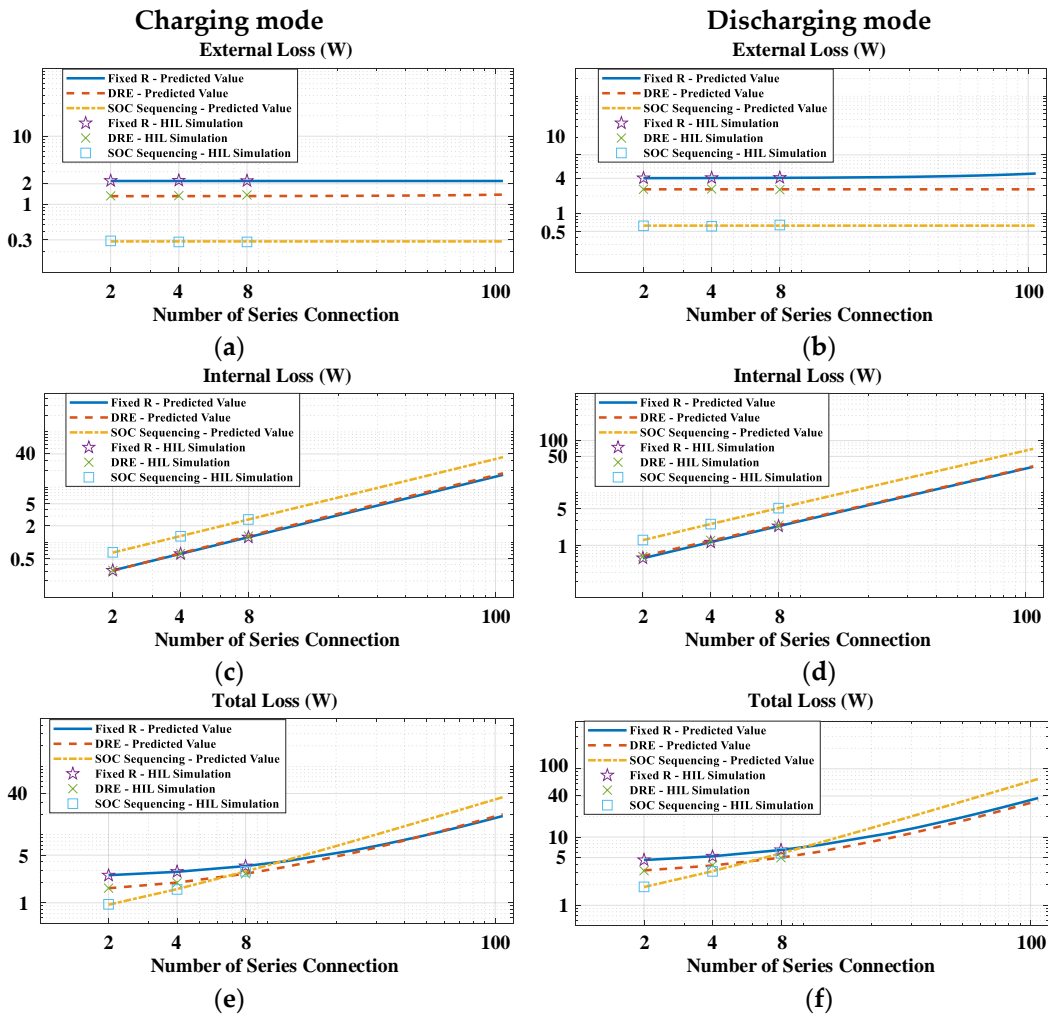
$$P_{loss\_internal} = \sum_{m=1}^N I_{m\_rms}^2 R_b \quad (21)$$

The power losses of the equalizer are compared in Table 4. It shows that the internal loss is proportionally increased by the number of series connections, whereas external loss is almost unchanged. The internal loss of the SOC-sequencing method is always higher than the other by 20% in discharging mode and by 15% in charging mode. In other words, the SOC-sequencing method can reduce the lifetime of the battery system.

**Table 4.** Power loss comparison.

Mode	Performance Index	Fixed-Resistor Method	Proposed Method	SOC Sequencing Method
<b>2S4P Configuration</b>				
Charging	$\sum P_{loss\_external}$ (W)	2.22	1.33	0.29
	$\sum P_{loss\_internal}$ (W)	0.31	0.31	0.66
	Total Loss (W)	2.53	1.64	0.95
Discharging	$\sum P_{loss\_external}$ (W)	4.04	2.6	0.62
	$\sum P_{loss\_internal}$ (W)	0.57	0.61	1.26
	Total Loss (W)	4.61	3.21	1.86
<b>4S4P Configuration</b>				
Charging	$\sum P_{loss\_external}$ (W)	2.24	1.34	0.28
	$\sum P_{loss\_internal}$ (W)	0.62	0.63	1.29
	Total Loss (W)	2.86	1.97	1.57
Discharging	$\sum P_{loss\_external}$ (W)	4.07	2.63	0.61
	$\sum P_{loss\_internal}$ (W)	1.14	1.24	2.54
	Total Loss (W)	5.21	3.87	3.14
<b>8S4P Configuration</b>				
Charging	$\sum P_{loss\_external}$ (W)	2.21	1.37	0.28
	$\sum P_{loss\_internal}$ (W)	1.24	1.30	2.6
	Total Loss (W)	3.45	2.67	2.89
Discharging	$\sum P_{loss\_external}$ (W)	4.14	2.56	0.64
	$\sum P_{loss\_internal}$ (W)	2.32	2.41	5.13
	Total Loss (W)	6.46	4.97	5.77

Because the number of series connections in the energy storage systems (BESS or EV) can be up to hundreds of cells, the curve fitting method is used to predict the power losses of proposed and conventional methods in larger battery configurations from the HIL simulation results. The power losses (external, internal, and total loss) based on HIL simulations and the predicted value are illustrated in the log–log curve in Figure 16. Although the external loss of the SOC-sequencing method is lower than the other methods, its total loss is dominated by the rapidly increasing internal loss. Therefore, when the number of series connections becomes larger, the proposed equalizer becomes more efficient than the SOC-sequencing method. When both total loss and equalization performance are considered together, the proposed equalizer becomes a promising method for parallel battery configuration with many series-connected cells.



**Figure 16.** Predicted power loss in: (a) charging mode—external loss; (b) discharging mode—external loss; (c) charging mode—internal loss; (d) discharging mode—internal loss; (e) charging mode—total loss; (f) discharging mode—total loss.

## 5. Conclusions

This paper proposes a novel dynamic resistance equalizer for parallel-connected battery configurations. Based on the SOC status of battery cells, the switches are controlled to modulate the impedance of the parallel branches while adjusting the branch current. The experimental results show that the cell inconsistency issue in the parallel battery configuration is obviously mitigated, which helps make the parallel-connected battery safer with a prolonged lifetime. The power loss analysis based on HIL simulations also shows that the proposed method is effective, especially for a parallel battery system with many series-connected cells in view of both equalization performance and power loss. Therefore, the proposed method is expected to be suitable for applications such as EV or SL-BESS.

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