High-Speed Battery SOC Adjustment Algorithm utilizing Bi-directional Cell Balancers in Coordination with Pack Charger

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ABSTRACT

In the second-life EV's batteries, the battery pack SOC adjustment process is essential both for maintenance and shipping. For this system, the conventional balancing methods are unsuitable for calibration purposes due to their non-optimized speed and lack of freedom in target SOC. This paper proposes a high-speed SOC adjustment algorithm for a bidirectional equalizer-integrated charger. The proposed algorithm can coordinate the charging/discharging process with the equalizing process at the same time. The proposed algorithm is verified by PSIM for 20 series-connected battery cells. The simulation results show a high equalization performance, and the total operating time is significantly reduced, compared to the conventional methods. Besides, the computation time of the proposed method is low, and thus, it is easy to implement for a large number of series connections just by a single embedded system-based BMS.

Keywords: Bi-directional equalizer, SOC adjustment, battery pack maintenance, Integrated Charging-equalizing.

1. INTRODUCTION

In the battery pack maintenance and shipping application, the SOC of the battery requires to be adjusted and be sustained at a certain level. However, battery SOC adjustment without a cell-equalizer is not safe due to cell inconsistency. The inconsistency becomes more serious when the series connection increases, especially in electric vehicles (EVs) where hundreds of cells are connected in series and parallel. Therefore, an equalizer is required to ensure that performances of battery cells are uniform. Generally, the equalization and the charging processes are separately executed.

In conventional studies, fast pack charging algorithms are studied without considering cell balancing [1-2]. High-speed cell balancing is only considered [3-4]. In fact, there is a lack of study that considers the coordinated operation for both the pack-charger and the cell-equalizer. Thus, the total processing time of the SOC adjustment includes equalizing and adjusting the SOC level of the cells to the target level.

This paper proposes a high-speed battery SOC adjustment algorithm utilizing a bi-directional cell-equalizer in coordination with a pack charger. This study is an improvement of [5] that replaces the unidirectional cell-equalizer with a bi-directional converter in order to accelerate time. The operation principle is described in Section 2, simulation results are shown in Section 3, and the conclusion is made in Section 4.

2. PROPOSED METHOD

The configuration of the proposed system includes a pack charger and a bi-directional equalizer, which is connected to the battery pack through a switch-matrix as Fig. 1. The pack charger charges or discharges the whole battery pack by a constant current, I_c, in order to adjust the SOC level of the cells to the target SOC level. Observe that the polarity of I_c demonstrates the direction of the process (it is positive in the charging process or negative in the discharging process). Besides, the bi-directional equalizer is operated to effectively perform the SOC equalization between the cells. By using the bi-directional equalizer, the energy is either regenerated from the battery pack to the cells or from the cell to the pack, respectively. Because the equalization is assigned only once for one cell, the number of equalization steps directly corresponds to the number of cells in the pack. While the battery cell is charged/discharged by a constant current, I_{bal}, the whole battery pack is discharged/charged by a corresponding constant current, I_p. By determining the operating time of each step, the total operation time of the SOC adjustment is determined.

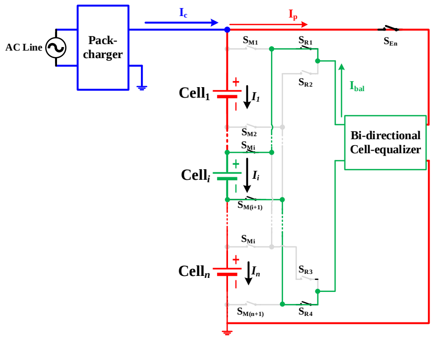
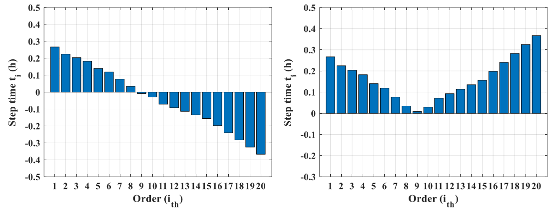


***Fig. 1**: Configuration of the system*



(a) *(b)*

***Fig. 2**: Processing time pattern: (a) the pattern of time for each step; (b) actual processing step time.*

According to [5], the amount of changed SOC after a period, $t - t_0$, is determined as

$$SOC(t) - SOC(t_0) = \frac{(t - t_0)I}{Q} \tag{1}$$

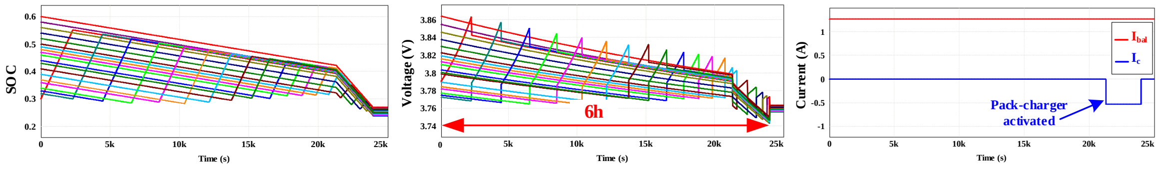
where $SOC(t)$ is the state of charge of the cell at time, t; t_0 represents the initial time of the process; Q is the available capacity of cells and is regarded as identical for all cells; I is the current pass through the cell. Therefore, the processing time of pack-charger, t_c, is expressed as

$$t_c = \frac{(SOC_{targ} - SOC_{init\_avg} + SOC_L)Q}{I_c} \tag{2}$$

where SOC_{targ} is the target SOC level at end of the process; SOC_L is the equivalent SOC loss of the cells; SOC_{int_avg} is the initial average SOC level of the cells. Finally, the processing time for each step, t_i, is expressed as

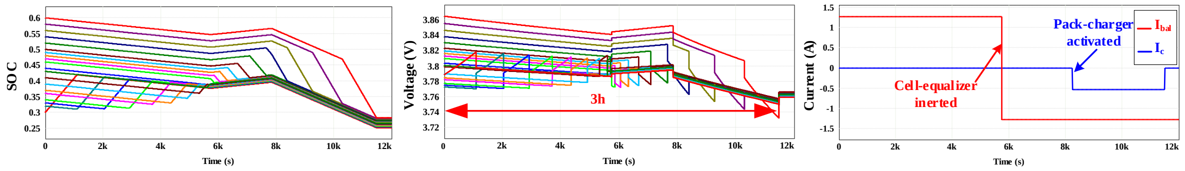
$$t_i = \frac{[SOC_{init\_avg} - SOC_i(t_0) - SOC_L]Q + t_{sum}I_p}{I_{bal}} \tag{3}$$

where i is the order of equalization steps during the process, and t_{sum} is the sum of the processing time expressed as



(a) (b) (c)

***Fig. 3**: Simulation results of the conventional method: (a) SOC profiles; (b) voltage profiles; (c) current profiles of I_{bal} and I_c.*



(a) (b) (c)

***Fig. 4**: Simulation results of the proposed method: (a) SOC profiles; (b) voltage profiles; (c) current profiles of I_{bal} and I_c.*

$$t_{sum} = \sum_{i=1}^{n} t_i . \qquad (4)$$

By choosing the value of t_{sum}, it is possible to optimize and minimize the total processing time. Fig. 2(a) shows the operating time pattern of each step when t_{sum} equals zero. With the operating time is positive, the equalizer operates in pack-to-cell mode. In contrast, the equalizer operates in the cell-to-pack mode when the operating time is negative. Therefore, by inverting the direction of the cell-equalizer current, the actual processing step time is presented as in Fig. 2(b). After the end of the operation of the pack-charger and the cell-equalizer, the SOC level of the cells is equalized at the target SOC point.

3. SIMULATION RESULT

To verify the proposed method, the simulations are implemented on PSIM for a battery string consisting of 20 cells (18650 3.6V/ 2600mA). The conventional method in [5] and proposed method are implemented under the same conditions as shown in Table 1. The initial SOC levels of the cells are varied between 30% and 60% while the target SOC point is fixed to 25%.

The simulation results of the conventional and the proposed methods are illustrated in Fig. 3 and Fig. 4, respectively. Both conventional and proposed methods can adjust and equalize the SOCs and voltages of the cells within 3% and 15mV, respectively. However, the proposed method only requires 3.1h, compared to 6h of the conventional method. The SOC and voltage profiles in Fig. 3(a), Fig. 3(b), Fig. 4(a), and Fig. 4(b) reflect the difference between two control strategies. While the conventional method only charges the cells one by one and the pack-charger discharge the whole pack, the proposed method charges lower SOC level cells and discharges higher ones. The current profiles in Fig. 3(c) and Fig. 4(c) also illustrate the control strategies.

During the test, SOC loss inside the battery is calculated to assess the effectiveness of the conventional and proposed methods. By reducing the operating time, SOC loss of the proposed method is reduced to 50% of SOC loss in the conventional method.

4. CONCLUSION

This paper proposes a high-speed battery SOC adjustment algorithm utilizing a bi-directional cell equalizer in coordination with a pack charger. The proposed method coordinates the operation of the pack charger and the bidirectional equalizer. The SOC levels of the cells can be adjusted to a target level while the equalization status of the cells is maintained. The proposed method can achieve a high equalization performance while the total operating time is significantly reduced. Besides, the SOC loss of the proposed method is only 50% of SOC loss in the conventional method. Furthermore, because the calculation time of the proposed method is very fast, it can be implemented by a simple embedded system-based BMS

Table 1: ***System configuration***

SOC target	25%
Configuration	*20S1P* (18650-3.6*V*/2.9*Ah*)
$\lvert I_c \rvert$	0.53*A*
$\lvert I_{bal} \rvert$	1.27*A*
$\lvert I_p \rvert$	0.1*A*
Efficiency of cell-equalizer	0.8

ACKNOWLEDGMENTS

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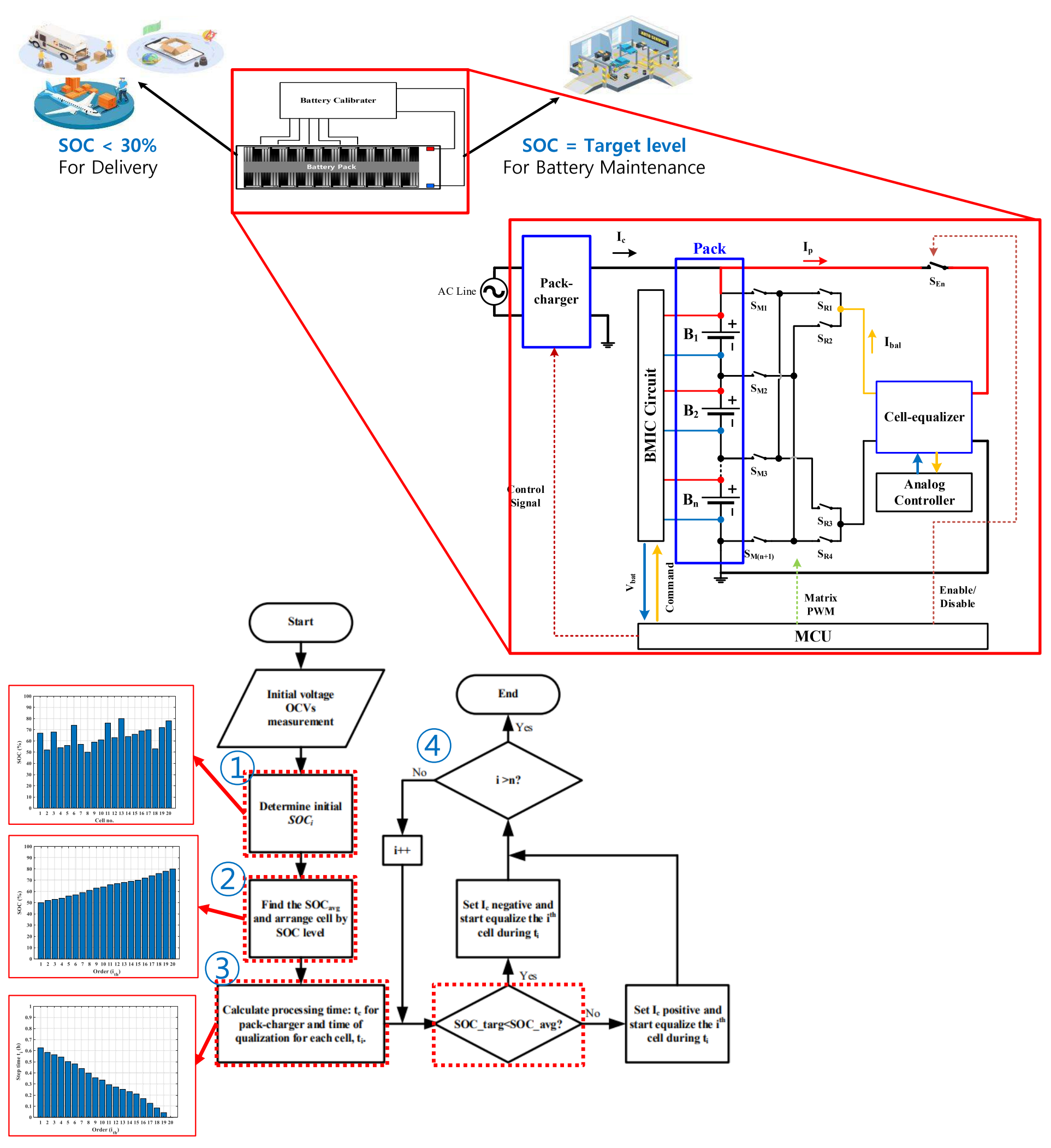
Summary

- Battery calibrator (including a cell-equalizer and a pack-charger) can achieve:
  - SOC set point freedom
  - Optimal switching (low energy loss)
  - Low computational burden
- Conventional methods have an inflexible and a low-speed operation.
- Proposed method adopts a **bi-directional converter** to has
  - All advantages of conventional method
  - Twice lower processing time than conventional method

Research Motivation



- SOC level must be adjusted to under 30% before the shipping.
- SOC level is set to **arbitrary level** for the maintenance.
- **Control flowchart:**

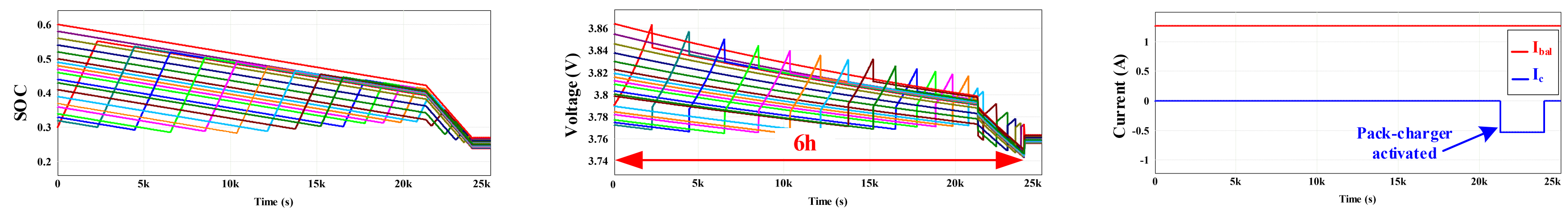
① SOCs are estimated by OCV-SOC look-up table.

② SOC levels are sorted in ascending order.

③ Operating times are obtained by charge transfer calculation.

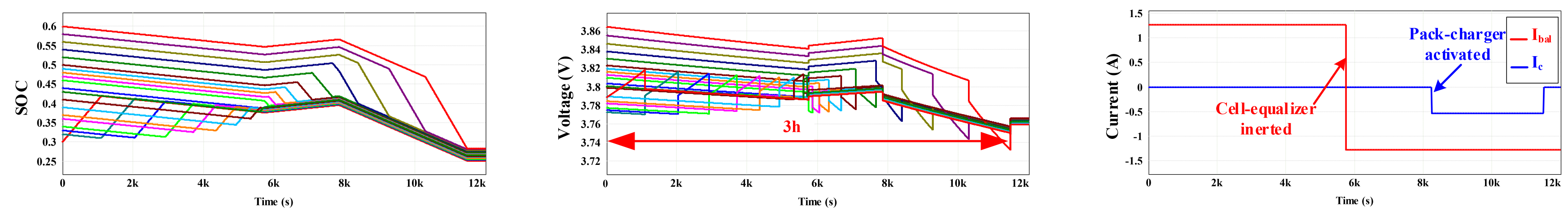
④ Switching patterns are decided.

Verification



(a) SOC profiles. *(b) Voltage profiles* *(c) Current profiles of I_{bal} and I_c*

Simulation results of the conventional method



(a) SOC profiles. *(b) Voltage profiles* *(c) Current profiles of I_{bal} and I_c*

Simulation results of the proposed method

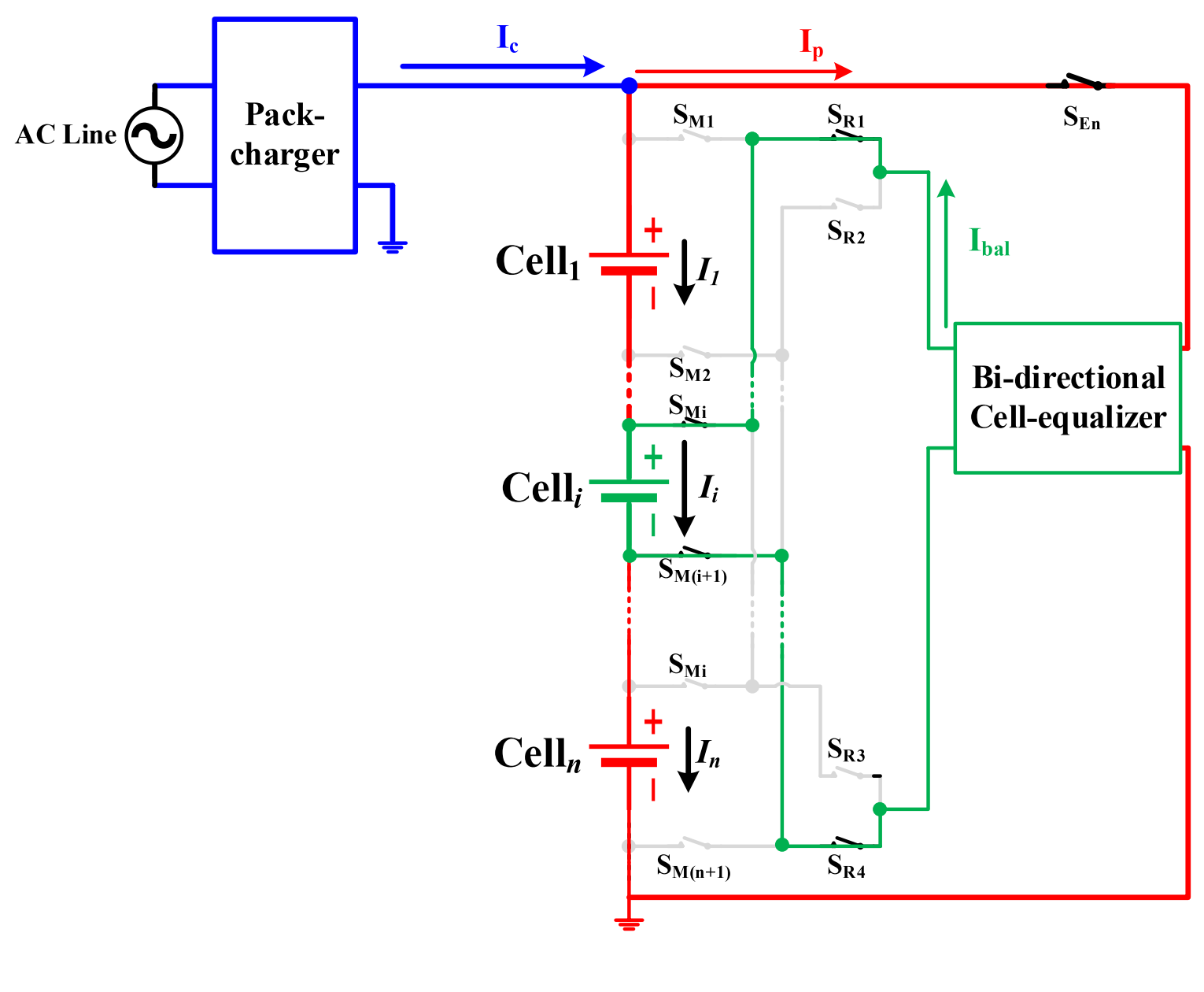
- Initial SOC levels of the cells are varied **between 30% and 60%.**
- Proposed method **charges** the **lower SOC level cells** and **discharges** the **higher ones.**
- SOCs and voltages of the cells are equalized **within 3% and 15mV, respectively**.
- **Processing time** in proposed method is just **a half** of that in conventional method.

Table 1: ***System configuration***

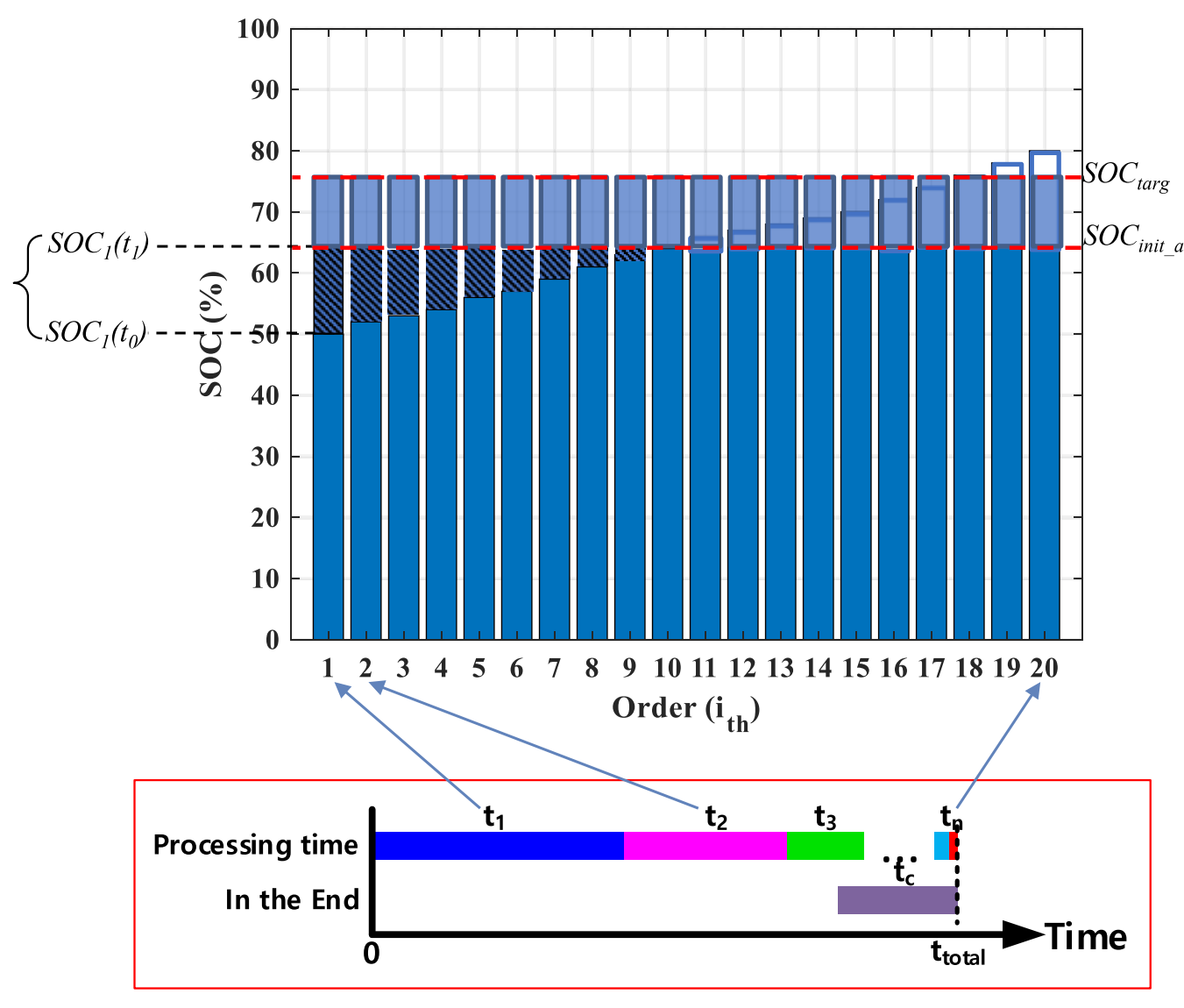
SOC target	25%
Configuration	20S1P (18650-3.6V/2.9Ah)
$\lvert I_c \rvert$	0.53A
$\lvert I_{bal} \rvert$	1.27A
$\lvert I_p \rvert$	0.1A
Efficiency of cell-equalizer	0.8

Proposed Method

- **Proposed Configuration**



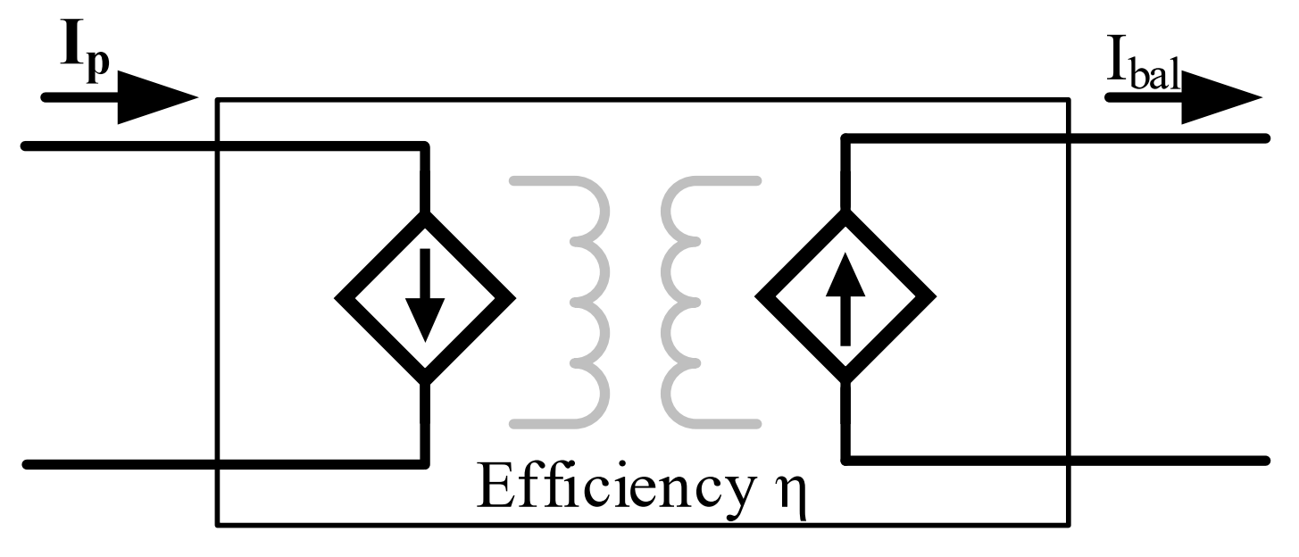
Proposed circuit structure.



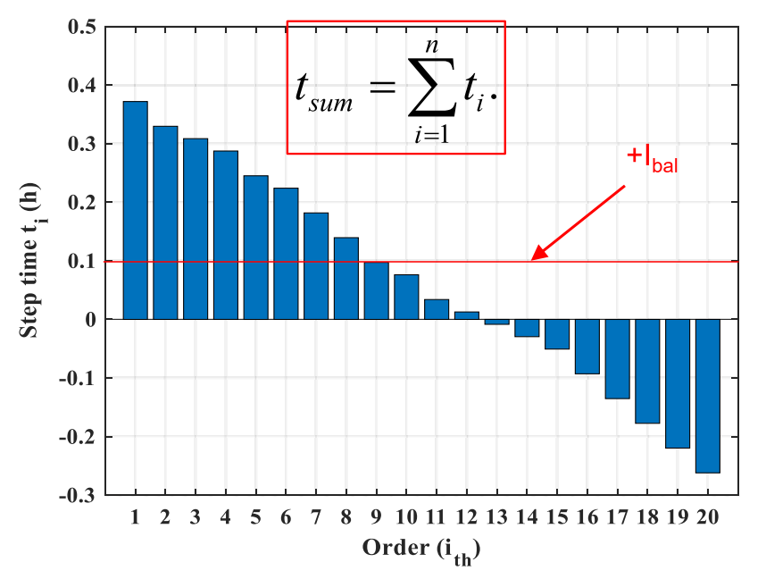
Energy transfer description

- Utilize the existing **switch-matrix network** of the conventional method.
- Replace the **uni-directional cell-equalizer** by a **bi-directional cell-equalizer**.
- Calculate the **processing time of individual cell** based on the **charge transfer operation analysis**.

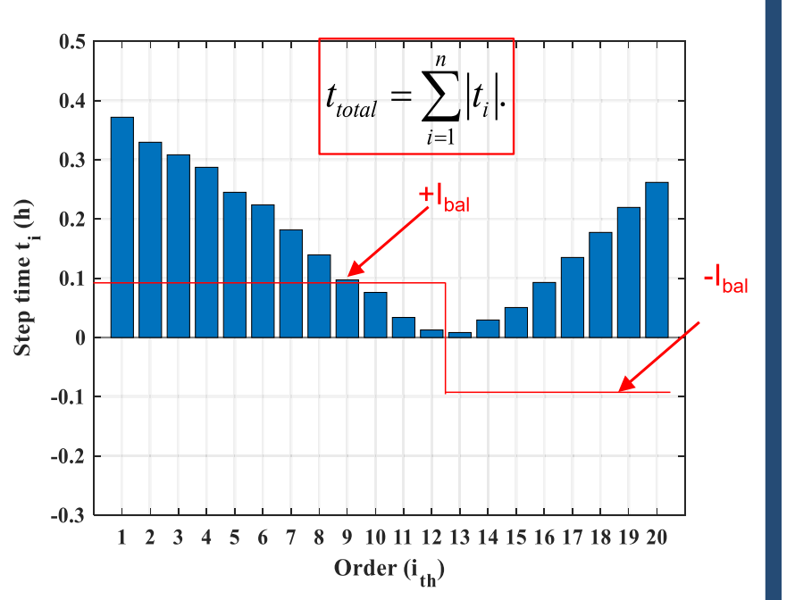
- **Theoretical analysis of the proposed methods:**



Cell-equalizer



Pattern of time for each step



Actual processing step time

- Denote I_{bal} is the **equalization current**, I_p is the **operation current of the pack-charger**

$$I_p = \frac{v_i . I_{bal}}{\eta . v_{pack}}$$

- **Equivalent SOC loss of cells**

$$SOC_L = \frac{\left(\frac{1}{\eta} - 1\right) \sum_{i=1}^{n} \frac{v_i}{n} I_{bal} t_{total}}{v_{pack} Q_{nom}}$$

- **Amount of changed-SOC level** after a period **(t - t$_0$)**

$$SOC(t) - SOC(t_0) = \frac{(t - t_0) I}{Q}$$

- **Processing time of pack-charger t_c**

$$t_c = \frac{(SOC_{targ} - SOC_{init\_avg} + SOC_L) Q}{I_c}$$

- **Average value of initial SOC level of cells**

$$SOC_{init\_avg} = \frac{\sum_{i=1}^{n} SOC_i(t_0)}{n}$$

- **Processing time of individual cell t_i**

$$t_i = \frac{[SOC_{init\_avg} - SOC_i(t_0) - SOC_L] Q + t_{sum} I_p}{I_{bal}}$$

With $t_{sum} = \sum_{i=1}^{n} t_i$.

- **Sign of processing time** illustrates **charging/discharging behaviour** applying on each step.
- If the **processing time** is **positive**, the calibrator operates in **pack-to-cell mode**.
- By choosing the value of t_{sum}, it is possible to minimize the total processing time.
- Calibrator operates in **the cell-to-pack mode** when the **operating time** is **negative**.

Conclusions

- A **high-speed battery SOC adjustment algorithm** utilizing **a bi-directional cell equalizer in coordination with a pack charger** is proposed.
- **SOC-levels of the cells** can be **adjusted to a target level** while the equalization status of the cells is maintained.
- **High equalization performance** is achieved while the **processing time and energy loss** are **just a half** of that in the conventional method.
- **Proposed method** can be implemented by **a simple embedded system-based BMS** due to **low computation burden.**