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ORIGINAL ARTICLE

Tapped-inductor inverter/rectifier structure with integrated matching network for capacitive power transfer systems

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Abstract
In a capacitive wireless power transfer (CPT) system, a high-frequency (HF) inverter and a matching network are separately considered for system design, and front-end or back-end DC-DC converters are usually added for voltage regulation. Buck-boost inverters and tapped inductors are combined to create a family of inverters, which merges the functions of the HF inverter and the input impedance matching network. Through the duality of inverters and rectifiers, a family of rectifiers is also proposed, providing the output impedance matching function. The front-end or back-end DC-DC converter stage is eliminated due to the wide voltage gain voltage feature of the proposed topology. In this study, the operation principle and gain properties of the proposed system are investigated for both constant current and constant voltage output modes. A prototype of a 100 W CPT system was designed and implemented to verify the feasibility of the proposed topology. Experimental results agree well with the theoretical analysis. The proposed CPT system can reduce the coupler voltage stress by 1.7 times compared with the conventional double-sided LC structure at the same transferred power and can also provide zero voltage switching operation.

Keywords Asymmetric half-bridge · Capacitive power transfer · Tapped inductor · Matching network

1 Introduction

Wireless power transfer technology has gained widespread application in various fields, including electric vehicles, wireless sensor networks, light-emitting diode (LED) lighting, and biomedical applications [1]. The dominant method for such power transfer has traditionally been inductive wireless power transfer (IPT) [1]. However, capacitive wireless power transfer (CPT) has recently gained attention as a promising alternative solution to replace IPT systems [2]. CPT employs electric fields rather than magnetic fields to transmit energy through metallic barriers, leading to minimal power losses [2]. Notably, CPT offers significant advantages in terms of cost reduction and reduced weight of the energy coupler structure [3].

A general two-stage CPT system architecture is shown in Fig. 1. The high-frequency (HF) inverter is used to produce AC voltage. The input match network (IMN) and the output matching network (OMN) are used as compensation circuits. The rectifier circuit is used to convert AC voltage to DC voltage. The front-end or back-end DC-DC converter is mostly used to regulate the input or output voltage [4]. The capacitance of a CPT coupler is usually from a hundred picofarads to a few nanofarads due to the naturally low permittivity of vacuum and air. This condition results in high impedance of a CPT coupler, thus generating high voltage stress in the coupler, which is the most significant limitation of the CPT system. According to the IEEE standard for safety level with respect to human exposure to electric fields, the electric field strength should be limited to 614 V/m with a frequency range from 0.1 to 1.34 MHz [5]. The literature presents two common solutions to reduce coupler voltage stress. First, the switching frequency is increased to reduce the impedance of the capacitive coupler. However, the switching frequency could not be easily increased beyond a few megahertz because of the limited switching characteristics of power semiconductor devices. Second, the IMN at the primary is utilized to boost the voltage before the capacitive coupler to reduce the current through the capacitive coupler. This voltage is then reduced back to the output

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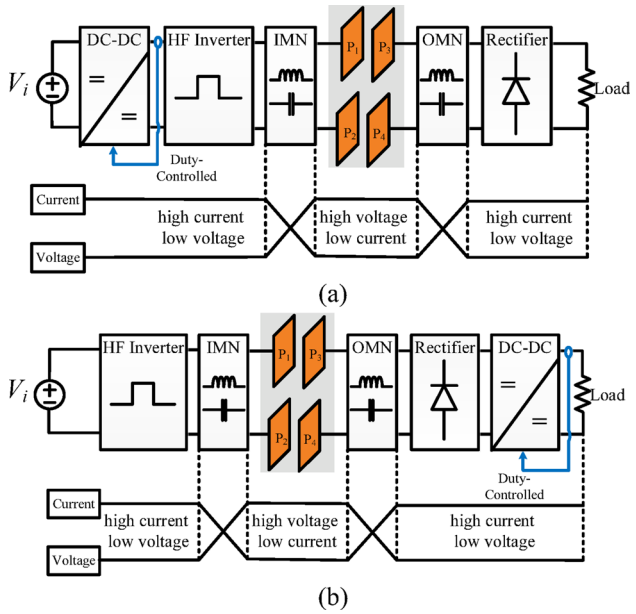

Fig. 1 Conventional two-stage CPT system architecture with: **a** front-end DC-DC converter; **b** back-end DC-DC converter

voltage by OMN as shown in Fig. 1, which is considered a more realistic way than the first one.

Various types of matching networks have been proposed in the literature to accommodate the second solution, such as L, LC, LCL, LCLC, and double-sided transformers. The advantage of the series L-compensation is its simplicity [6]. However, it still requires the switching frequency to be in the MHz range to provide sufficient power capability. The advantage of the double-sided LC compensation circuit is its feasibility in long-distance applications [7]. The LCL compensation is the combination of L and LC [8]. Double-side LCLC can maintain a high coupling coefficient for efficiency consideration. However, the complex design of the double-sided LCLC compensating circuit is a disadvantage [9] because the circuit has eight passive components. Furthermore, adding more components to the circuit can result in additional power losses, lowering system efficiency. As demonstrated in [10], the double-sided transformer compensation network can also be utilized for impedance transformation. However, the size of the system increases because of the bulkiness of the transformer. Other high-order compensation networks were proposed in [11], increasing complexity and component count. A special shape of the compensation network has been proposed in the literature [12–15]. The drawbacks of conventional compensations include low voltage gain (L, CL), design complexity, component count (LCLC, double-sided LCLC), and bulkiness (double-sided transformer).

Adopting the high-gain HF inverter/rectifier is advisable to reduce the burden of matching network. However, the half-bridge and full-bridge topologies are most commonly used, and those kinds of buck-type inverters cannot afford a wide control range. Thus, front-end or back-end DC-DC converters are usually added for voltage regulation, as shown in Fig. 1 [4]. However, the multistage system becomes costly and complex. The buck-boost inverter has been proposed to overcome this issue [16, 17]. However, the output voltage gain of the buck-boost inverter is limited by the voltage stress of the main power switches. Therefore, the buck-boost topology is not enough to obtain the voltage-boosting required for the CPT system.

The literature reports that the tapped-inductor topology can extend the control range and increase the voltage gain of the converter [18]. Therefore, combining the buck-boost inverter and tapped inductor creates a new family of inverters with the integrated impedance matching network. Through the duality of the inverter and the rectifier, a new family of rectifiers can also be proposed with the integrated impedance matching network. The complex compensation network and the additional DC-DC converter can be eliminated. In other words, the function of the compensation network and the DC-DC converter can be merged into a single-stage HF inverter located on the primary side, and the function of the compensation network and the rectifier can be merged into a single rectifier on the secondary side. The main contributions of this paper are summarized as follows:

1. A family of CPT inverter topologies that integrate the inverter and the impedance matching network by combining buck-boost operation with a tapped-inductor structure.
2. A family of rectifier topologies that provide impedance matching on the receiver side without additional matching networks.
3. Elimination of front-end or back-end DC–DC converters owing to the wide voltage gain characteristic of the proposed high-frequency inverter, enabling both CC and CV operation.

The rest of this paper is structured as follows: In Sect. 2, the proposed family of tapped-inductor inverters/rectifiers with an integrated matching network for CPT systems is derived. In Sect. 3, the working principle is presented. Equivalent circuit model analysis of the tapped-inductor CPT system for CC-CV operation is presented in Sect. 4. The feasibility of the proposed family topology is verified in Sect. 5. Finally, the results of the study are summarized in Sect. 6.

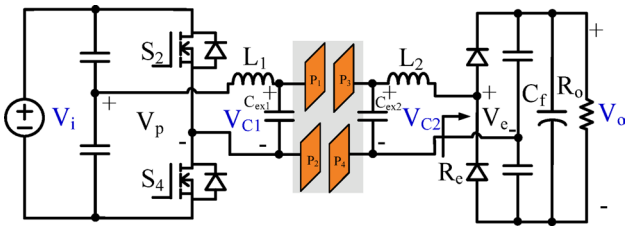

Fig. 2 Conventional CPT systems double-sided LC compensation with half-bridge inverter and half-wave rectifier

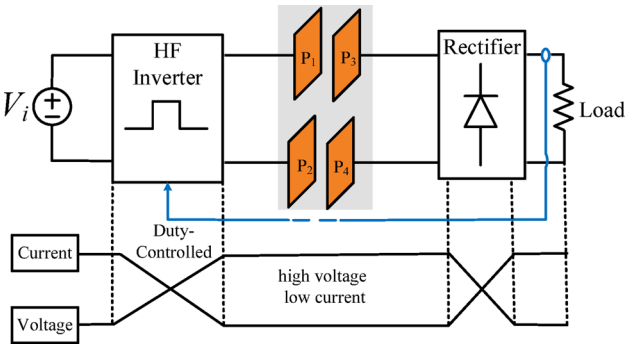

Fig. 3 Proposed tapped-inductor inverter/rectifier integrated matching network structure for the CPT system

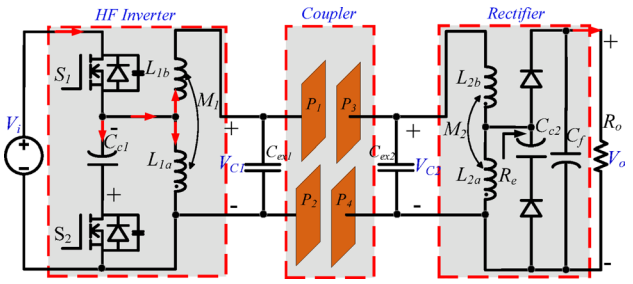

Fig. 4 Proposed tapped-inductor inverter/rectifier system for the CPT system

2 Tapped-inductor inverter/rectifier with integrated matching network structure

2.1 Problem definition

The capacitive coupler of the CPT system containing four plates, P_1–P_4, as shown in Fig. 2, is used for the analysis. In the CPT system, the capacitance of a capacitive coupler is usually from a hundred picofarads to a few nanofarads due to the naturally low permittivity of air. This condition results in high impedance of a CPT coupler, which introduces high voltage stress in the coupler.

This issue is most commonly solved by placing the reactive component on both sides of the capacitive couplers to step up the voltage before and step it down after the capacitive coupler. For that purpose, double-sided LC compensation is most common due to the simplicity and low component count, as shown in Fig. 2, where C_{ex1} and C_{ex2} are external capacitors [9, 19]. For low- and medium-power applications, half-bridge inverter and half-wave rectifiers are frequently used in CPT systems [12]. By the fundamental harmonic approximation, the output voltage of the inverter and the input voltage of the rectifier are given by

$$V_p = \frac{\sqrt{2}V_i}{\pi}\sin\left(\frac{\pi(2D-1)}{2}\right), V_e = \frac{\sqrt{2}}{\pi}V_o \tag{1}$$

where V_i is the DC input voltage of the HF inverter, V_e is the AC input voltage of the rectifier, V_o is the DC output voltage at load resistance R_o, and D is the duty cycle of the half-bridge inverter. However, this kind of buck-type inverter cannot afford the wide control range. Thus, front-end or back-end DC-DC converters are usually added for voltage regulation. The voltage before and after the capacitive coupler is given by

$$V_{C1} = V_p + V_{L1} \tag{2}$$

$$V_{C2} = V_e + V_{L2} \tag{3}$$

where V_{L1} and V_{L2} are the voltage applied to the inductor L_1 and L_2, respectively.

In this paper, the inverter, resonant tank, and rectifier are considered together to boost the voltage gain, thereby further reducing the voltage stress on the capacitive coupler. Merging the functions of the IMN and the front-end DC–DC converter into an HF inverter, and the OMN and the back-end DC–DC converter into a rectifier can simplify the overall system, as shown in Fig. 3.

2.2 Circuit topologies

The novel inverter/rectifier configuration to achieve such functionality is presented in Fig. 4, featuring two switches, S_1 and S_2, which are controlled by asymmetrical pulse-width-modulated gating pulses. The proposed configuration is formed by the combination of a clamp capacitor, C_{c1}, and a tapped inductor, L_1. Tapped inductor L_1 contains inductors L_{1a} and L_{1b}, which are used for voltage boost and compensation for the capacitive coupler. The tapped-inductor rectifier is also employed in the secondary side to restore the voltage. Therefore, the proposed configuration with a double-sided tapped inductor consists of a high-gain inverter with compensation on the primary side and a high-gain rectifier with compensation on the secondary side, as shown in Fig. 4. The various tapped-inductor inverter topologies can be derived as shown in Fig. 5, where the voltage V_p can be boosted by the tapped inductor.

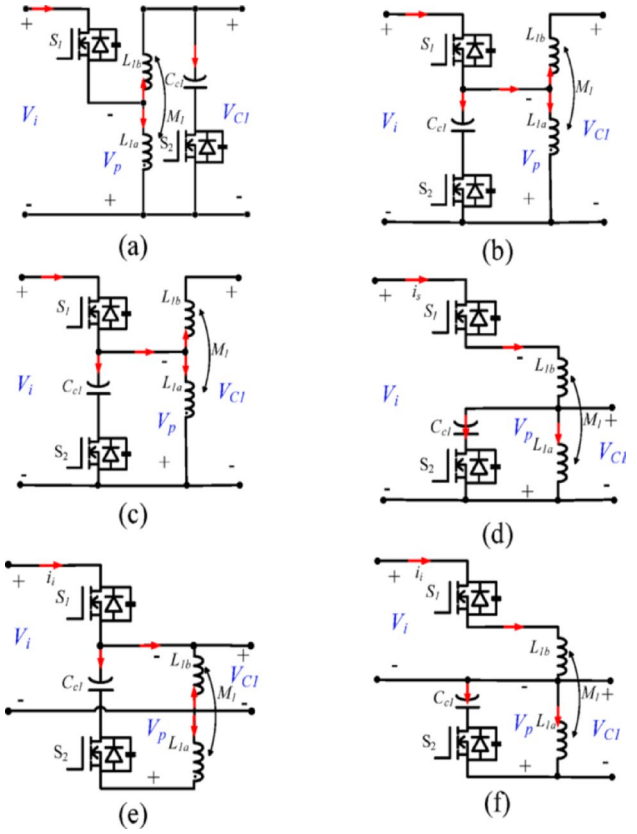

Fig. 5 Family of tapped-inductor inverter with integrated matching network: **a** switch-to-tap; **b** switch and capacitor-to-tap; **c** output-to-tap; **d** output and capacitor-to-tap; **e** ground-to-tap; **f** ground and capacitor-to-tap

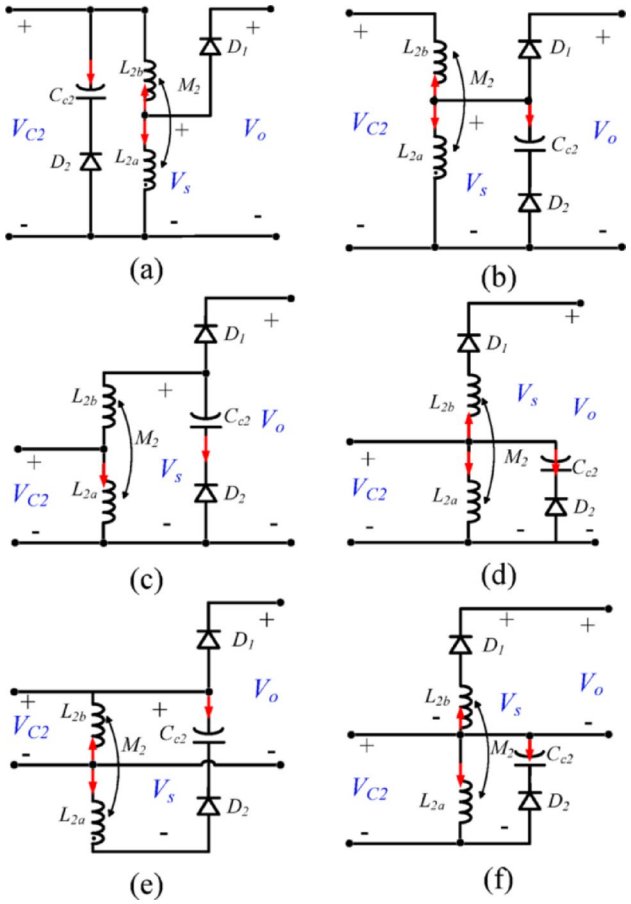

Fig. 6 Family of tapped-inductor rectifier with integrated matching network: **a** switch-to-tap; **b** switch and capacitor-to-tap; **c** output-to-tap; **d** output and capacitor-to-tap; **e** ground-to-tap; **f** ground and capacitor-to-tap

The family of tapped-inductor inverter with integrated matching network is derived by changing the configuration of topology in a similar manner as the tapped-inductor DC-DC converters [18], as shown in Fig. 5. The newly derived tapped-inductor inverter structure with integrated matching network for the CPT system can be categorized in six ways: switch-to-tap in Fig. 5a; switch and capacitor-to-tap in Fig.

5b; output-to-tap in Fig. 5c; output and capacitor-to-tap in Fig. 5d; ground-to-tap in Fig. 5e; ground and capacitor-to-tap in Fig. 5e. Through the duality between the inverter and the rectifier, six versions of the rectifier can also be derived as shown in Fig. 6.

3 Analysis of the proposed circuit

The topology shown in Fig. 4 is used as an example to describe the operation principles of the proposed topologies, where the inverter in Fig. 5b and the rectifier in Fig. 6b are integrated as a building block.

Before the operation and characteristics of the proposed system topology are illustrated, the following assumptions are made:

1) The clamp capacitor voltages in both the inverter and the rectifier are considered constant due to a sufficiently large capacitance of C_{c1} and C_{c2} .
2) The two switches, S_1 and S_2, have identical characteristics.
3) All parasitic components except the output capacitance, C_{oss1} and C_{oss2}, of the switches are neglected.
4) The quality factor of the resonant tank is high enough to make a sinusoidal current assumption.
5) The output voltage is constant due to a sufficiently large C_f.

3.1 Operation analysis

The winding ratio of the tapped-inductor is a function of the inductances and is defined as

$$N_1 = 1 + \frac{M_1}{L_{1a}}, N_2 = 1 + \frac{M_2}{L_{2a}} \tag{4}$$

where M_1 is the mutual inductance between L_{1a} and L_{1b} for the primary tapped inductor L_1, and M_2 is the mutual inductance between L_{2a} and L_{2b} for the secondary tapped inductor L_2. The key operation waveforms of the proposed system are shown in Fig. 7. The operation of the proposed topology can be divided into four stages.

Stage 1 [$-\pi D \le \omega t < \pi D$]: During this time interval, switch S_1 is on and switch S_2 is off, as shown in Fig. 8a. The primary voltage, v_p, is clamped to the input voltage, V_i, and the drain-to-source voltage of the switch S_2 is clamped as indicated in (5). The current in inductor L_{1a} is given by (6).

$$v_{DS2}(\omega t) = \frac{V_i}{1-D} \tag{5}$$

$$i_{L2b}(\omega t) = \begin{array}{l} \frac{1}{\omega L_{2b}}[\omega M_2 I_{s,\max}(\cos(\omega t+\theta) - \cos(\theta - \pi D_e)) \\ -V_L(\omega t + \pi D_e)] + i_{L2b}(-\pi D_e) \end{array} \tag{6}$$

where D is the duty cycle. When the polarity of the input current of the rectifier changes from negative to positive, the diode D_1 conducts.

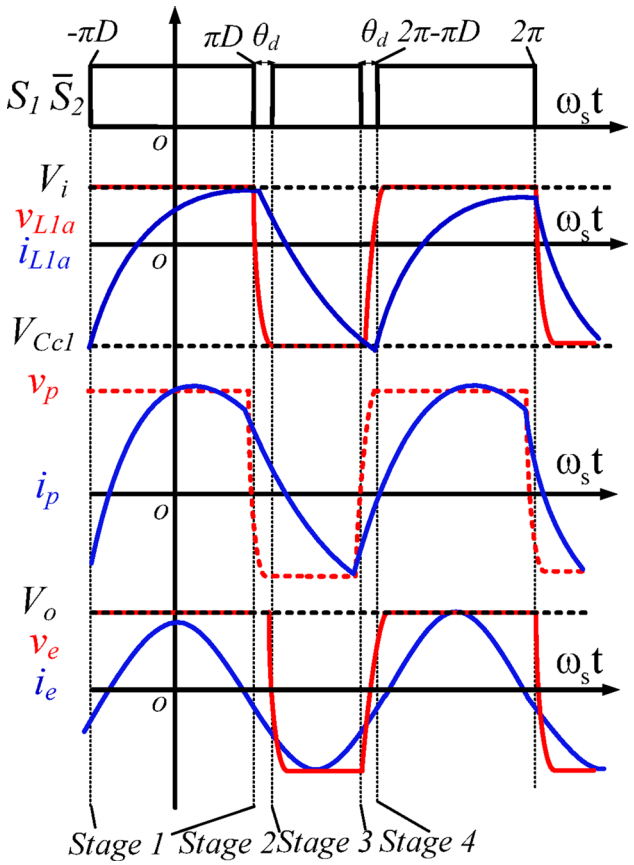

Fig. 7 Key operation waveforms of the proposed tapped-inductor inverter/rectifier with integrated matching network for the CPT system

In rectifier, this stage begins when the voltage induced across the secondary winding L_{2b} becomes positive and exceeds the output voltage V_o, thereby forward-biasing the diode D_1. A resonant current commences flowing from L_{2b} through D_1 to load. This current rises from zero to a peak and then, due to the natural resonance, decays back to zero. The diode D_1 continues to conduct as long as this current is positive. When the resonant current naturally terminates and reaches 0 A, diode D_1 turns off. This constitutes the zero-current switching (ZCS) turn-off event.

Stage 2 [$\pi D \le \omega t < \pi D + \theta_d$]: During the dead time interval θ_d when both switches S_1 and S_2 are off, as shown in Fig. 8b, zero-voltage switching (ZVS) of S_2 is achieved by the energy stored in the tapped inductor L_1, which simultaneously charges and discharges the parasitic output capacitors of switches S_2 and S_1, respectively. The diode D_1 still conducts due to phase lagging of the diode current compared with the diode voltage for the soft switching.

In the rectifier, this stage begins when the voltage induced across the secondary winding L_{2a}, V_e, becomes sufficiently positive to forward-bias the diode D_2. A resonant current, analogous to Stage 1, commences. This current flows from the negative output, through D_2, and into the resonant tank. As in Stage 1, this current is quasi-sinusoidal, rising from zero and naturally decaying back to zero. When the current reaches 0 A, diode D_2 turns off, achieving ZCS.

Stage 3 [$\pi D + \theta_d \le \omega t < 2\pi - \pi D - \theta_d$]: During this time interval, switch S_2 is on and switch S_1 is off, as shown in Fig. 8c. The parasitic output capacitor of S_2 is already completely discharged at $\omega t = \pi D + \theta_d$. Thus, S_2 activates in a ZVS condition, the switch S_1 drain-to-source voltage is clamped as indicated by (7), and the currents flowing in L_{1a}, L_{1b}, and C_{cc1} are added up to zero as indicated by (8).

$$v_{DS1} = \frac{V_i}{1-D} \tag{7}$$

$$i_{L1a}(\omega t) + i_{L1b}(\omega t) + i_{cc1}(\omega t) = 0 \tag{8}$$

where i_{L1b} and i_{cc1} are the current in the resonant tank and the clamp capacitor, respectively. When the polarity of the rectifier input current i_e changes from negative to positive, the diode D_2 conducts.

In the rectifier, this stage begins when the voltage induced across the secondary winding L_{2a}, V_e, becomes sufficiently positive to forward-bias the diode D_2. A resonant current, analogous to Stage 1, commences. This current flows from the negative output, through D_2, and into the resonant tank. As in Stage 1, this current is quasi-sinusoidal, rising from zero and naturally decaying back to zero. When the current reaches 0 A, diode D_2 turns off, achieving ZCS.

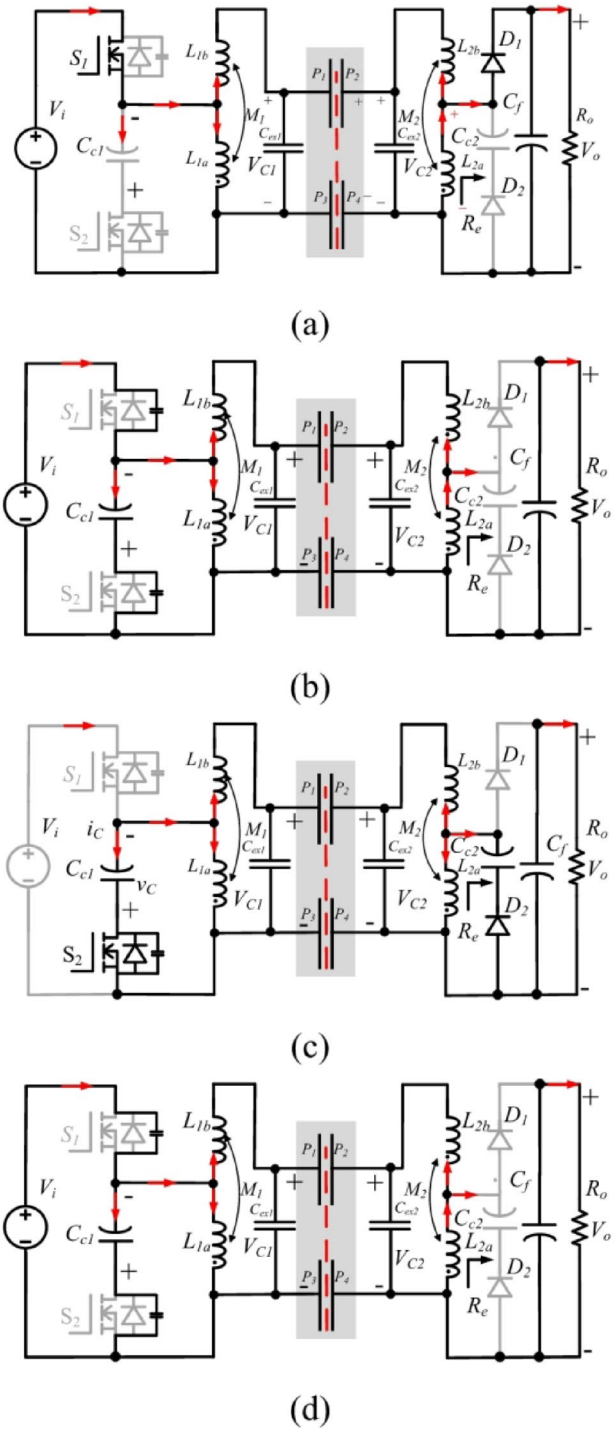

Fig. 8 Operation stages of the proposed topology: **a** Stage 1; **b** Stage 2; **c** Stage 3; **d** Stage 4

Stage 4 [2π- πD – $\theta_d \leq \omega t < 2\pi$- πD]: During this time interval, both switches S_1 and S_2 are off, as shown in Fig. 8d. ZVS of switch S_1 can be achieved by using the energy stored in the inductors L_{1a}, L_{1b} and L_{2b} to charge the parasitic output capacitor of S_1 and discharge the output capacitor of S_2.

In the rectifier, this stage starts when the current through D_2 has just reached zero, and D_2 is now reverse-biased. The induced voltage is swinging back to the positive polarity but has not yet reached the level required to forward-bias D_1. Both diodes remain off. The resonant tank voltage continues to rise until it is sufficient to trigger Stage 1.

On the basis of the operation principles of the proposed topologies, the voltage gain can be derived. With the use of the flux balance condition for L_{1a}, the average voltage of the clamp capacitor, V_{cc1}, and the peak-to-peak current in the inductor L_{1a} can be derived as follows:

$$V_{cc1} = \frac{D}{1-D} V_i \tag{9}$$

and

$$\Delta I_{L1a} = \frac{D}{L_{1a} f_s} V_i. \tag{10}$$

The proposed inverter can be controlled by a pulse width modulation (PWM) gating signal at the switching frequency, f_s. Under the high-quality factor assumption, the primary voltage can be approximated by its fundamental component. The waveform of the primary voltage, V_p, has an even symmetry, as shown in Fig. 7. Thus, the primary voltage is well approximated by

$$V_{p,1} = \frac{\sqrt{2} N_1 \sin \pi D}{\pi (1-D)} V_i. \tag{11}$$

In a similar way, the voltage gains of all the proposed inverter topologies can be calculated, as shown in Table 1 and plotted in Fig. 9. As can be seen in Fig. 9, the voltage gain of the switch-to-tap and the ground-to-tap is much higher than that of the conventional full-bridge and half-bridge configuration. The ground and capacitor-to-tap and ground-to-tap have the widest voltage gain, thus being suitable for applications that require a wide voltage variation such as photovoltaic converter, battery charger, and uninterruptible power supplies. The output-to-tap is more suitable for the application with a relatively small voltage variation, such as consumer electronics and LED lighting applications. Switch-to-tap and switch and capacitor-to-tap (Fig. 5a and b) have the highest voltage gain for the same winding ratio N_1 and duty cycle D, so they are the most suitable inverter candidates for CPT systems in terms of voltage gain. Therefore, switch and capacitor-to-tap is the most suitable for analysis in this paper for CPT systems. In this case, the combination of inverter and rectifier can be chosen according to the requirement of the step-up or step-down voltage at the output voltage conversion ratio. For example,

Table 1 Voltage gain of the tapped inductor in different topologies in Fig. 5

Figures	Topologies	Voltage gain
5a	Switch-to-tap	$\frac{\sqrt{2}N_1 \sin \pi D}{\pi(1-D)}$
5b	Switch and capacitor-to-tap	$\frac{\sqrt{2}N_1 \sin \pi D}{\pi(1-D)}$
5c	Output-to-tap	$\frac{\sqrt{2} \sin \pi D}{N_1(1-D)}$
5d	Output and capacitor-to-tap	$\frac{\sqrt{2} \sin \pi D}{\pi N_1(1-D)}$
5e	Ground-to-tap	$\frac{\sqrt{2}(N_1-1) \sin \pi D}{\pi(1-D)}$
5f	Ground and capacitor-to-tap	$\frac{\sqrt{2}(N_1-1) \sin \pi D}{\pi(1-D)}$

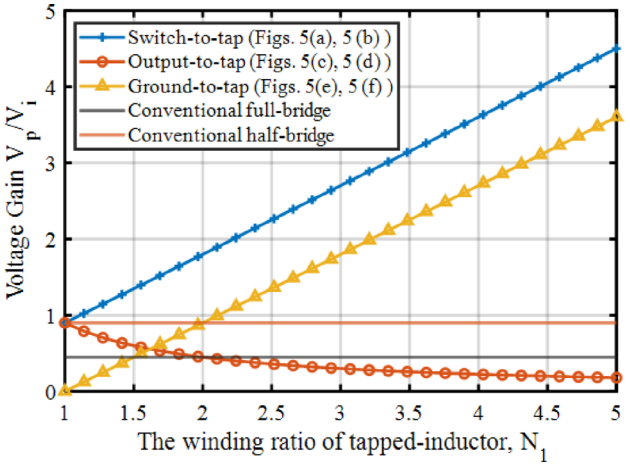

Fig. 9 Voltage gain comparison of the proposed family of the tapped-inductor half-bridge inverter for the CPT system when duty cycle D=0.5

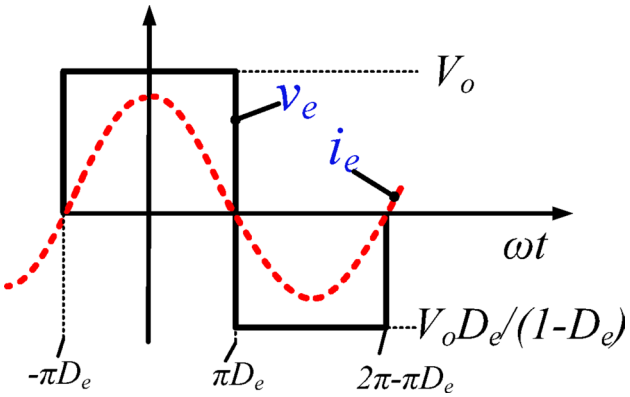

Fig. 10 Rectifier current and voltage waveforms

the output-to-tap topology can be used due to the step-up conversion gain for both the inverter and the rectifier when a high voltage at the output voltage is required, which can further boost the output voltage.

3.2 Operation analysis of rectifier

The voltage gain of rectifiers is a lateral inversion of inverters and thus equal to the reciprocal voltage gain of inverters in Table 1, having a step-down voltage gain that is much higher than that of the conventional half-wave rectifier.

The rectifier current and voltage waveform are shown in Fig. 10. The voltage applied to the inductor L_{2a}, V_e, is equal to V_o in the positive cycle and to V_{cc2} in the negative cycle. With the use of the flux balance condition to the inductor L_{2a}, the voltage in the negative cycle is equal to

$$V_{C2} = \frac{D_e}{1-D_e} V_o \tag{12}$$

where D_e is the effective conduction duty cycle of the rectifier. Therefore, the first harmonic of the rectifier input voltage is given by

$$V_e = \frac{\sqrt{2} \sin \pi D_e}{\pi (1-D_e)} V_o. \tag{13}$$

Assuming that no loss dissipation occurs in the rectifier, the input power of the rectifier should be equal to the output power of the rectifier as

$$\left(\frac{\sqrt{2} \sin \pi D_e}{\pi (1-D_e)} V_o \right)^2 \frac{1}{R_e} = \frac{V_o^2}{R_o}. \tag{14}$$

Thereby, the AC of the equivalent resistance is given by

$$R_e = \left(\frac{\sqrt{2} \sin \pi D_e}{\pi (1-D_e)} \right)^2 R_o. \tag{15}$$

The value of D_e is determined by assuming that the current i_{L2b} is sinusoidal, as follows:

$$i_{L2b}(\omega t) = -I_{L2b,\max} \cos(\omega t + \theta) \tag{16}$$

where $I_{L2b,\,max}$ and θ are the amplitude and phase shift angle in reference to the output voltage of the resonant tank, V_e, respectively. The inductor current of L_{2a} is given by (17) during $-\pi D_e<\omega t\leq\pi D_e$,

$$i_{L2a}(\omega t)=\begin{array}{l}\frac{1}{\omega L_{2b}}\left[\omega M_2 I_{s,\max}\left(\cos(\omega t+\theta)-\cos(\theta-\pi D_e)\right)\right.\\ \left.-V_L(\omega t+\pi D_e)\right]+i_{L2b}(-\pi D_e)\end{array} \tag{17}$$

and during $\pi D_e<\omega t\leq 2\pi-\pi D_e$,

$$i_{L2a}(\omega t)=\begin{array}{l}\frac{1}{\omega L_{2b}}\left[I_{s,\max}M_2\omega(\cos(\omega t+\theta)-\cos(\pi D_e+\theta))\right.\\ \left.+\frac{D_e V_L}{1-D_e}(\omega t-\pi D_e)\right]+i_{L2b}(\pi D_e)\end{array} \tag{18}$$

The input current of the rectifier i_e is calculated by

$$i_e(\omega t)=i_{L2a}(\omega t)-i_{L2b}(\omega t). \tag{19}$$

because $\omega t=\pm\pi D_e$ are defined as the instant of the current zero crossing, as shown in Fig. 10

$$\begin{cases} i_e\left(-\pi D_e\right)=0\\ i_e\left(\pi D_e\right)=0.\end{cases} \tag{20}$$

From those conditions, the expression of i_{L2a} at $-\pi D_e$ and the phase shift angle θ are given by

$$i_{L2a}(-\pi D_e)=\frac{\pi D_e V_o}{\omega(L_{2a}-M_2)} \tag{21}$$

where

$$\theta=\pi D_e-\arccos\left(-\frac{\pi D_e V_o}{I_{s,\max}\omega(L_{2a}-M_2)}\right) \tag{22}$$

With the charge balance applied to the capacitor C_{c2}

$$\int_{\pi D_e}^{2\pi-\pi D_e} i_e(\omega t)d(\omega t)=0, \tag{23}$$

the amplitude $I_{s,\,max}$ of the current i_{Lb2} can be expressed as

$$I_{s,max}=-\frac{\pi L_{2a}I_o}{(L_{2a}-M_2)\left[\sin(\pi D_e)\cos(\theta)-\pi D_e\cos(\pi D_e-\theta)\right]} \tag{24}$$

The average current of i_e is equal to the output current I_o

$$I_o=\frac{1}{2\pi D_e}\int_{-\pi D_e}^{\pi D_e} i_e\left(\omega t\right)d\left(\omega t\right)+\frac{1}{2\pi\left(1-D_e\right)}\int_{\pi D_e}^{2\pi-\pi D_e} i_e\left(\omega t\right)d\left(\omega t\right). \tag{25}$$

With (25) substituted to (15), the equivalent resistance R_e is given by

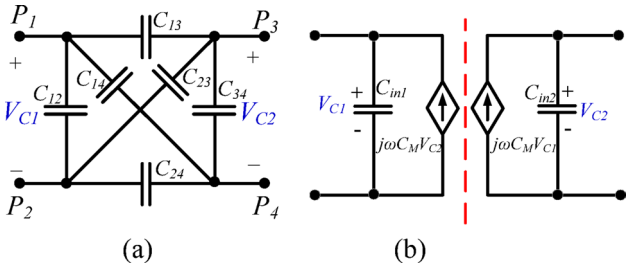

Fig. 11 Equivalent circuit model of the capacitive coupler: **a** circuit model of the coupling capacitors; **b** equivalent two-port model

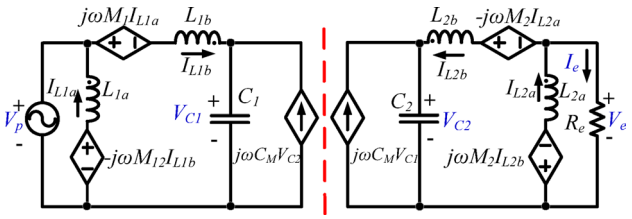

Fig. 12 Simplified equivalent AC circuit model of the proposed double-side tapped-inductor CPT system

$$R_e=-\frac{\pi L_{2a}V_o}{I_{s,max}(L_{2a}-M_2)\left[\sin(\pi D_e)\cos(\theta)-\pi D_e\cos(\pi D_e-\theta)\right]} \tag{26}$$

The AC equivalent resistance, R_e, presented in (26), is newly derived in this paper specifically for the proposed topology's frequency domain representation. This formulation is developed to accurately reflect both the impedance characteristics and nonlinear impedance transformation effect introduced by the rectifier.

4 Overall analysis of tapped-inductor CPT systems for CC-CV operation

The capacitive coupler of the CPT system contains four plates P_1–P_4, which have six capacitances as shown in Fig. 11a. It can be represented by the two-port network model, as shown in Fig. 11b, where C_1 and C_2 are equivalent self-capacitance defined as $C_1=C_{in1}+C_{ex1}$ and $C_2=C_{in2}+C_{ex2}$ and the capacitive coupling coefficient is $k_c=C_M/(\sqrt{C_1C_2})$ with C_M as the mutual capacitance [13, 26]. The simplified equivalent circuit model of the overall system is shown in Fig. 12. Note that every voltage and current is represented in its phasor notation. By KVL, the relationship of the current can be expressed as follows:

$$\begin{array}{l} I_{L1b}=Y_{L1}\left(N_1V_1-V_{C1}\right)\\ I_{L2b}=Y_{L2}\left(N_2V_2-V_{C2}\right)\\ I_{L2a}=-\left(N_3\left(N_2V_2-V_{C2}\right)+V_e\right)Y_{L2a}.\end{array} \tag{27}$$

From the results of (27), KCL is applied to derive the relationship of the voltage as follows:

$$\begin{aligned} &Y_{L1}\left(N_1V_1 - V_{C1}\right) + Y_M \cdot V_{C2} = V_{C1} \cdot Y_{C1} \\ &Y_{L2}\left(N_2V_2 - V_{C2}\right) + Y_M \cdot V_{C1} = V_{C2} \cdot Y_{C2} \\ &Y_{L2}\left(N_2V_2 - V_{C2}\right) + \left(N_3\left(N_2V_2 - V_{C2}\right) + V_e\right) Y_{L2a} = -Y_{RL} \cdot V_2 \end{aligned} \tag{28}$$

where

$$\begin{aligned} &Y_{L2a} = \tfrac{1}{j\omega L_{2a}}, Y_{L1a} = \tfrac{1}{j\omega L_{1a}}, Y_{L2b} = \tfrac{1}{j\omega L_{2b}}, Y_{L1b} = \tfrac{1}{j\omega L_{1b}}, \\ &Y_{C1} = j\omega C_1, Y_{C2} = j\omega C_2, Y_M = j\omega C_M, \\ &Y_{L1} = \tfrac{1}{j\omega\left(L_{1b} - \left(M_1^2/L_{1a}\right)\right)}, Y_{L2} = \tfrac{1}{j\omega\left(L_{2b} - \left(M_2^2/L_{2a}\right)\right)}, \\ &N_1 = \left(1 + \left(M_1/L_{1a}\right)\right), N_2 = \left(1 + \left(M_2/L_{2a}\right)\right), N_3 = \tfrac{M_2}{\left(L_{2b} - \left(M_2^2/L_{2a}\right)\right)}, \\ &Y_1 = j\omega C_1 + \tfrac{1}{j\omega\left(L_{1b} - \left(M_1^2/L_{1a}\right)\right)}, Y_2 = j\omega C_2 + \tfrac{1}{j\omega\left(L_{2b} - \left(M_2^2/L_{2a}\right)\right)}, \end{aligned} \tag{29}$$

The voltage gain G_v=V_e/V_p and the transconductance G_i=I_e/V_p are determined as follows:

$$G_v = \frac{V_e}{V_p} = \frac{Y_M Y_{L1} N_1}{D_0 + \frac{1}{R_e A}\left(Y_1 Y_2 - Y_M^2\right)} \tag{30}$$

$$G_i = \frac{I_e}{V_p} = \frac{Y_M Y_{L1} N_1}{R_e D_0 + \frac{1}{A}[Y_1 Y_2 - Y_M^2]}, \tag{31}$$

where

$$\begin{aligned} &D_0 = Y_1\left[Y_2\left(N_2 + \frac{Y_{L2a}}{A}\right) - Y_{L2}N_2\right] - Y_M^2\left(N_2 + \frac{Y_{L2a}}{A}\right), \\ &A = Y_{L2} + N_3 Y_{L2a}. \end{aligned} \tag{32}$$

4.1 CV operation mode

As shown in (30), the voltage gain G_v is independent of the equivalent load resistance R_e when

$$Y_1 Y_2 - Y_M^2 = 0. \tag{33}$$

Therefore, the CV frequency that ensures CV mode operation can be given by

$$\omega_{CV1,2} = \sqrt{\frac{\omega_1^2 + \omega_2^2 \pm \sqrt{\left(\omega_1^2 + \omega_2^2\right)^2 - 4(1 - k_c^2)\omega_1^2\omega_2^2}}{2(1 - k_c^2)}} \tag{34}$$

where ω_1 and ω_2 are defined as

$$\omega_1 = \frac{1}{\sqrt{C_1\left(L_{1b} - \left(M_1^2/L_{1a}\right)\right)}}, \omega_2 = \frac{1}{\sqrt{C_2\left(L_{2b} - \left(M_2^2/L_{2a}\right)\right)}}. \tag{35}$$

With (34) substituted to (30), the magnitude of G_v in the CV condition is therefore given by

$$G_{CV} = \left|\frac{V_e}{V_p}\right|_{\omega=\omega_{CV1,2}} = \sqrt{\frac{\omega_{CV1,2}^2 - \omega_1^2}{\omega_{CV1,2}^2 - \omega_2^2}}\sqrt{\frac{C_1}{C_2}}. \tag{36}$$

When the capacitive coupler is designed to be symmetric where L_{1a}=L_{2a}=L_a, L_{1b}=L_{2b}=L_b, M_1=M_2=M, and C_1=C_2=C, the CV frequency and the voltage gain are further simplified as follows:

$$\omega_{CV1,2} = \frac{\omega_0}{\sqrt{1 \mp k_c}}, \tag{37}$$

$$|G_{cv}|_{\omega=\omega_{CV1,2}} = \sqrt{\frac{C_1}{C_2}} \tag{38}$$

where

$$\omega_0 = \frac{1}{\sqrt{C\left(L_b - \left(M^2/L_a\right)\right)}}. \tag{39}$$

Therefore, voltage gain can be designed by changing the capacitive ratio C_1/C_2.

4.2 CC operation mode

As shown in (31), the transconductance gain G_i is independent of the equivalent load resistance R_e when

$$Y_1 Y_2 - Y_1 Y_{L2}\frac{N_2}{\left(N_2 + \left(Y_{L2a}/A\right)\right)} - Y_M^2 = 0. \tag{40}$$

Therefore, the CC frequency that ensures CC mode operation can be given by

$$\omega_{CC} = \omega_0\sqrt{\frac{-(F-2) + \sqrt{(F-2)^2 + 4(1 - k_c^2)(F-1)}}{2(1 - k_c^2)}} \tag{41}$$

where

$$F = \frac{L_{2a} + L_{2b} + 2M_2}{L_{2a} + M_2}. \tag{42}$$

With (41) substituted to (31), the magnitude of G_i at the CC condition is therefore given by

$$G_{CC} = \left|\frac{I_e}{V_p}\right|_{\omega=\omega_{CC}} = \frac{N_1 N_2 \omega_{CC} C_M}{j\omega_o^2\left[k_c^2(\omega_{CC}/\omega_0)^4 - \left(1 - (\omega_{CC}/\omega_0)^2\right)^2\right]} \tag{43}$$

The gain is coupling-dependent and can therefore be designed by changing the tap ratio of L_1 and L_2, which affects N_1 and N_2 in this formula.

4.3 Control strategy

The system primarily utilizes frequency control to achieve CV or CC operation, depending on the load requirements or operational mode. By adjusting the operating frequency, we precisely manipulate the impedance of the resonant tank, thereby controlling the overall power delivery and optimizing for either CV or CC characteristics, which is crucial for battery charging or variable load scenarios. For voltage regulation control at the output, we implement the PWM duty cycle control of the inverter. This approach allows for fine-tuning of the output voltage by adjusting the effective input voltage applied to the resonant tank, especially when operating conditions might otherwise cause deviations from the desired voltage level.

4.4 Comparison with existing CPT systems

The comparison between the proposed tapped-inductor inverter/rectifier with integrated matching network and the existing CPT systems is shown in Table 2. A full-bridge inverter with four switches and full-wave diode rectifier with four diodes is mostly used in the existing CPT system [7, 20, 13, 21]. Moreover, the conventional CPT system supports either CV or CC operation [7, 20] but not both. In the proposed system, only two switches and two diodes are required for the inverter and the rectifier, showing less component count than the existing system. Moreover, step-up and step-down are possible while still achieving both CC and CV regulation in the proposed system.

5 Prototype design and experimental verification

5.1 Prototype design

In verifying the analysis, the design of the proposed WPT system follows a systematic multistage procedure to ensure optimal performance, high efficiency, and robust output regulation. In Step 1, all critical system specifications and operating parameters, including input/output voltage, desired output power, air gap, and nominal operating frequency, are defined. Step 2 involves selecting suitable inverter and rectifier topologies on the basis of the desired voltage gain characteristics as shown in Table 1. In Step 3, the physical dimensions of the capacitive coupling plates, their spacing, and the effective coupling capacitance C_s, C_p are characterized using a two-port network approach, assuming a symmetric coupler for simplicity. Step 4 focuses on calculating the required compensation inductances L_1, L_2, including the design of a tapped inductor whose tapping ratio N_1, N_2, and

Table 2 Topology comparisons for the CPT system

References	Driving topology	Compensation type	Number of inverter switches	Number of rectifier diodes	Number of compensation inductors-capacitors	Mutual capacitance	Output property	Coupler voltage stress	Circuit simplicity
[7]	Full-Bridge	Dual LC	4	4	2–2	2.8 pF	Step-down CV	Medium	Simple
[20]	Full-Bridge	Dual LC	4	0	4–3	3 pF	Step-down CC, CV	Medium	Simple
[22]	Half-Bridge	L	2	4	1–0	1 nF (1 mm airgap)	CV	High	Simple
[13]	Full-Bridge	LCL	4	4	4–2	37.86 pF	Step-down CC	Medium	Moderate
[23]	Full-Bridge	Dual LCLC	4	4	4–4	36.7 pF	Step-down CC	Low	Complex
[10]	Half-Bridge	Dual transformer	2	4	1–0	256 pF	Step-down CC	Medium	Moderate
[21]	Full-Bridge	Dual LC	4	4	4–4	11 pF	Step-down CC	Low	Complex
[8]	Full-Bridge	LCL-LC	4	4	3–2	100 pF	-	Low	Complex
[24]	Class E	L	2	2	3–2	1.7 nF (rotary CPT)	-	High	Simple
This paper	Buck-boost Half-Bridge	Tapped-Inductor	2	2	2–2	200 pF	Step-up and down CC, CV	Medium	Simple

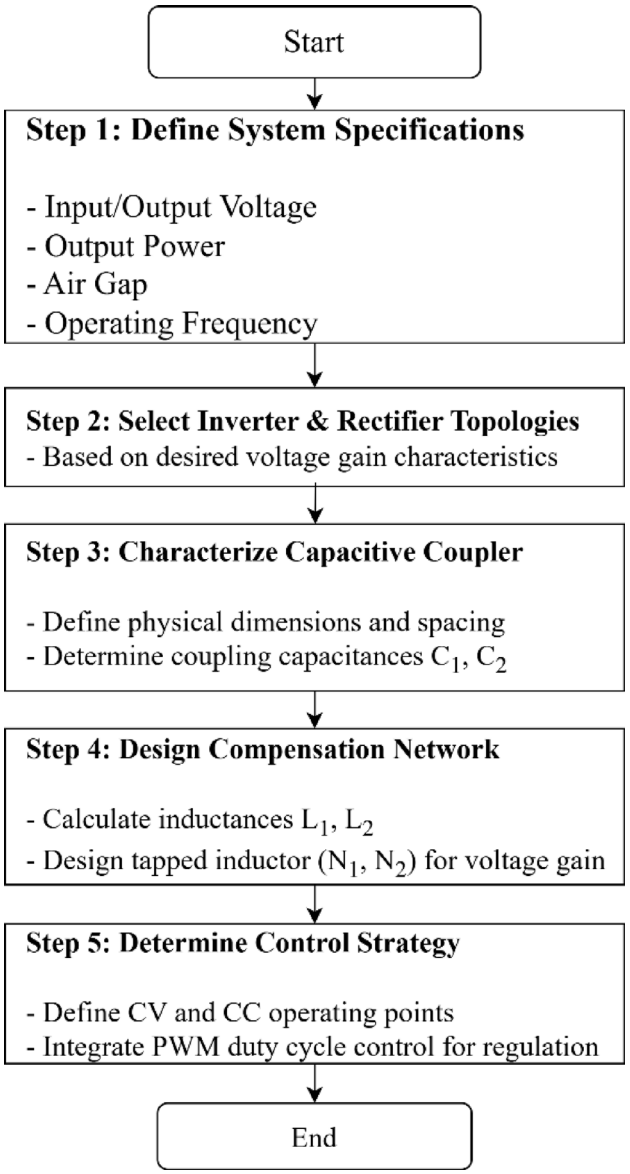

Fig. 13 Design procedure of the proposed system

capacitive ratio C_1/C_2 determine the system voltage gain and ensure resonance with the coupler capacitance at the operating frequency. In Step 5, CV and CC operation points are determined, integrating with PWM duty cycle control for voltage regulation. The design procedure of the proposed system is summarized in Fig. 13.

A prototype design of the CPT system is given in this section. Four identical (600 mm × 600 mm) aluminum plates are used as capacitive couplers. Air is the dielectric medium between the aluminum plates, with a distance of 17 mm between P_1 and P_3, and between P_2 and P_4. Two external capacitors, C_{ex1} and C_{ex2}, with 500 pF are added to the input and output side of the coupler. The capacitances of C_1, C_2, and C_M are measured as 795, 795, and 225 pF, respectively. The system is designed to be symmetric for both input matching network and output matching network such that L_{1a}=L_{2a}, L_{1b}=L_2b, and M_1=M_2. DC input voltage V_i is set at 50 V, and the equivalent load resistance is varied from 40 Ω to 80 Ω. The system parameters are designed as shown in Table 3.

Table 3 System parameters of tapped-inductor compensated CPT system

Symbol	Parameters	Values	Unit
f_s	Switching frequency	400	kHz
$L_{1a(L2a)}$	Parallel inductance	60	µH
$L_{1b(L2b)}$	Parallel inductance	230	µH
$M_1(M_2)$	Mutual inductance	18.2	µH
C_{12}, C_{14}, C_{13}, C_{23}, C_{24}	Physical-world circuit capacitance of coupler	01.5, 0.8, 198.5, 1.3, 201.3	pF
$C_1(C_2)$	Equivalent self-capacitance	700	pF
C_M	Mutual capacitance	200	pF
$C_{c1}(C_{c2})$	Clamp capacitance	50	µF
C_f	Output filter capacitance	200	µF

5.2 Simulation

The gain simulations of the system for different load conditions according to the analysis in Sect. 4 are shown in Fig. 14. Two CV operation points f_{CV1} = 335 kHz and f_{CV2} = 440 kHz and only one CC operation point at f_{CC} = 420 kHz exist, which match well with the calculated values from (34) and (41). Moreover, because the system is designed to be symmetric, the voltage gain G_v is unity at CV operation. Only resistive load R_e is considered in the analysis, which is why voltage V_e and current I_e have the same phase angle. As shown in Fig. 14c, the phase angle of voltage V_e at CV operation and current I_e at CC operation are θ_{CV1}=0°, θ_{CV2}=180°, and θ_{CC}=90°, respectively, when V_p is used as the reference phase.

Coupler voltage stress comparison with the traditional LC compensation of the CPT system is given by the simulation results. Inductors L_1 and L_2 with a value of 222 µH are connected on both sides of the capacitive coupler, as shown in Fig. 2, to form a resonant circuit with the capacitive coupler. The DC output voltage is fixed at 50 V. The transferred power is adjusted by the input voltage to deliver 50 W output power. The stress voltage V_1 and V_2 of the proposed topology is only 0.8 kV, while the voltage stress of LC compensation is as high as 1.34 kV. As a result of the inherent high voltage gain, the proposed CPT system can reduce the voltage stress by about 1.7 times compared with conventional LC compensation at the same transferred power.

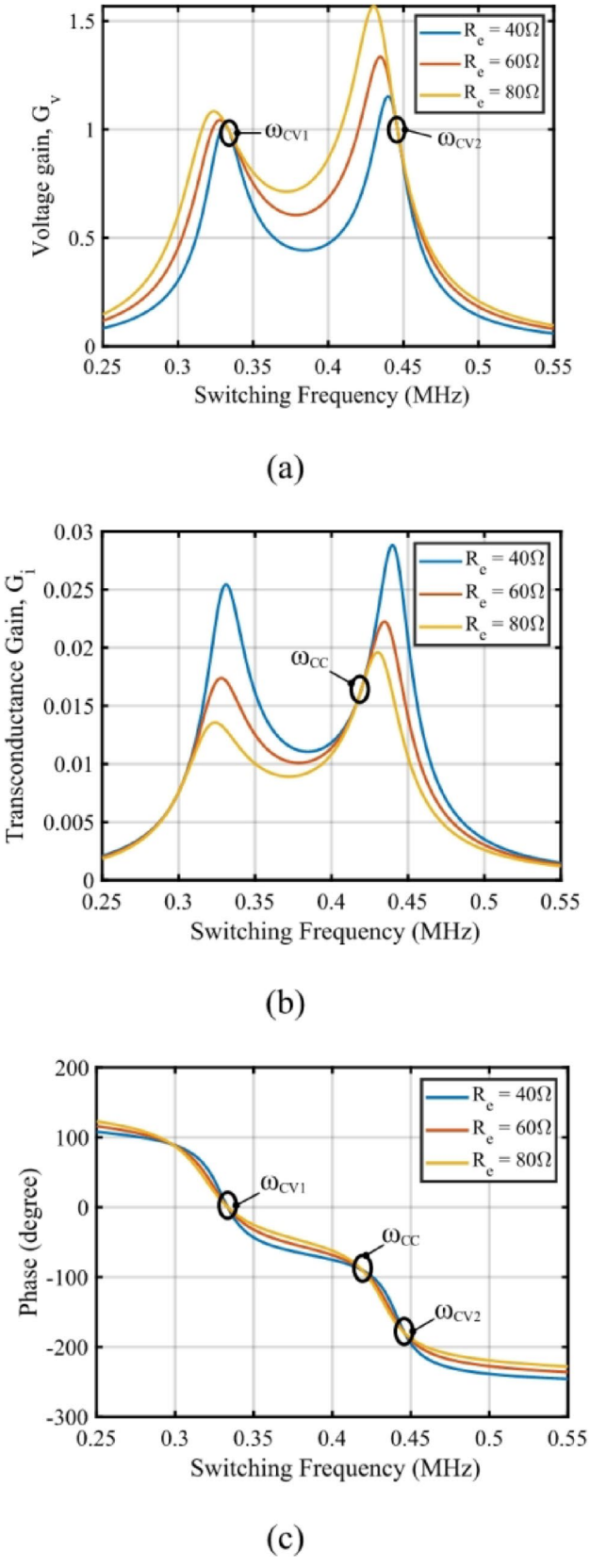

Fig. 14 Gain simulation of the proposed CPT system: **a** magnitude of the voltage gain G_v; **b** magnitude of the transconductance gain G_i;**c** phase angle of G_v and G_i

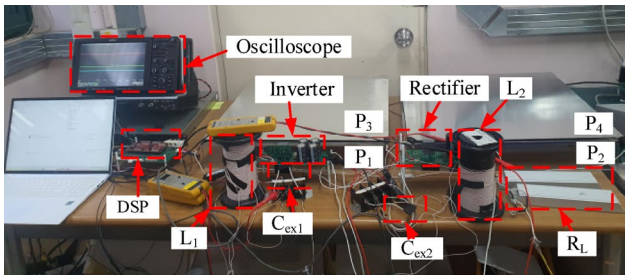

Fig. 15 Experimental setup of the proposed CPT system

5.3 Experimental verification

The experiment is conducted with the hardware setup shown in Fig. 15. Silicon carbide MOSFETs (CREE C3M0065090) with an on-resistance of 78 mΩ are used as the switches of the HF inverter and silicon carbide Schottky diodes with 1 V forward voltage (CREE C3D16060D) are used for the rectifier. The DSP (TI TMS320F28379D) is used as PWM generator for switches. The air-core tapped inductor was selected primarily for its performance, which was the focus of our study. The air-core design was essential for preventing core saturation at high currents and reducing core loss at high frequencies, thus ensuring high linearity and stable efficiency. While air-core inductors can be bulky, volume optimization was not the target of this study. Compared with compact ferrite-core designs, our choice was a necessary and deliberate trade-off between volume and system performance. Air core is used for two tapped-inductors with AWG 40 Litz wire. The measured parasitic capacitance components on primary side L_{1a} and L_{1b} are 14.5 and 15.1 pF, respectively, while they are 19.2 and 18.3 pF on secondary side L_{2a} and L_{2b}, respectively. The system is designed to operate at the ω_{cv1}, ω_{cv2} and ω_{cc} points, as illustrated in Fig. 14, which is why their effect on system operation is considered negligible. Figure 16 demonstrates the impedance curves for the system considering the ideal case (without parasitics) and with parasitics. Here, the AC analysis simulation of the equivalent circuit of the proposed system is obtained with and without the aforementioned parasitic values through LTspice to observe their effects. The impedance curves for both cases nearly overlap, showing only shifts. Thus, parasitics slightly alter the resonant frequencies, but the overall frequency response and resonance behavior remain largely unchanged. The experiment was conducted for both CV and CC operation conditions.

1) *CV operation results*: For CV operation condition, switching frequency f_s is set at f_{CV2} = 440 kHz. The experimental results of the CV working mode are shown in Fig. 17 for a load resistance R_e = 40 Ω. As shown in Fig. 17, V_p is lagging V_e by 180° at the CV frequency, which agrees with Fig. 14c.

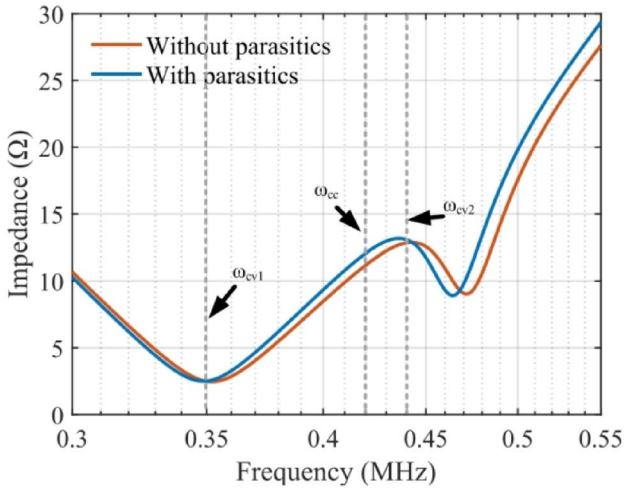

Fig. 16 Effect of parasitic components in tapped inductor

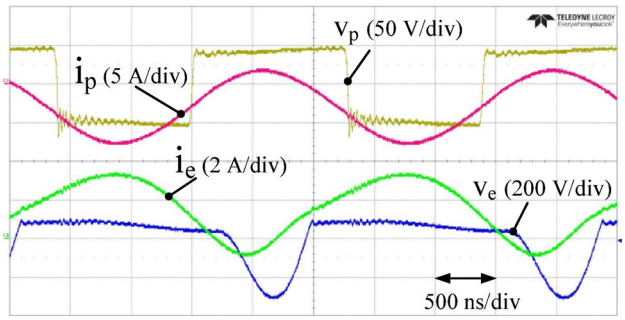

Fig. 17 Experimental waveforms in the CV operation mode

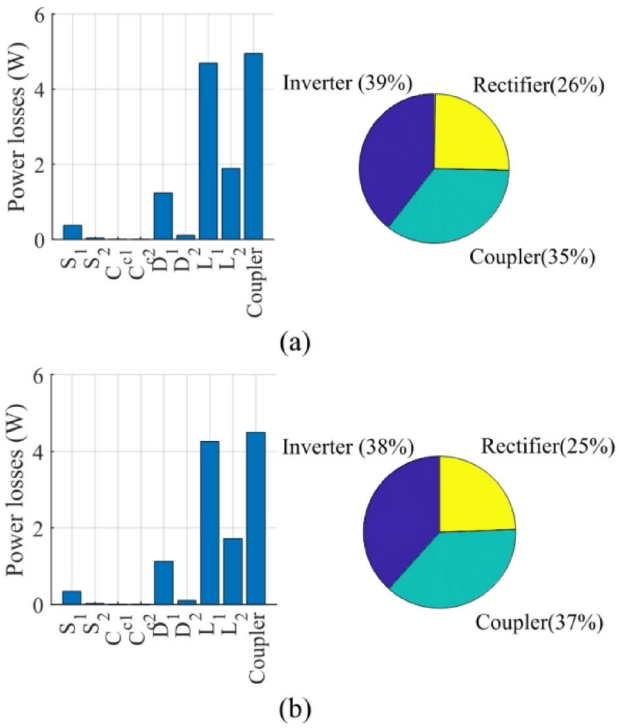

Fig. 18 Loss breakdown: **a** CV operation; **b** CC operation

Table 4 Coupler loss percentage in existing works

References	Power rating	Operation frequency	System efficiency	Coupler loss
[21]	1.8 kW	1 MHz	85.6%	36%
[7]	150 kW	1.5 MHz	74.8%	26%
[27]	3.75 kW	13.55 MHz	94.7%	5.3%
This paper	50 W	400 kHz	81.5%	35%

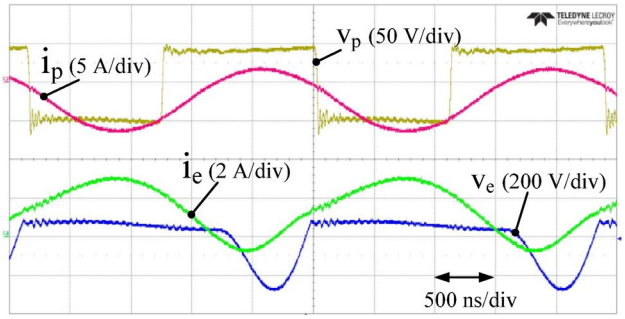

Fig. 19 Experimental waveforms in the CC operation mode

The power loss distribution among the circuit components is shown in Fig. 18a. The power loss in the compensation inductors and capacitors is calculated by their internal resistances and measured by an LCR Meter (Agilent 4263B). MOSFETs and diode losses are calculated by their drain-to-source resistance and the forward voltage information from datasheets. The remaining losses are dissipated in the couplers. The power analyzer (Yokogawa WT1804E) is used to measure the system efficiency. The DC-DC system efficiency is 81.5%, and its loss breakdown is shown in Fig. 18a. In future designs, thicker wire and low-loss external capacitors with a lower dissipation factor can be used to reduce the system loss and improve its efficiency. The coupler losses are categorized into two types: innate loss and region loss. The innate losses in the coupler structure include metal conduction losses and polarization loss (dielectric losses) [25]. The region loss is caused by the air and the leakage current loss between the CPT couplers and the surrounding objects [26]. Coupler loss percentages reported in existing works are summarized in Table 4. The coupler loss percentage achieved in this paper is comparable to that of existing works. To reduce the coupler's power loss, its innate loss can be minimized by improving the conductivity of the metal plates, which lowers the coupler's equivalent series resistance.

2) CC operation results: For CC operation condition, the switching frequency fs is set at 420 kHz. Experimental results of the CC mode are shown in Fig. 19 for a load resistance R_e = 40 Ω, which shows the output voltage V_e lags the input voltage V_p by 90°. This finding agrees with the expected theoretical result shown in Fig. 14c. The DC–DC

system efficiency is 78.8%, and the loss breakdown is shown in Fig. 18b.

6 Conclusion

This paper proposes a family of tapped-inductor inverter/rectifiers with an integrated matching network structure for CPT systems. The tapped inductor and buck-boost inverter are combined to reduce the voltage stress of the CPT system by providing a high voltage conversion ratio.

The proposed topology also has the advantage of a wide voltage gain to eliminate the additional DC-DC converter, resulting in fewer components. The proposed topology can operate in CC and CV modes, which are clearly advantageous for CPT's most popular battery charging applications. The experimental results agree well with the theoretical analysis. The proposed CPT system can reduce the voltage stress by 1.7 times compared with the conventional double-side LC at the same transferred power.

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Declarations

Conflict of interest While conducting this study, Sung-Jin Choi served as the Editor-in-Chief of the Journal of Power Electronics. Editorial Board Member status has no bearing on editorial consideration.

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