Energy Conversion
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공학박사 학위논문

전계결합형 무선전력전송 시스템의 커플러 전압 스트레스 저감 및 오정렬 보상을 위한 토폴로지 및 제어 전략

Topology and Control for Capacitive Power Transfer System with Reduced Voltage Stress and Misalignment Compensation

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Topology and Control for Capacitive Power Transfer System with Reduced Voltage Stress and Misalignment Compensation

Supervisor: Professor SUNG-JIN CHOI

A Dissertation

Submitted to
the Graduate School of the University of Ulsan
In partial Fulfillment of the Requirements
for the Degree of

Doctor of Philosophy

by

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To my parents for all the support and understanding

To my wife with full of love

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Life is a journey, and pursuing a PhD has been one of the most challenging yet rewarding adventures of my life. As this chapter finally comes to an end next month, I realize that this journey has not only been about academic growth, but also about personal and mental development. It has shaped the way I think, taught me resilience, and strengthened my ability to face challenges both inside and outside academia.

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Abstract

Capacitive Power Transfer (CPT) is an emerging wireless power transfer (WPT) technique that utilizes electric fields between metal plates to transmit energy. Compared to conventional Inductive Power Transfer (IPT) systems, CPT offers several advantages, such as the elimination of eddy-current losses in nearby metal structures and the potential for lightweight and low-cost systems. However, due to the low permittivity in air or vacuum, it suffers from high voltage stress between electrodes or CPT couplers, limited power transfer capability, and a narrow control range, which are obstacles to its adoption in practical applications.

This dissertation proposes circuit topologies and control strategies to address these technical drawbacks and enhance the feasibility of CPT systems. The main contributions of this dissertation include: first, a circuit matching technique robust to CPT coupler misalignment; second, a primary-side control strategy capable of compensating for coupler misalignment by estimating secondary-side voltage information and regulating output voltage across wide load conditions; third, a control method that extends the voltage gain of the high-frequency inverter to manage wide input voltage and load variations and achieve zero-voltage switching; and fourth, a method to reduce voltage stress on CPT couplers through a tapped-inductor based asymmetric half-bridge structure.

This dissertation is largely composed of a control technology section (Chapters 2 and 3), which deals with the modeling of misalignment and control strategies to overcome it, and a topology technology section (Chapters 4 and 5), which proposes inverter topologies providing a wide input/output control range and zero-voltage switching (ZVS), and presents methods to reduce the voltage stress applied to CPT couplers. First, Chapter 2 presents guidelines for optimal inverter and coupler design through the modeling of coupler misalignment. Utilizing the duality relationship between IPT and CPT technologies, similarities in equivalent models are derived, and misalignment compensation methods for series-series, series-parallel, parallel-series, and parallel-parallel structures are derived through two-port network (or four-terminal network) analysis. Meanwhile, Chapter 3, utilizing the equivalent model derived in Chapter 2, presents a parameter estimation technique capable of estimating the load voltage without secondary-side physical quantity measurement when misalignment occurs, and a primary-side control method using this. This method estimates key system parameters such as coupling capacitance and load impedance in real-time, allowing the con-

trol system to dynamically adjust the inverter's operating conditions to maintain optimal power transfer even in the presence of coupler misalignment or variable load conditions. It was verified through simulation that the proposed control method significantly improves system adaptability, allowing the CPT system to maintain stable power transfer and efficiency even with more than 20% lateral misalignment. Therefore, through the proposed algorithm, the additional communication line required for primary-secondary feedback control can be eliminated, and the coupling capacitance value indicating the degree of misalignment can also be estimated, enabling the design of a CPT system robust to coupler misalignment.

Meanwhile, Chapter 4 proposes an asymmetric half-bridge CPT inverter topology as a single power stage inverter circuit structure with high voltage gain, applicable to application circuits with a very wide input voltage range, such as those for universal AC input. In particular, Chapter 5 further develops this by presenting a family of tapped-inductor based inverter and rectifier topologies. Through this, the actual current flowing through the CPT coupler can be reduced, thereby decreasing the voltage stress on the CPT coupler, and an additional advantage of simplifying the complex networks typically required in conventional matching circuits was obtained. Hardware experiments verified that the proposed topology delivers 50W across an air gap of 100 mm, achieving a system efficiency of over 80%, and maintains soft-switching over a wide load range.

In conclusion, through the series of techniques presented in this dissertation, a more misalignment-tolerant and safer CPT system can be configured. Furthermore, by eliminating additional DC-DC conversion circuits and simplifying complex compensation networks through primary-side control via parameter estimation, the application range of CPT technology can be further expanded. This is expected to further strengthen the competitiveness of CPT technology compared to established technologies such as wired charging or IPT systems. Although not covered in this research, promising future research topics could include increasing the power density of CPT systems through high-frequency operation, bidirectional wireless power transfer, and technologies for dynamic wireless charging and multi-coupler utilization.

Contents

List of Abbreviations

AC	Alternating Current
CPT	Capacitive Power Transfer
DC	Direct Current
EMI	Electromagnetic Interference
FEA	Finite Element Analysis
FHA	Fundamental Harmonics Approximation
HF	High Frequency
IMN	Input Matching Network
IPT	Inductive Power Transfer
OMN	Output Matching Network
PI	Proportional Integral
PP	Parallel-Parallel
PS	Parallel-Series
PWM	Pulse Width Modulation
SiC	Silicon Carbide
SP	Series-Parallel
SS	Series-Series
WPT	Wireless Power Transfer
ZVS	Zero Voltage Switching

List of Nomenclatures

I_i,V_i	Input current and Input voltage
I_o,V_o	Load current and load voltage
P, Q	Active and reactive powers
T_s	Switching period
f_s	Switching frequency
ω_s	Angular switching frequency
$S_1 - S_1$	Inverter MOSFETs
$D_1 - D_4$	Rectifier diodes
$P_1 - P_4$	Metal plates
R_L	Load resistance
R_e	Equivalent resistance

Superscripts

ref	Reference value

Subscripts

n	n^{th} harmonic component

Chapter 1

Introduction

1.1 Background of Wireless Power Transfer

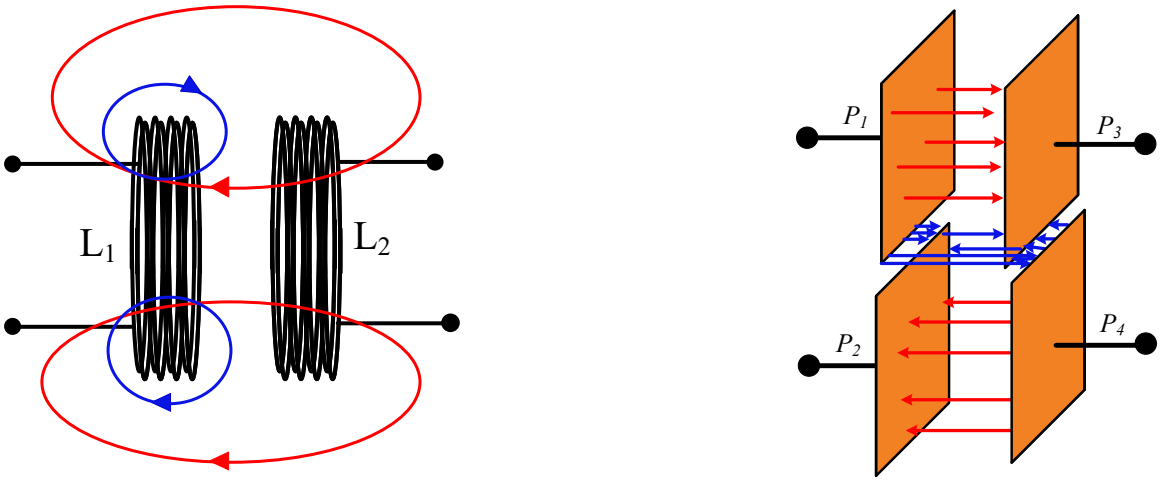
Wireless Power Transfer (WPT) is a revolutionary concept in electricity transmission, first invented by Nikola Tesla over a century ago [1–3]. Tesla's experiments, such as lighting fixtures bulbs wirelessly, laid the groundwork for cutting-edge WPT technologies, which allow electricity to be transmitted without the need of wires [3, 4]. Nowadays, WPT has a growing function in society, driving the development of purposes like wireless charging for smartphones [5], electric powered automobiles (EVs) [6–8], drones [9–11], and even medical implants [12–14], where direct connections are impractical. The substantial adoption of WPT is reshaping modern infrastructure, enabling a future where normal cables and plugs could be phased out [15]. Traditional wired systems are not only susceptible to losses, but they also rely on large and expensive infrastructure, which is often powered by fossil fuels. Wireless power, on the other hand, has the potential to change the way energy is provided, notably in industries such as EVs, industrial automation, and distributed energy [16, 17]. The primary approach to wireless power transfer (WPT) employs an inductive interface between the source and the load, known as inductive power transfer (IPT) [4, 18, 19], while an alternative method allows power to be transmitted through a capacitive interface, referred to as capacitive power transfer (CPT), which normally requires at least two capacitors [20]. In comparison to CPT, IPT transmitters and receivers are characterized by a more intricate design and typically require higher-cost materials [21]. On top of that, IPT depends on electromagnetic induction between coils, which generates eddy current losses, causing temperature rise of nearby objects which is dangerous in practice. This hindrance has driven the development of alternative applied sciences like CPT. By incorporating CPT into energy

Table 1.1: Comparison of CPT and IPT.

Feature	**Capacitive Power Transfer (CPT)**	**Inductive Power Transfer (IPT)**
Working Principle	Electric fields between plates transfer energy using high-frequency AC.	Magnetic fields from coils induce current in the receiver.
Advantages	- Thin, low-cost	- High efficiency
	- Less affected by nearby metals	- Suitable for high power transfer
	- Easy to shield (Faraday cage)	- Mature standards (Qi, EV, etc.)
	- Conformal to surfaces	- Long distance possible
Disadvantages	- Low power and short range	- Affected by nearby metals
	- Sensitive to alignment	- Bulky and costly coils
	- High AC voltage risk	- EMI concerns
	- Affected by dielectric changes	- Heat generation
Applications	Medical implants, sensors, robot	EV charging, phones, automation

infrastructure fields, it may help to minimize energy loss, improve the efficiency of renewable energy sources, and lessen the overall environmental effect of traditional power distribution networks. What is more, this strategy leads in cost and size savings as compared to inductive charging solutions [22, 23]. A comparison of capacitive and inductive power transfer is provided in Table 1.1.

Unlike IPT, CPT uses electric fields between conductive plates transfers the power through metal barriers while reducing significant power losses as shown in Fig. 1-1. CPT systems also tend to generate less heat and electromagnetic interference, making them a safer and extra efficient choice in sensitive environments, such as scientific units or incredibly populated urban areas [24]. According to current research, CPT is showing promise in

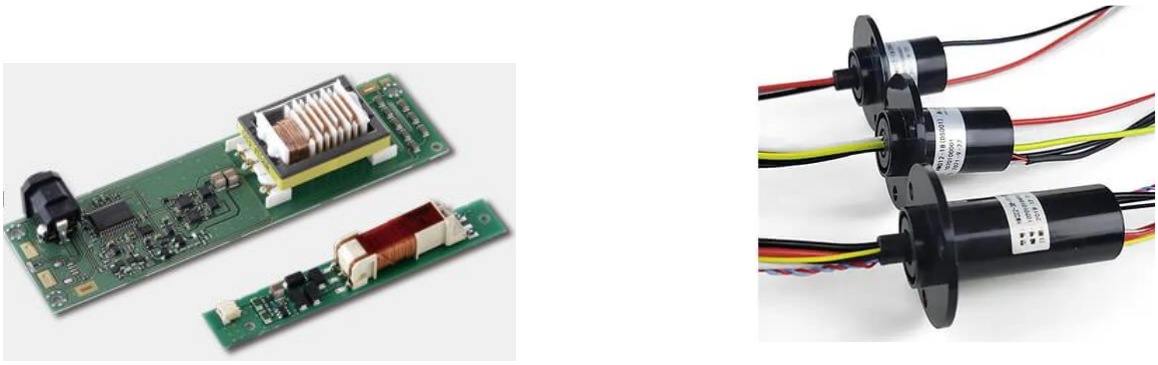


(a) (b)

Figure 1-1: Energy coupler of (a) IPT and (b) CPT.

Table 1.2: Examples of commercial capacitive power transfer (CPT) products information.

Company	Product Type	Primary Application	Target Customer	Website link
Murata Fig. 1-2(a)	Component Module	Connector replacement in small devices, rotating parts, or sealed enclosures.	Product Design Engineers	Website link [26]
GRAND Fig. 1-2(b)	Industrial Rotary System	Non-contact slip ring replacement for harsh industrial environments.	Industrial Automation Integrators	Website link [27]



(a) (b)

Figure 1-2: Examples of commercial capacitive power transfer (CPT) (a) capacitive coupling wireless power transmission modules with 10 W output power [26] and (b) through hole slip rings with 2 A output current and 240 V output voltage [27].

decreasing energy losses and presenting greater scalable options for power transfer [25]. As the improvement of WPT continues, the technology's viable impact on society is vast. It ought to enable wireless strength grids, enhance the effectiveness of renewable energy systems, and make contributions to a more sustainable future by means of eliminating the need for transmission wires.

The benefits of CPT technology are also primarily found in its affordability, lightweight design, and minimal eddy-current loss in nearby metals. Building on these advancements, CPT offers considerable potential for achieving contactless power transfer. Therefore, this thesis is essential to refine the technology by developing new topologies and new control strategies, as ongoing innovation in this field will enhance the overall performance of these systems and create more efficient solutions to meet future application demands. There is significant industrial demand for CPT technology, which has led to its commercialization. Table 1.2 lists several real-world products and their applications.

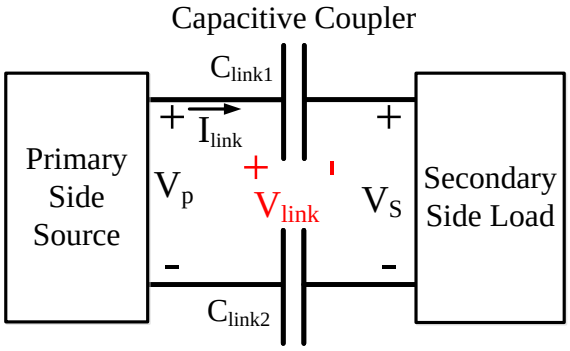


Figure 1-3: Capacitive power transfer concept.

1.2 State-of-the-Art and Challenges of Capacitive Power Transfer

CPT has been developed in circuit model establishment, where various coupling architectures were created, and power transfer from milliwatts to kilowatts over distances ranging from millimeters to decimeters [4]. The power transfer capability of a CPT system holds immense potential and promises to evolve into large-scale industrialization in the future to minimize the cost of configuration and recognize additional advantages in commercial products. Considering CPT applications, the technology demonstrates significant versatility across various domains. As shown in Fig. 1-3 the simplified CPT concept with AC primary side sources and secondary side load, the power is transferred through the two linked capacitors, C_{link1} and C_{link2}. The capacitance C_{link1} and C_{link2} of a CPT coupler is from a hundred picofarads to a few nanofarads due to the naturally low permittivity in vacuum and air. This results in a high impedance of a CPT coupler, which results in high voltage stress in the coupler as shown in

$$|V_{link}| = I_{link}\frac{1}{\omega_s C_{link1,2}} \tag{1.1}$$

where ω_s is the angular frequency of the primary side source. During the operation of CPT system, the capacitive coupler may not have a fixed alignment as there are many kinds of misalignments of CPT as shown in Fig. 1-4. The capacitive power transfer can be considered as a variable capacitive coupler as shown in Fig. 1-5. In summary, there are two fundamental issues of the CPT system. The first issue is the high voltage stress at the capacitive coupler and the second one is misalignment of the capacitive coupler. To overcome

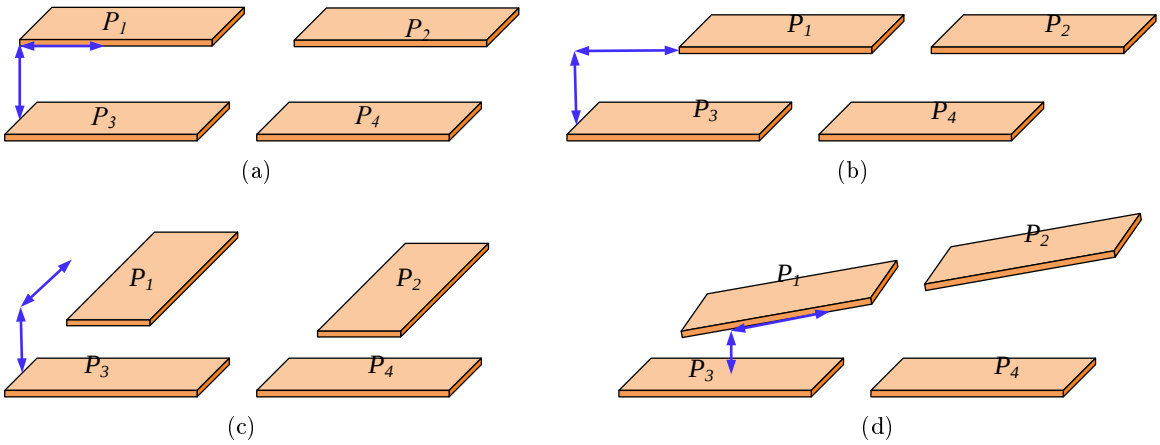


Figure 1-4: Coupling interface: (a) perfect alignment (b) lateral misalignment; (c) rotational misalignment; (d) angular misalignment

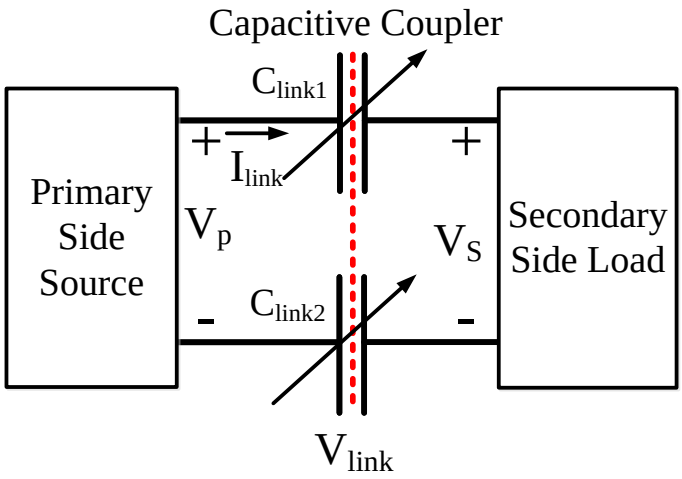


Figure 1-5: Capacitive power transfer with capacitive coupler in misalignment case.

the high voltage stress at the capacitive coupler issue, there are two common solutions in literature. First, switching frequency is increased to reduce the impedance of the capacitive coupler. However, due to the limited switching characteristics of power semiconductor devices and the restriction of the operation frequency range beyond a few megahertz, the switching frequency could not be increased. Second, the matching network is utilized to boost the voltage before capacitive coupler to reduce the current through the capacitive coupler in input matching network (IMN) at primary side and then voltage is reduced to output voltage by output matching network (OMN) as shown in Fig. 1-6, which is considered more realistic than the first one.

Various types of matching networks have been proposed in the literature to boost up the voltage, such as series, parallel, LLC, LCC, CLL, LCLC, and double-sided transformers as

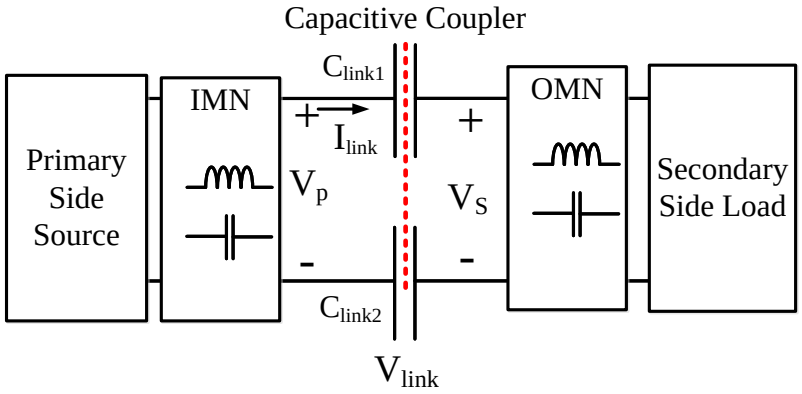


Figure 1-6: Capacitive power transfer with IMN and OMN concept.

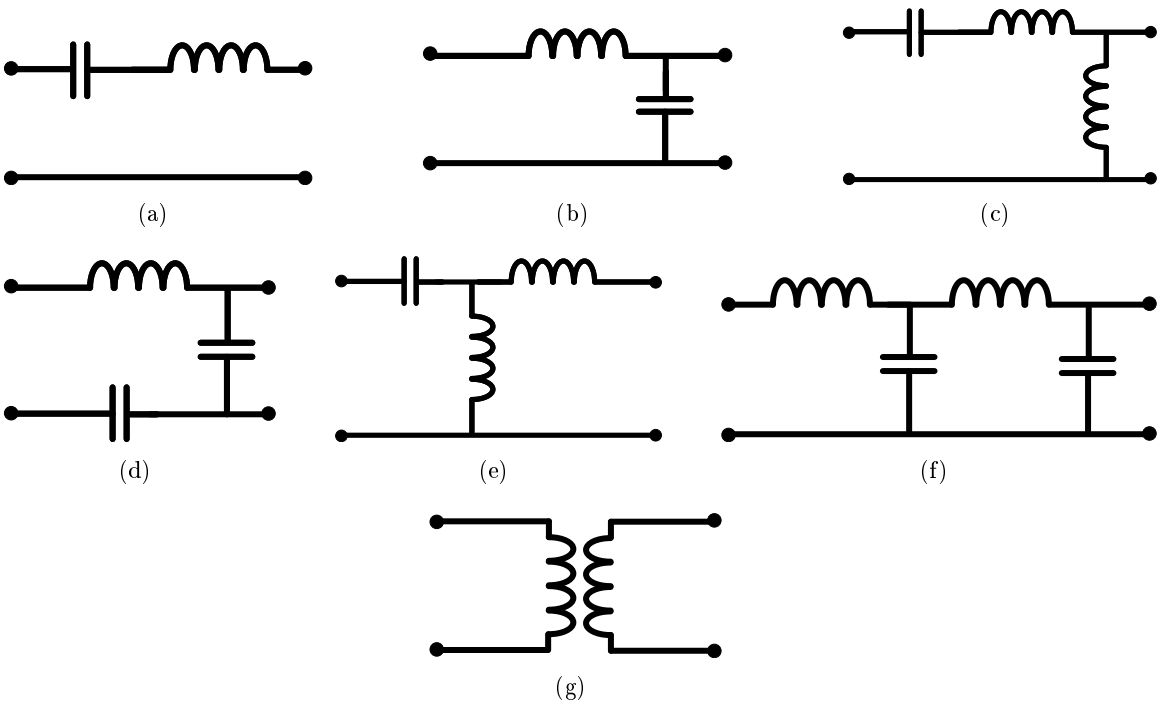


Figure 1-7: Matching network: (a) series (b) parallel (c) LLC (d) LCC (e) CLL (f) LCLC (h) transformer.

shown in Fig. 1-7. The advantage of series L compensation is its simplicity [28]. However, it still requires switching frequency to be in MHz range to provide sufficient power capability. The advantage of the double-sided LC compensation circuit is its feasibility in long distance [29]. The LCL compensation is the combination of L and LC [30, 31]. The complex design of the double-sided LCLC compensating circuit is a disadvantage. Because the circuit has eight passive components, the system cost and weight are raised. Furthermore, adding more components to the circuit can result in additional power losses, hence lowering system efficiency. As demonstrated in [32], the double-sided transformer compensation network can

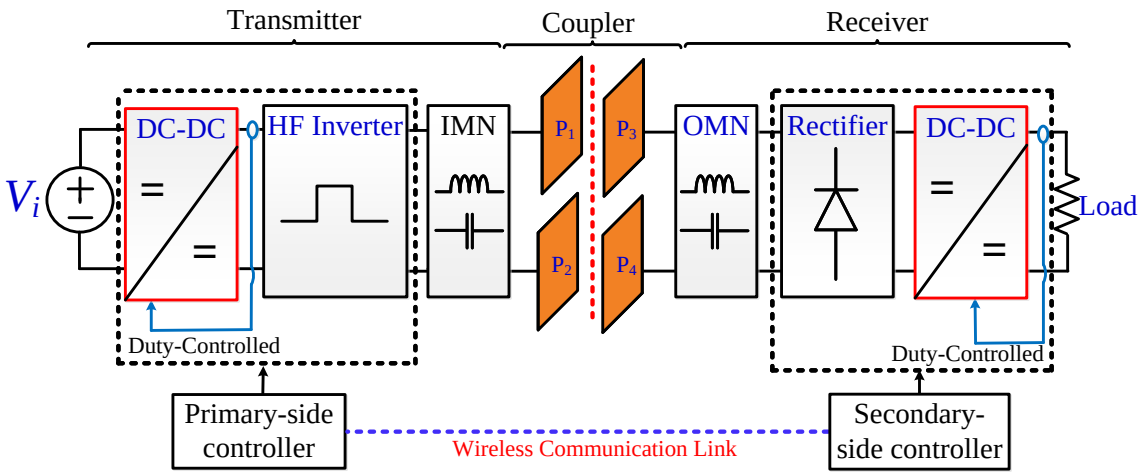


Figure 1-8: Capacitive power transfer system with front-end or back-end DC-DC converter.

also be utilized for impedance transformation. However, the bulkiness of the transformer increases the size of system. A high order compensation topology of CPT has been proposed in [20, 33]. However, due to complexity and large number of component count, it is not easy to apply. Some special shapes of compensation networks have been proposed in the literature [34–36]. The drawbacks of conventional compensation can be listed as low voltage gain (L, CL), design complexity, component counts (LCLC, double-sided LCLC), and bulkiness (double-sided transformers).

To overcome the second issue, the misalignment of the capacitive coupler, there are several solutions for that. The full-bridge or half-bridge inverter are normally used as controllable AC voltage source by duty control, and frequency control [20]. Nonetheless, those inverters cannot afford to regulate the wide control range, and thus front-end or back-end DC-DC converters are usually added for voltage regulation, as shown in Fig. 1-8 [37]. However, the system's two conversion phases make it costly and complex. Furthermore, system efficiency is lowered. Therefore, a single-stage configuration provides a compact, efficient, and more trustworthy CPT system. However, in this instance, the HF (high frequency) inverter must cope with the broad voltage regulation, which may be a difficulty for the current HF inverter. In the CPT systems, a range of topologies are available for the HF inverter.

Among various topologies that are available for the HF inverter in CPT systems [29, 38–41], the phase-shift full-bridge configuration is widely considered the most suitable topology since it can adjust both the magnitude and frequency of the primary voltage [42, 43]. But the thing is, it requires four power switches and gate drivers, which complicates the system and drives up the cost. On the other hand, to accomplish zero-voltage switching (ZVS), the

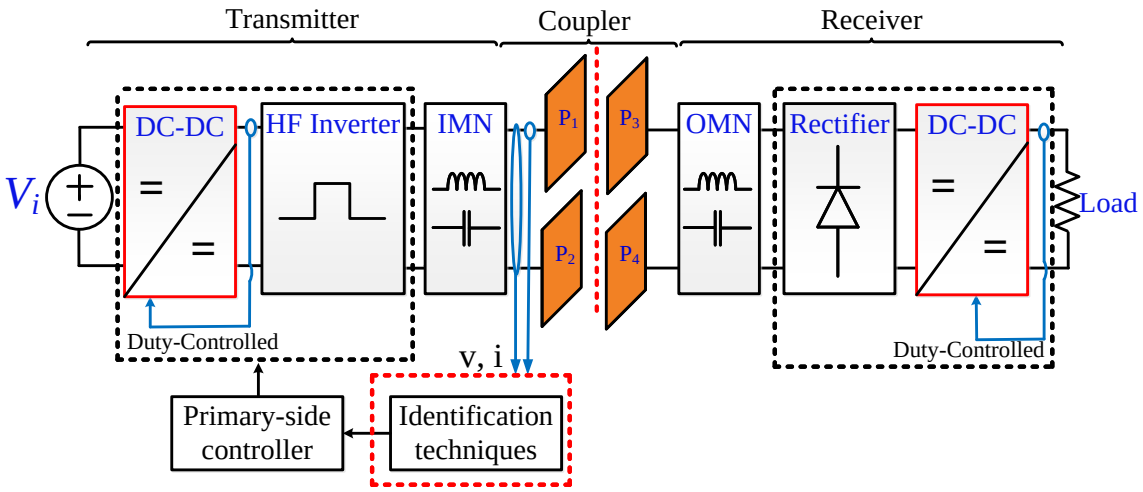


Figure 1-9: Capacitive power transfer system with primary side control method.

operational frequency should be tuned, so that it is inductively higher than the resonant frequency [44]. When ZVS is accomplished, the current should lag the voltage. It implies that the input impedance should be inductive when the phase angle is positive. Under light load conditions, the ZVS zone becomes much narrower than usual.

Another important part of CPT system is output current or voltage regulation. Under diverse operating conditions, the primary-side coupler and secondary side coupler varies, thereby influencing the power delivery quality. Therefore, control methods have been proposed to regulate the power in the system when misalignment occurs. A controller, particularly implemented on the primary-side, has conventionally been applied where parameter values are fedback from the secondary-side to the primary-side controller via wireless communication channels as shown in Fig. 1-8. However, delay, high cost and complexity of the system are limitations that are associated with this implementation [45]. Necessity for further innovation in primary-side control mechanisms that do not rely on any communication are crucial for maximizing the adaptability of these wireless systems across both static and dynamic applications.

In literature, early works reported in [46] as well as [47] have proposed single controller for the WPT system that requires only monitoring and utilizing parameters on the transmitting side of the system. Recent studies [48, 49] have also highlighted the importance of developing techniques for primary-side parameter identification, which can adapt to the conditions of operation, thereby enhancing the overall efficiency and viability of wireless power transfer systems, especially when traditional communication methods are impractical or infeasible. With the goal of simplicity and low cost of the system, front-end identification methods

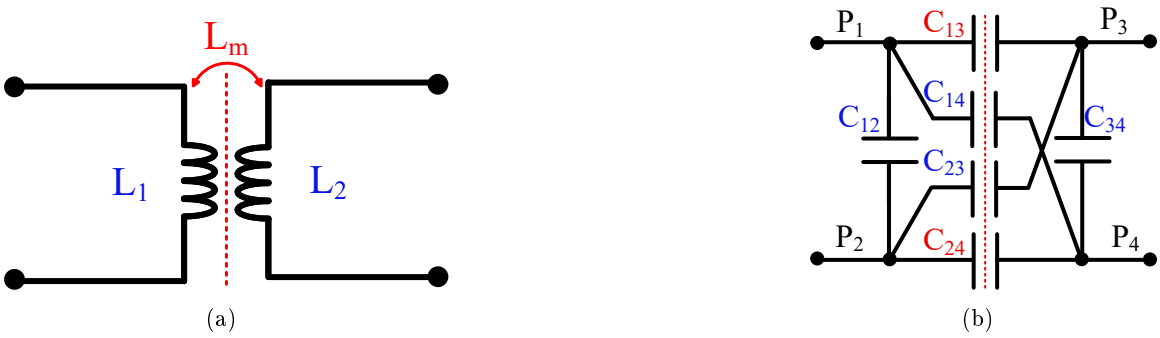


Figure 1-10: Coupling of (a) IPT (b) CPT.

stand out as innovative solutions that address this challenge in WPT systems as they play a role of acquiring information of system parameters to be utilized by the primary-side controller as shown in Fig. 1-9.

In this system, an identification function should be added to estimate the mutual capacitance and the output load resistance to regulate the output voltage or current at the secondary side. However, unlike IPT system, the coupler of CPT has six mutual capacitance [50, 51] as shown in Fig. 1-10. Which makes it much more difficult to estimate compared to the IPT system. As a result, estimation methods that have been proposed in the IPT system which could not be directly applied to the CPT system, thus new estimation method is necessary.

In light of these advancements, a comprehensive review of compensation topologies, capacitive coupler designs, and the latest advancements in CPT technology has been presented in [20]. This study found that CPT offers superior performance in handling large misalignments, particularly in electric vehicle charging applications. High-frequency electric fields are frequently used by CPT systems to obtain power transfer. The coupling capacitances are determined by the plate area, plate distance, and dielectric material used between the plates. The research and use of CPT technology have rapidly increased. After years of development, CPT systems have seen significant advancements in power transfer capability, efficiency, and transfer distance. Despite the advancements that CPT has attained such as voltage compensation, misalignment compensation, and primary side control aspects there are some limitations that have not been clearly investigated yet. This thesis intends to address existing challenges while enhancing applications suitable for various objectives to facilitate and foster the practical implementation of CPT technology.

1.3 Research Objectives

The purpose of this thesis is to evaluate CPT systems for advanced topology and control for capacitive power transfer systems to optimize voltage stress and improve misalignment compensation. Several innovative topologies will be proposed to achieve a broader voltage gain and increase the output voltage, thereby eliminating the need for an additional DC-DC converter and a complex compensation network. Additionally, a new primary control strategy accompanied by a parameter identification method is recommended.

Chapter 2 presents the fundamental architecture of CPT systems. Subsequently, it investigates diverse coupler structures and further explores misalignment-insensitive designs for CPT.

Chapter 3 introduces parameter identification for CPT system. Modeling and controller design is then developed based on this analysis.

Chapter 4 presents a new architecture that makes CPT systems even simpler and easier to control.

Chapter 5 presents a family of inverter/rectifier with integrated matching networks for CPT system which merges the functions of HF inverter/rectifier and impedance matching network.

Chapter 6 concludes design proposal of CPT systems to enhance above solutions and open new ideas for design concepts in the future.

1.4 Thesis Contribution and Organization

This thesis briefly provides background information on various categories of WPT systems and a comparison of different WPT technologies and also introduces the application of capacitive wireless power transfer (CPT) systems. It then reviews the challenges associated with wireless power transfer. The general structure of capacitive power transfer systems is discussed as shown in Fig. 1-11, with a focus on advanced topology and control of capacitive wireless power transfer, specifically addressing the inverter, compensation network, and capacitive coupler such as decreasing voltage stress and strengthening misalignment compensation. Finally, this thesis outlines its specific contributions to the field. The contributions of this research are summarized as follows:

1. Introduction: States about the background, the state-of-the-art and challenges, research objectives, scope and limitations, and thesis structure. Gives the background

information related to research, defines the problems of capacitive power transfer, and presents research objectives and methodology used to accomplish these objectives. Thesis structure is built up to fit overall comprehension content.

2. Misalignment insensitive structure of CPT system: Presents guidelines for optimal inverter and coupler design through the modeling of capacitive coupler misalignment. Utilizing the duality relationship between IPT and CPT technologies, similarities in equivalent models are derived, and misalignment compensation methods for series-series, series-parallel, parallel-series, and parallel-parallel structures are derived through two-port network (or four-terminal network) analysis.

3. Parameters identification for primary-side control: Utilizing the equivalent model derived in Chapter 2, presents a parameter estimation technique capable of estimating the load voltage without secondary-side physical quantity measurement when misalignment occurs, and a primary-side control method using this estimated information. This method estimates key system parameters such as coupling capacitance and load impedance in real-time, allowing the control system to dynamically adjust the inverter's operating conditions to maintain optimal power transfer even in the presence of coupler misalignment or variable load conditions.

4. Voltage regulation control scheme with wide input capability and extended ZVS: Proposes an asymmetric half-bridge CPT inverter topology as a single power stage inverter circuit structure with high voltage gain, useful for application with a very wide input voltage range, such as those for the universal AC input requirements.

5. Further develops this by presenting a family of tapped-inductor based inverter and rectifier topologies. Through this, the actual current flowing through the CPT coupler can be reduced, thereby decreasing the voltage stress on the CPT coupler, and an additional advantage of simplifying the complex networks typically required in conventional matching circuits was obtained.

6. Conclusions and suggestions: Concludes the main content and provides the directions for future works.

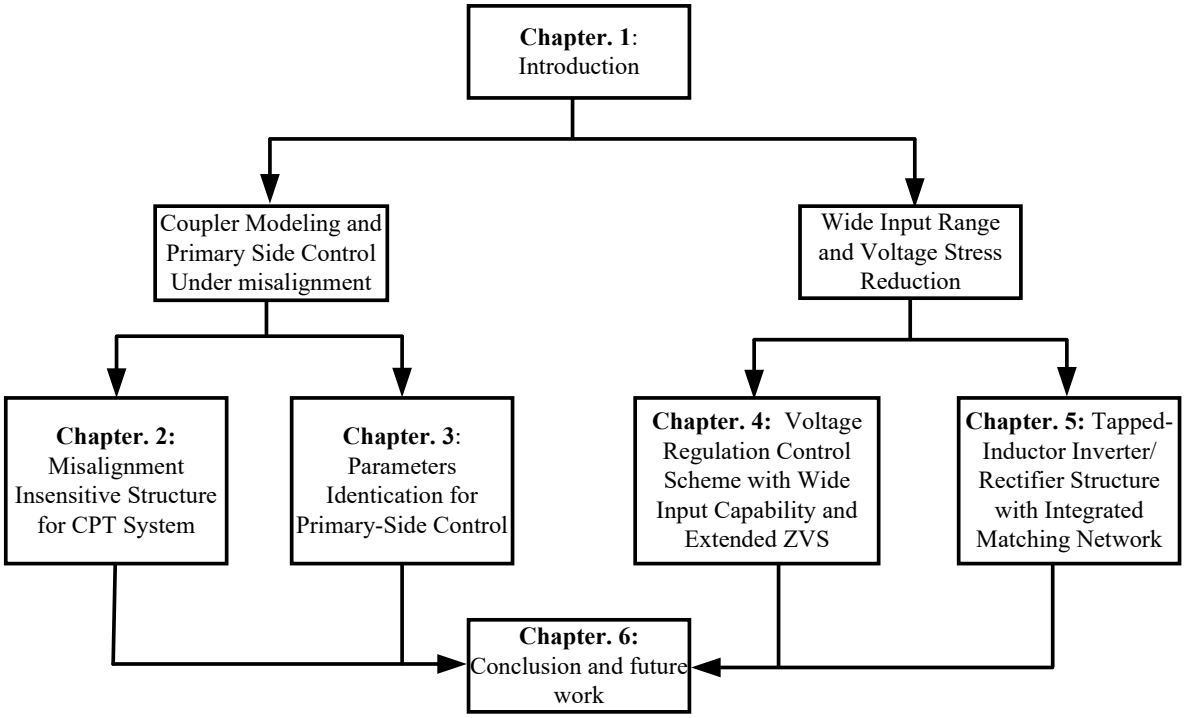


Figure 1-11: Overview of thesis structure.

Chapter 2

Misalignment Insensitive Structure for CPT System

This chapter investigates the general structure of capacitive power transfer (CPT) systems under misalignment compensation. Among various capacitive coupler structures, the four-plate rectangular structure is the most commonly used in CPT and has been selected for analysis in this chapter. Selection guideline of compensation network for misalignment mitigation is presented.

2.1 Introduction

The general structure of the capacitive power transfer system is shown in Fig. 2-1. The DC voltage is converted to a high-frequency (HF) AC voltage using an HF inverter. An input matching network (IMN) is required to compensate for the coupler's capacitance, reducing

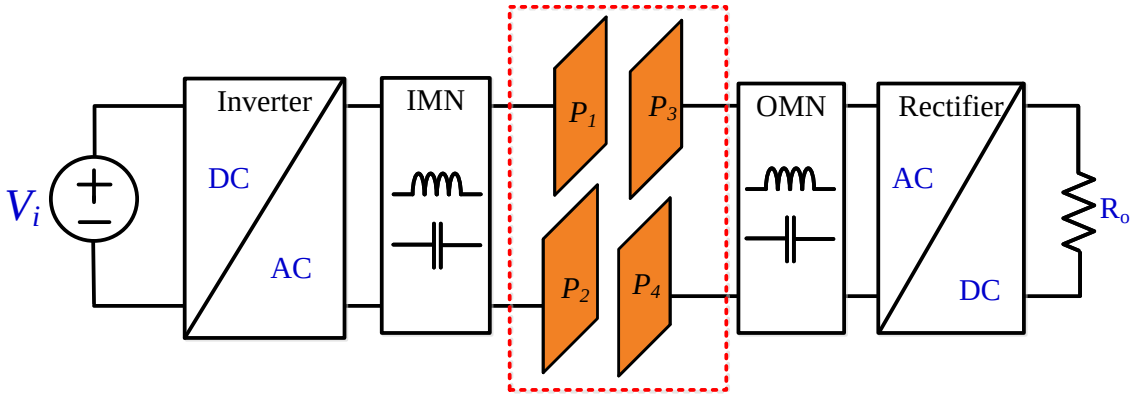


Figure 2-1: General structure of the capacitive power transfer system.

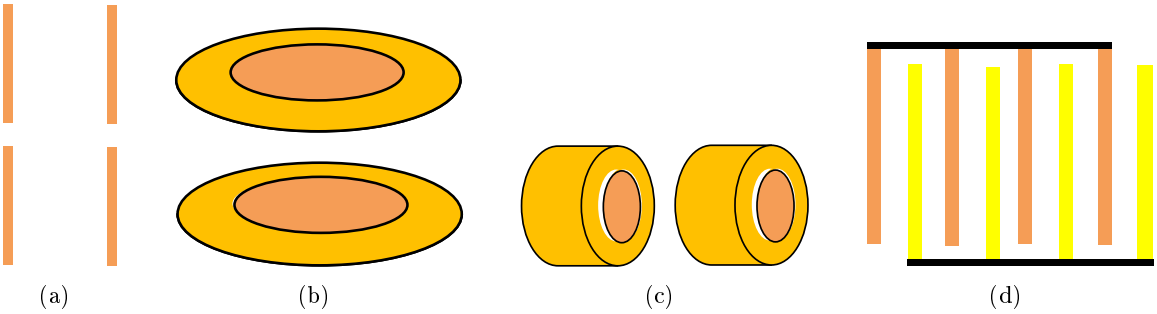


Figure 2-2: Capacitive coupler structures (a) rectangular (b) circular (c) cylindrical (d) stack array

the volt-ampere rating of the circuit, while an output matching network (OMN) is used to boost the current. A rectifier is then used to recover the DC voltage that supplies the load.

2.2 Capacitive Coupler

The energy coupler is the most important part of the CPT system. The transferred power is limited by the voltage stress of the capacitive coupler. There are many types of coupler shapes, such as rectangular, circular, cylindrical, and stacked arrays, as shown in Fig. 2-2. Rectangular plates are suitable for applications such as phones, laptops, and EVs [5–7]. Circular plates are suitable for rotating applications such as medical devices [12–14, 52, 53] and motors [54–56]. Stacked arrays can be used for applications that require a high-capacitance coupler, such as connections and robots [4, 57, 58]. The rectangular coupler is most commonly used for many applications.

Rectangular coupler structures can take many forms, including two-plate [59], four-plate with horizontal alignment [60], four-plate with vertical alignment [50], five-plate [61], six-plate [62], multiple-transmitter and multiple-receiver [63], and multiple-transmitter with a two-plate receiver [64], as illustrated in Fig. 2-3. Among these, the four-plate capacitive coupler structure is most commonly used in numerous applications, such as phones, laptops, and EVs [5–7]. Therefore, this thesis analyzes the four-plate rectangular capacitive coupler structure.

Fig. 2-1 illustrates a conventional CPT system configuration. The capacitive coupler within such a system typically consists of four plates, $P_1 \sim P_4$, with power transferred from plates P_1 and P_2 to plates P_3 and P_4. In a conventional four-plate coupler arrangement, any two plates can be coupled, resulting in six interconnected capacitors: C_{12}, C_{13}, C_{14}, C_{23}, C_{24}, and C_{34} as shown in Fig. 2-4(b) [50]. This model can be simplified into a two-port network,

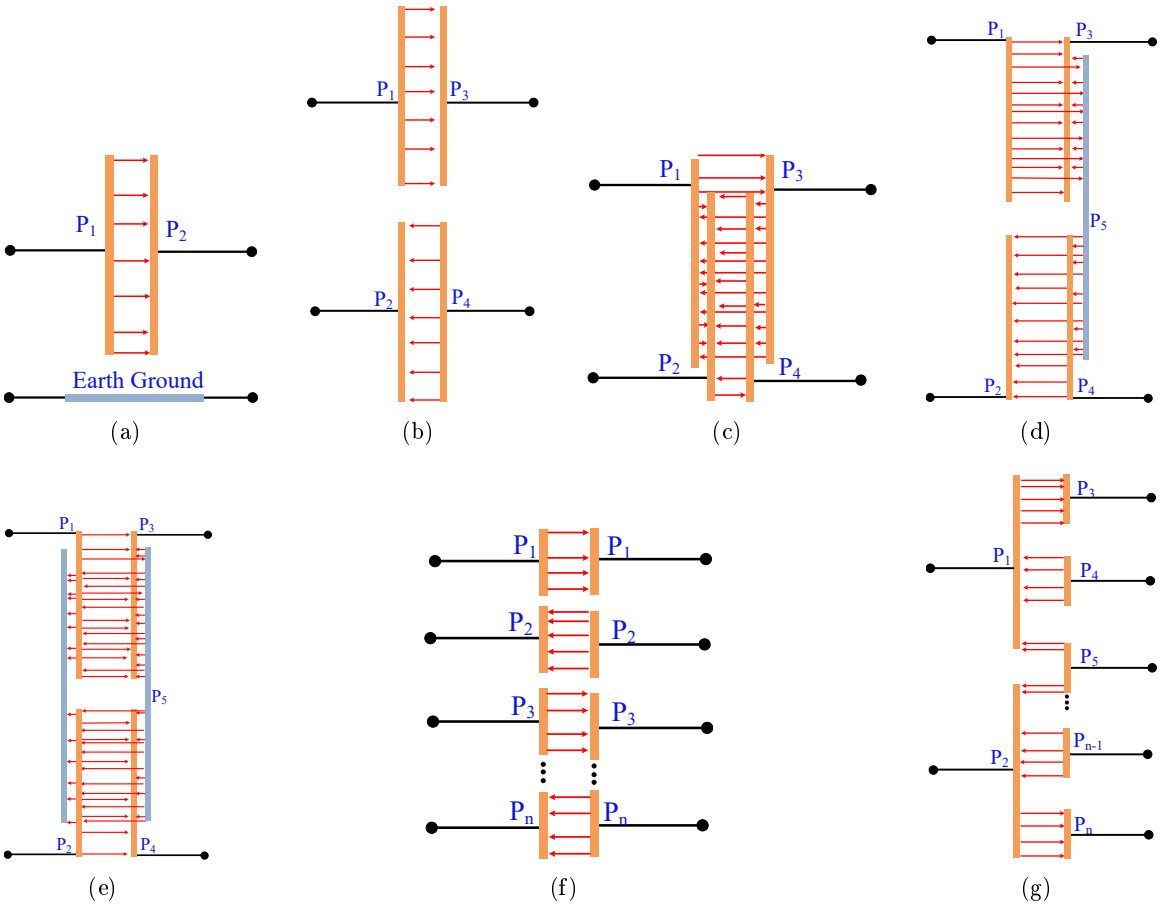


Figure 2-3: Rectangular CPT coupler structures (a) two plates (b) four plates with horizontal alignment (c) four plates with vertical alignment (d) five plates (e) six plate (g) multiple-transmitters and multiple receivers (e) multiple-transmitter and a two plates receiver.

as shown in Fig. 2-5(b), where C_1 and C_2 are the short-circuit self-capacitances and C_m is the equivalent mutual capacitance [50, 65]. V_1 and I_1 represent the voltage and current at the input terminals of the capacitive coupler, respectively, while V_2 and I_2 represent those at the output terminals. In this chapter, all voltages and currents are represented using phasor notation. Notably, the inductive power transfer (IPT) counterpart typically features only one mutual inductor between its two coupling coils as shown in Fig. 2-4(a). As a result, it is critical to establish a comprehensive yet straightforward coupling model for capacitive couplers, as this greatly simplifies circuit analysis and design [51].

2.2.1 The Duality of IPT and CPT Coupler

The T-equivalent of the IPT coupler is shown in Fig. 2-5(a). The open-circuit input impedance Z_{in}, as viewed from the primary and the secondary sides respectively, are given

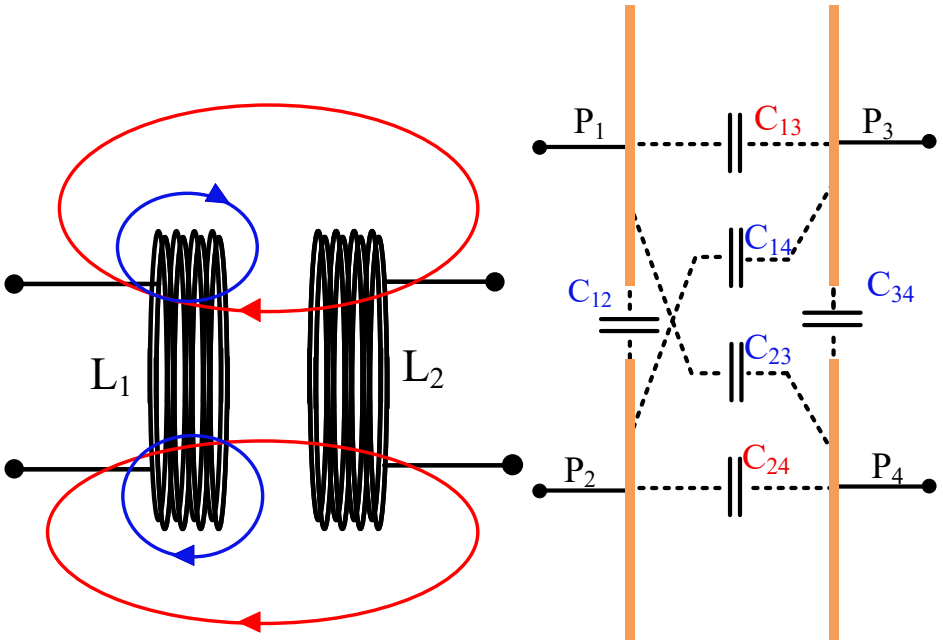


Figure 2-4: Energy coupler (a) Inductive coupler (b) Capacitive coupler.

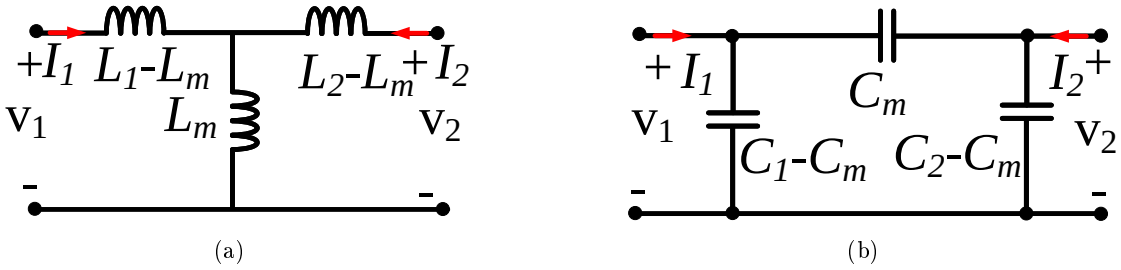


Figure 2-5: (a) T equivalent model of IPT coupler (b) π equivalent model of CPT coupler.

by

$$\begin{aligned} Z_{\text{in,pri}} &= \left.\frac{\mathbf{V_1}}{\mathbf{I_1}}\right|_{\mathbf{I_2}=0} &= j\omega L_1 \\ Z_{\text{in,sec}} &= \left.\frac{\mathbf{V_2}}{\mathbf{I_2}}\right|_{\mathbf{I_1}=0} &= j\omega L_2 \end{aligned} \tag{2.1}$$

which are the open-circuit self-inductances L_1 and L_2 , those are constant and measurable values. The π equivalent circuit model of CPT coupler is shown in Fig. 2-5(b) and the

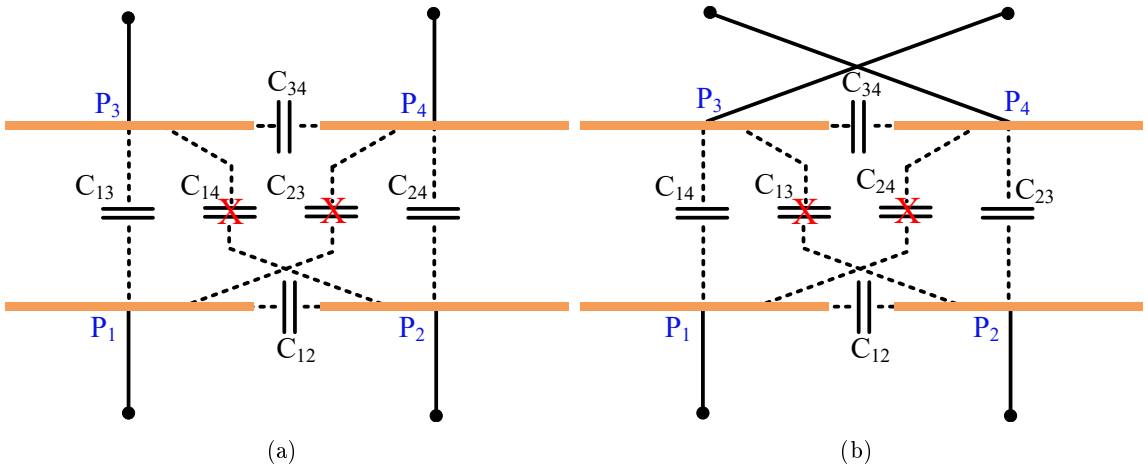


Figure 2-6: (a) A well-aligned case C_{14} and C_{23} can be zero (b) an extremely misaligned case where C_{13} and C_{24} can be zero.

open-circuit input impedance seen form the primary and the secondary side are given by

$$\begin{aligned} Z_{\text{in,pri}} &= \left.\frac{\mathbf{V_1}}{\mathbf{I_1}}\right|_{\mathbf{I_2}=0} &&= \frac{1}{j\omega(1-k_c^2)C_1} = \frac{1}{j\omega C_p} \\ Z_{\text{in,sec}} &= \left.\frac{\mathbf{V_2}}{\mathbf{I_2}}\right|_{\mathbf{I_1}=0} &&= \frac{1}{j\omega(1-k_c^2)C_2} = \frac{1}{j\omega C_s} \end{aligned} \tag{2.2}$$

where

$$\begin{cases} C_1 = C_{12} + \dfrac{(C_{13}+C_{14})(C_{23}+C_{24})}{C_{13}+C_{14}+C_{23}+C_{24}} \\ C_2 = C_{34} + \dfrac{(C_{13}+C_{23})(C_{14}+C_{24})}{C_{13}+C_{14}+C_{23}+C_{24}} \\ C_m = \dfrac{C_{13}C_{24}-C_{14}C_{23}}{C_{13}+C_{14}+C_{23}+C_{24}} \\ C_p = (1-k_c^2)C_1 \\ C_s = (1-k_c^2)C_2 \\ k_c = \dfrac{C_m}{\sqrt{C_1C_2}} = \dfrac{C_m(1-k_c^2)}{\sqrt{C_pC_s}} \end{cases} \tag{2.3}$$

C_p and C_s are measurable values. A detailed derivation of C_1, C_2, and C_m are given by [50]. It should also be noted that C_1 and C_2 from the general six-capacitor model, C_p, C_s are coupling-dependent capacitor. However, by the duality between IPT and CPT systems, C_p and C_s in the simplified two-port model should be analogous to self-inductances and thus be almost constant irrespective of the misalignment. To prove that C_p and C_s are not sensitive

to the displacement, two specific extreme cases are considered. The first is a well-aligned case where the cross-capacitors C_{14} and C_{23} can be almost zero as shown in Fig. 2-6(a). The second is an extremely misaligned case where the main coupling capacitors C_{13} and C_{24} can be zero as shown in Fig. 2-6(b). Under these conditions, (2.3) can be rewritten as:

when $C_{14} = 0$ and $C_{23} = 0$

$$\begin{cases} C_m = \dfrac{C_{13}C_{24}}{C_{13} + C_{24}} \\ C_1 = C_{12} + C_m \\ C_2 = C_{34} + C_m \end{cases} \tag{2.4}$$

and when $C_{13} = 0$ and $C_{24} = 0$

$$\begin{cases} C_m = \dfrac{-C_{14}C_{23}}{C_{14} + C_{23}} \\ C_1 = C_{12} - C_m \\ C_2 = C_{34} - C_m \end{cases} \tag{2.5}$$

Surprisingly, C_p and C_s are found to be equal in both extreme cases. The key insight is that although the intermediate relationship used to determine C_m and consequently the relationship between C_1 and C_m differs, and the sign of C_m itself is opposite in the two cases relative to the chosen positive root in its derivation, these differences ultimately cancel out when solving for C_1. The fundamental equation $k_c^2 C_1 C_2 = C_m^2$ illustrates why this is the case, as it does not depend on the sign of C_m due to the squared term. Therefore, in both cases, C_p and C_s are given by:

$$C_p = \frac{2C_{12} + k_c^2(C_{34} - C_{12}) + k_c\sqrt{k_c^2(C_{12} - C_{34})^2 + 4C_{12}C_{34}}}{2} \tag{2.6}$$

$$C_s = \frac{2C_{34} + k_c^2(C_{12} - C_{34}) + k_c\sqrt{k_c^2(C_{12} - C_{34})^2 + 4C_{12}C_{34}}}{2} \tag{2.7}$$

C_p and C_s can be expressed as functions of C_{12}, C_{34}, and k_c. Moreover, C_1 and C_2 are also expressed as follows

$$C_1 = \frac{2C_{12} + k_c^2(C_{34} - C_{12}) + k_c\sqrt{k_c^2(C_{12} - C_{34})^2 + 4C_{12}C_{34}}}{2(1 - k_c^2)} \tag{2.8}$$

$$C_2 = \frac{2C_{34} + k_c^2(C_{12} - C_{34}) + k_c\sqrt{k_c^2(C_{12} - C_{34})^2 + 4C_{12}C_{34}}}{2(1 - k_c^2)} \tag{2.9}$$

In CPT systems, C_{12} and C_{34} are typically constant capacitances. Thus, C_p and C_s vary primarily with k_c, as illustrated in Fig. 2-7. It should be noted from this figure that C_p

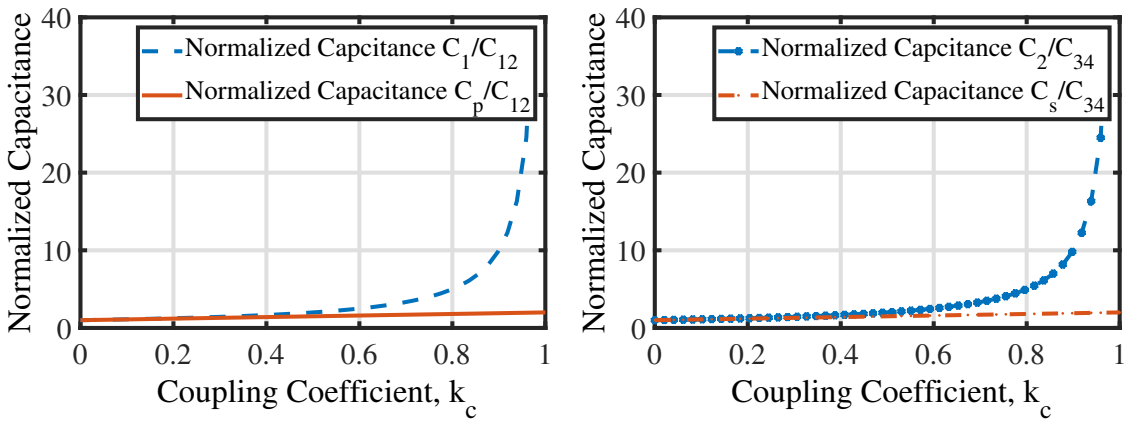


Figure 2-7: The variation of the of normalized capacitance verse coupling coefficient (a) the primary side capacitance C_1/C_{21} and C_p/C_{21} (b) the secondary side capacitance C_2/C_{34} and C_s/C_{34}.

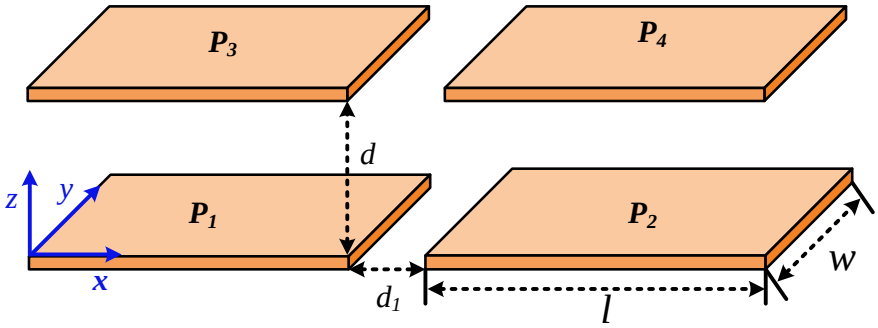


Figure 2-8: Rectangular value plate for Ansys Maxwell simulation.

and C_s remain almost constant despite the variation in k_c. In contrast, C_1 and C_2 vary significantly as k_c changes.

2.2.2 Simulation Verification

To verify the analysis, a simulation was built in the FEA tool Ansys Maxwell. Four identical rectangular plates were used to form a capacitive coupler. Fig. 2-8 shows the structure and dimensions of the plates. The plate dimensions are length l = 600 mm and width w = 600 mm. The horizontal distance between the primary and secondary sets of plates is denoted by d, and the distance between two plates on the same side is d_1. In the simulation, equivalent capacitances were obtained by assigning a 0 V potential to plates P_2, P_3, and P_4, and a 1 V potential to plate P_1. Therefore, the six capacitance parameters could be directly measured. The simulation data were then used to calculate C_p, C_s, C_1, and C_2 based on

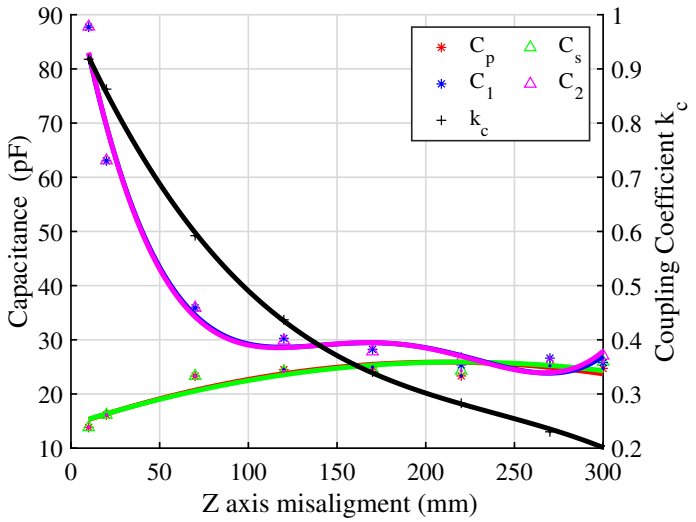


Figure 2-9: The variation of capacitances C_1, C_2, C_s, C_p and coupling coefficient k_c under Z-axis misalignment.

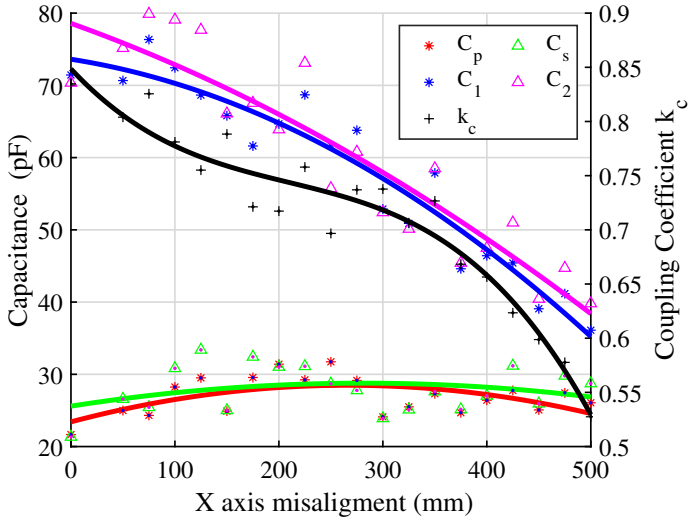


Figure 2-10: The variation of capacitances C_1, C_2, C_s, C_p and coupling coefficient k_c under X-axis misalignment.

(2.6), (2.7) (2.8), (2.9).

In the first scenario, the vertical distance d between the primary and secondary plates is varied from 10 mm to 300 mm. The variations of the internal capacitances of the six-capacitor model are not explicitly shown here but are known to be strongly coupling-dependent, as charge absorption and distribution are closely related to the relative positions of the plates. Consequently, the coupling coefficient k_c decreases as d increases.

Fig. 2-9 illustrates the behavior of derived parameters: it shows that C_1 and C_2 are strongly dependent on the coupling. In contrast, both C_p and C_s remain relatively constant, as also shown in Fig. 2-9. This implies that C_m is only the primary coupling-dependent

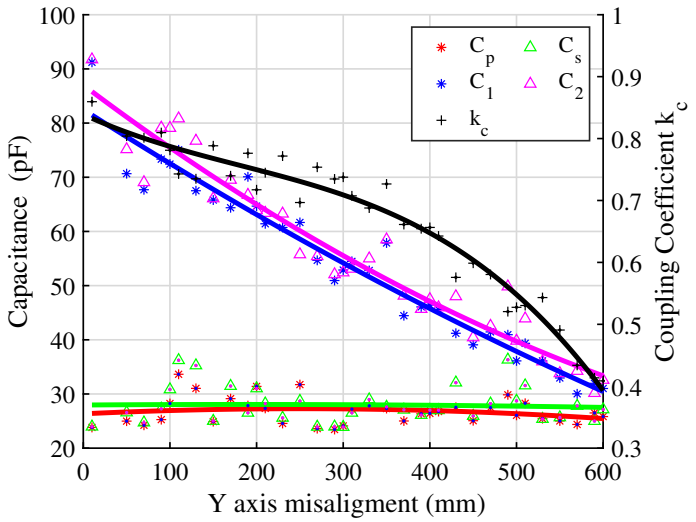


Figure 2-11: The variation of capacitances C_1, C_2, C_s, C_p and coupling coefficient k_c under Y-axis misalignment.

capacitance.

In addition to vertical distance variations, misalignment conditions are also investigated. With d fixed at 50 mm, the primary side plates are moved along the X and Y axes. The corresponding variations in the derived capacitance parameters are summarized in Figs. 2-10 and 2-11, respectively. From these results, a similar conclusion can be drawn as from Fig. 2-9, the open-circuit self-capacitances C_p and C_s are almost coupling-independent, while C_1, C_2, and C_m vary with misalignment.

Furthermore, as the distance d increases, the effective primary-side capacitance C_1 tends to converge towards the value of C_p as shown in Fig. 2-9. In the weak coupling region, C_1 also becomes less sensitive to coupling variations. Therefore, the benefit of model with C_p and C_s is coupling independence. The choice of model is closely related to application specifications such as coupler size, transfer distance, and misalignment tolerance. For applications requiring strong coupling, like the charging of small devices, employing the model based on the mialigment-insensitive parameters C_p and C_s is particularly attractive.

2.2.3 Experimental Verification

To verify the analysis, a prototype of the capacitive coupler was constructed using four aluminum plates (600 mm x 600 mm), as shown in Fig. 2-12. Due to the symmetrical structure of the coupler, only the capacitances C_p and C_1 were measured. According to two-port network theory, C_p was measured by leaving the secondary side open-circuited, while

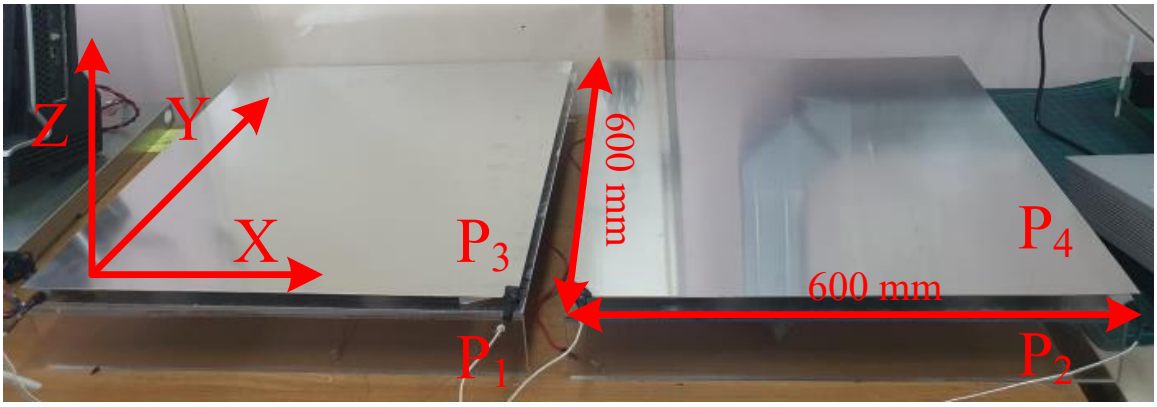


Figure 2-12: Experimental setup of capacitive coupler.

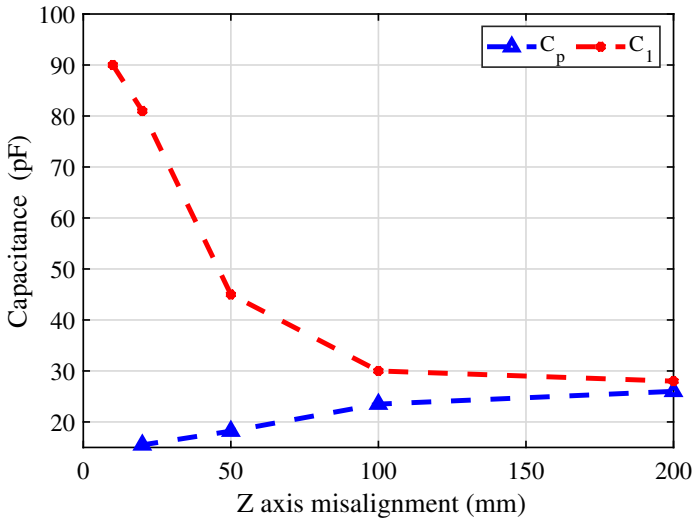


Figure 2-13: Experimental results of capacitive coupler under Z axis misalignment.

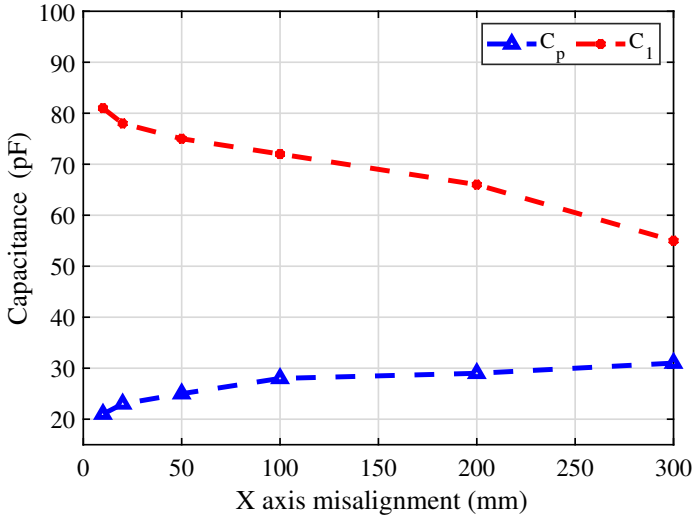


Figure 2-14: Experimental results of capacitive coupler under X axis misalignment.

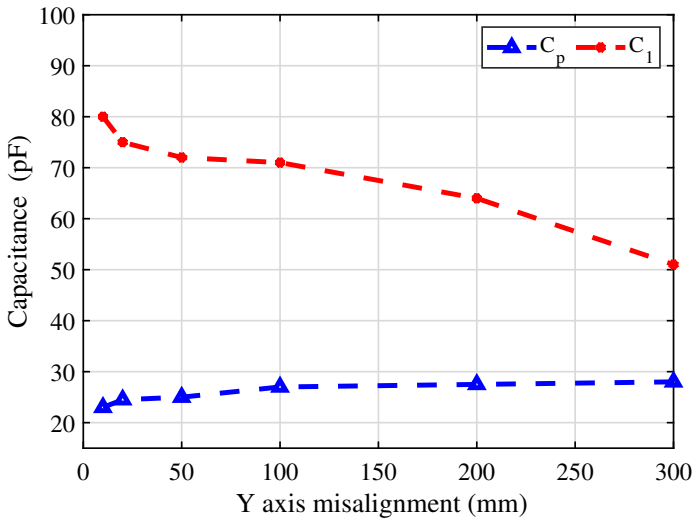


Figure 2-15: Experimental results of capacitive coupler under Y axis misalignment.

C_1 was measured by short-circuiting the secondary side.

Misalignment along the Z-axis was tested by varying the distance, Z, from 10 mm to 200 mm. The experimental results, shown in Fig. 2-13, demonstrate that C_p remained almost constant during Z-axis misalignment, whereas C_1 was highly dependent on the coupling distance. These experimental results show good agreement with the theoretical analysis and simulation results. Likewise, similar behavior was observed for misalignment along the X-axis and Y-axis, as shown in Fig.2-14 and Fig.2-15, respectively.

2.3 Compensation Topology

From the analysis in the previous section, the capacitances C_p and C_s were shown to be almost constant under misalignment conditions. This characteristic could be beneficial for misalignment compensation and for parameter identification in primary-side control schemes. To further analyze these features, the π-equivalent two-port network of the capacitive coupler is examined. From this π-equivalent circuit model, the four basic sets of two-port network parameters namely, z-parameters, y-parameters, g-parameters, and h-parameters can be expressed as follows:

The four z-parameter are:

$$z_{11} = \left.\frac{V_1}{I_1}\right|_{I_2=0} = \frac{1}{j\omega C_p} \tag{2.10}$$

$$z_{12} = \left.\frac{V_1}{I_2}\right|_{I_1=0} = \frac{1}{j\omega C_m(1/k_C^2 - 1)} \tag{2.11}$$

$$z_{21} = \left.\frac{V_2}{I_1}\right|_{I_2=0} = \frac{1}{j\omega C_m(1/k_C^2 - 1)} \tag{2.12}$$

$$z_{22} = \left.\frac{V_2}{I_2}\right|_{I_1=0} = \frac{1}{j\omega C_s} \tag{2.13}$$

The four y-parameter are:

$$y_{11} = \left.\frac{I_1}{V_1}\right|_{V_2=0} = \frac{j\omega C_p}{1-k_c^2} \tag{2.14}$$

$$y_{12} = \left.\frac{I_1}{V_2}\right|_{V_1=0} = -j\omega C_m \tag{2.15}$$

$$y_{21} = \left.\frac{I_2}{V_1}\right|_{V_2=0} = -j\omega C_m \tag{2.16}$$

$$y_{22} = \left.\frac{I_2}{V_2}\right|_{V_1=0} = \frac{j\omega C_s}{1-k_c^2} \tag{2.17}$$

The four h-parameter are:

$$h_{11} = \left.\frac{V_1}{I_1}\right|_{V_2=0} = \frac{1-k_c^2}{j\omega C_p} \tag{2.18}$$

$$h_{12} = \left.\frac{V_1}{V_2}\right|_{I_1=0} = \frac{C_m(1-k_c^2)}{C_p} \tag{2.19}$$

$$h_{21} = \left.\frac{I_2}{I_1}\right|_{V_2=0} = -\frac{C_m(1-k_c^2)}{C_p} \tag{2.20}$$

$$h_{22} = \left.\frac{I_2}{V_2}\right|_{I_1=0} = j\omega C_s \tag{2.21}$$

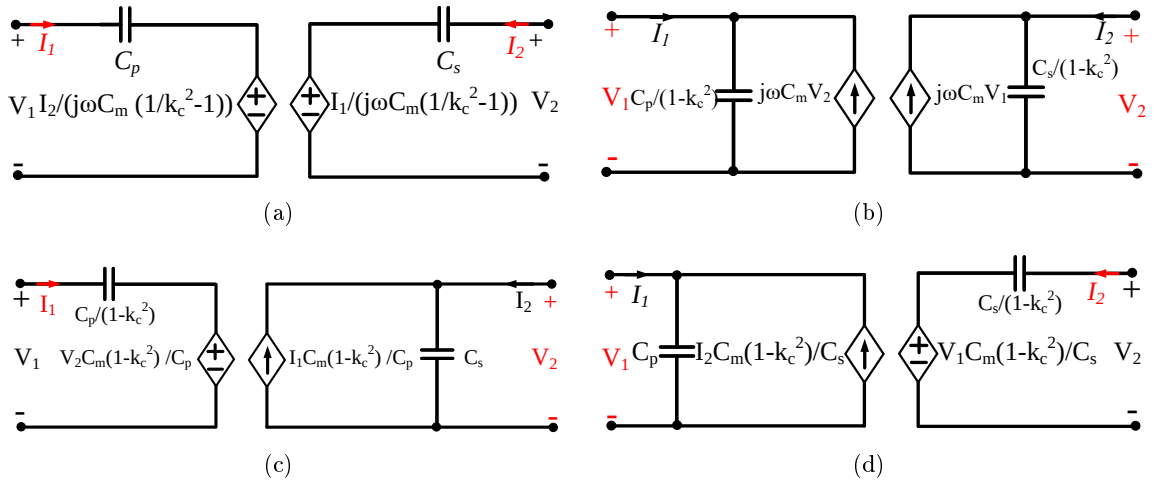


Figure 2-16: Equivalent circuit of capacitive coupler for (a) z-parameter (b) y-parameter (c) h-parameter (d) g-parameter.

The four g-parameter are:

$$g_{11} = \left.\frac{I_1}{V_1}\right|_{I_2=0} = j\omega C_p \tag{2.22}$$

$$g_{12} = \left.\frac{I_1}{I_2}\right|_{V_1=0} = -\frac{C_m(1-k_c^2)}{C_s} \tag{2.23}$$

$$g_{21} = \left.\frac{V_2}{V_1}\right|_{I_2=0} = \frac{C_m(1-k_c^2)}{C_s} \tag{2.24}$$

$$g_{22} = \left.\frac{V_2}{I_2}\right|_{V_1=0} = \frac{1-k_c^2}{j\omega C_s} \tag{2.25}$$

Equivalent circuit of capacitive coupler for z-parameters, y-parameters, h-parameters, and g-parameters are shown in Fig. 2-16. An compensation network is needed to compensate for the coupler's capacitance. Before investigating compensation networks further, the basic requirements for compensation can be listed as follows [66, 67]:

- A square wave voltage source connecting in parallel to a shunt capacitor is not allowed due to the large current spikes that occur in the source during switch state transitions.
- A current source connected in series with an inductor should be avoided due to high voltage spikes.
- A current source series with a capacitor, the resultant topology is non-resonantly coupled.

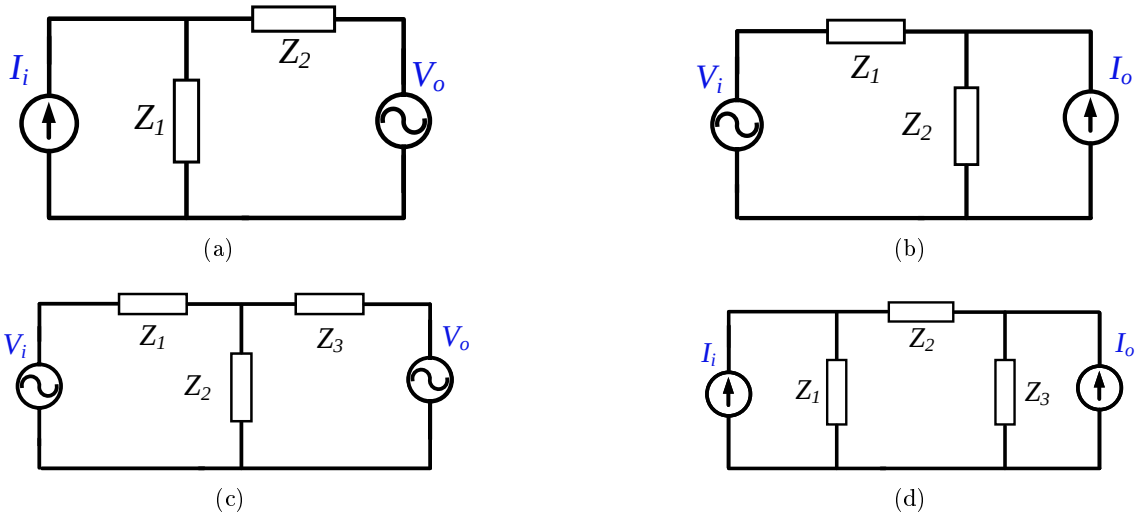


Figure 2-17: Compensation network (a) L-type for ICS (b) L-type for IVS (c) T-type for IVS (d) π-type for ICS.

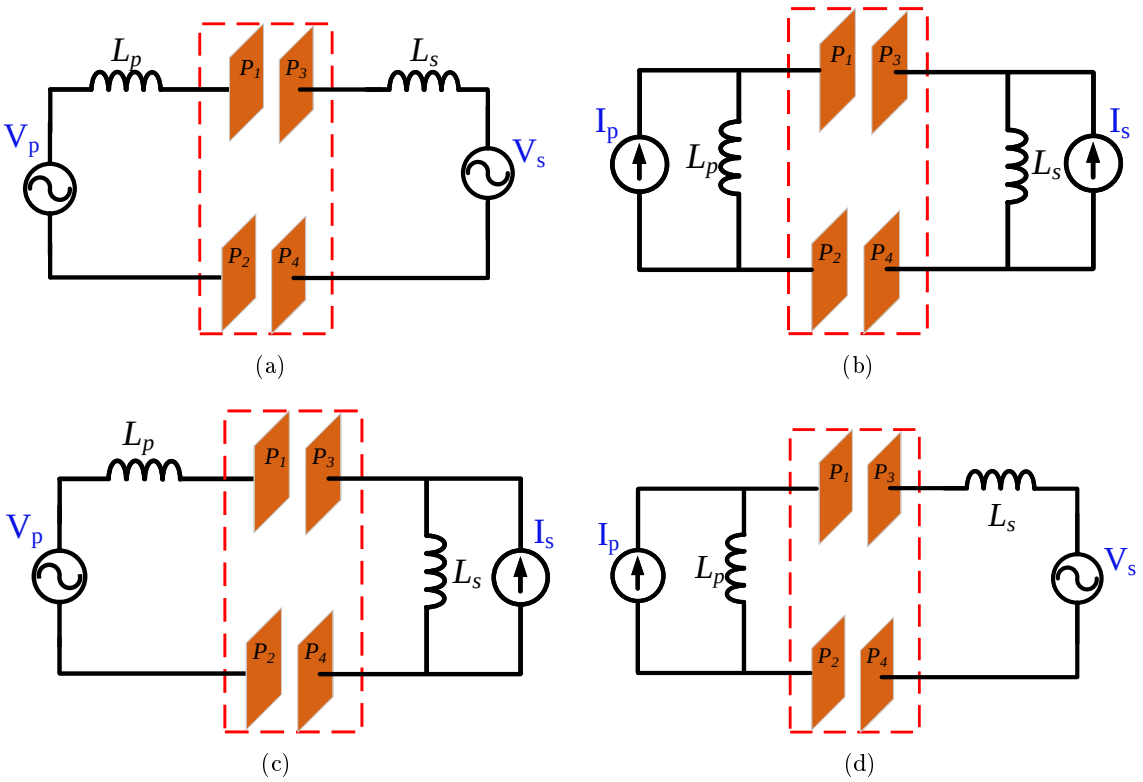


Figure 2-18: Four basic CPT compensations (a) series-series (b) parallel-parallel (c) series-parallel (d) parallel-series.

- A voltage source parallels with an inductor, the resultant topology is also non-resonantly coupled.

According to these basic requirements, possible general compensation configurations include T-type for an Input Voltage Source (IVS), π-type for an Input Current Source (ICS), L-type for an ICS, and L-type for an IVS, as illustrated in Fig. 2-17. When self-inductance is employed to resonate with the capacitive coupler, elements can be added in series or parallel on both the primary and secondary sides which is form of L-type for an ICS, and L-type for an IVS as shown in Fig. 2-18. This results in four basic compensation topologies: series-series (SS) [29, 68], parallel-parallel (PP), series-parallel (SP) [69], and parallel-series (PS) [70] as shown in Fig. 2-19. These topologies are well-suited for analysis using z-parameters, y-parameters, h-parameters, and g-parameters respectively. The zero phase angle frequency of four basic compensation can be expressed as follows

$$\omega_{ss} = \frac{1}{\sqrt{L_p C_p}} = \frac{1}{\sqrt{L_s C_s}} \tag{2.26}$$

$$\omega_{pp} = \frac{1}{\sqrt{\frac{L_p C_p}{1-k_c^2}}} = \frac{1}{\sqrt{\frac{L_s C_s}{1-k_c^2}}} \tag{2.27}$$

$$\omega_{sp} = \frac{1}{\sqrt{\frac{L_p C_p}{1-k_c^2}}} = \frac{1}{\sqrt{L_s C_s}} \tag{2.28}$$

$$\omega_{ps} = \frac{1}{\sqrt{L_p C_p}} = \frac{1}{\sqrt{\frac{L_s C_s}{1-k_c^2}}} \tag{2.29}$$

where ω is are the angular resonant frequency of primary and secondary. It should be noted that only ω_{ss} is constant with the variation of k_c, thus zero phase angle of SS compensation is constant during the misalignment. Therefore, the CPT with SS compensated on both sides is recommended for misalignment mitigation. This feature can be also used for parameters identification for primary side control of CPT system, the variation of capacitive coupler can be simplified by coupling coefficient variation only.

By utilizing these fixed self-capacitances for resonance, the resulting resonant frequency naturally becomes independent of coupling. Furthermore, the zero-phase-angle (ZPA) frequency of this SS configuration also remains constant under misalignment conditions. Therefore, a CPT system with SS compensation on both sides is recommended for misalignment mitigation.

High-order compensation can be employed to enhance misalignment tolerance and reduce component stress [33, 71, 72]. Such compensation often utilizes T-type configurations for IVS or π-type configurations for an ICS, leading to well-known topologies like LLC, CLL, and

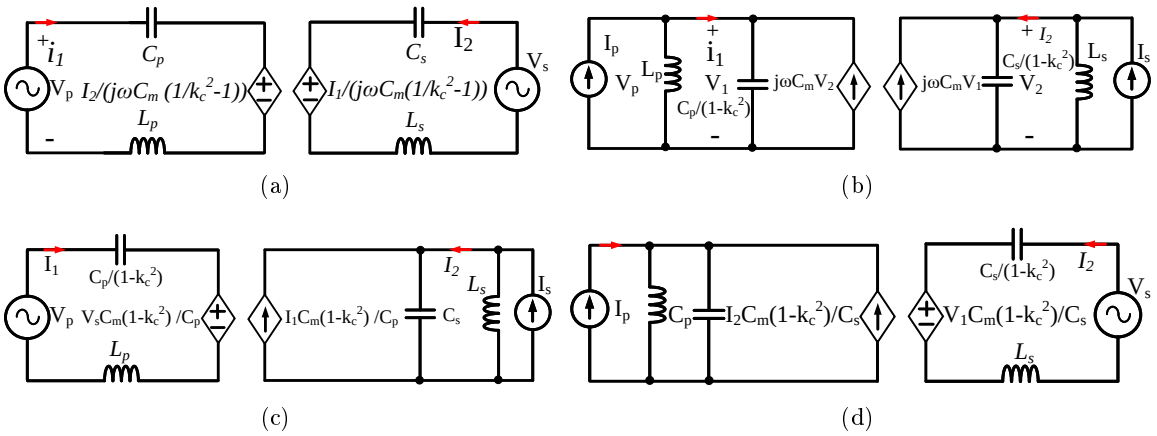


Figure 2-19: Equivalent circuit of four basic CPT compensations (a) series-series (b) parallel-parallel (c) series-parallel (d) parallel-series.

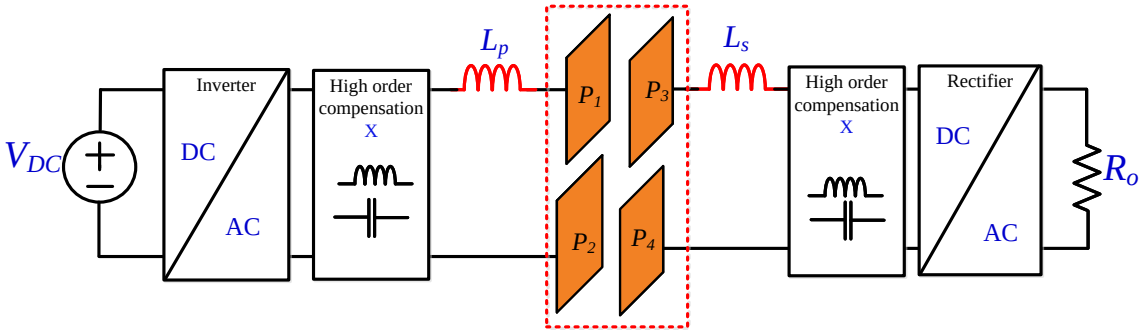


Figure 2-20: Recommended structure X-SS-X for with high order compensation of capacitive power transfer system for misalignment mitigation.

CLC [31, 73]. In these contexts, X-SS-X compensated topologies are highly recommended for robust misalignment mitigation, as depicted in Fig. 2-20, where the 'X' component in these topologies typically refers to an additional T-type or π-type compensation network (e.g., forming LLC, CLL, or CLC structures), and this concepts are further detailed in [74, 75].

To minimize the number of passive components, a principle often advocated, series compensation is a preferred approach for addressing misalignment. Therefore, T-type configurations for high-order compensation are generally recommended for system with IVS, as series compensation can be considered an integral part of the T-circuit model. This characteristic is advantageous for parameter identification in the primary-side control of CPT systems. In such an arrangement, variations in the capacitive coupler's behavior can be largely attributed to changes in coupling, thereby simplifying the model.

2.4 Conclusion

A selection guideline for compensation networks aimed at mitigating misalignment effects has been presented. It is shown that the zero-phase-angle (ZPA) frequency of the series–series (SS) configuration remains constant under misalignment conditions. Therefore, a CPT system employing SS compensation on both the primary and secondary sides is recommended for effective misalignment mitigation. Furthermore, X-SS-X compensated topologies are strongly recommended for enhanced robustness against misalignment. The proposed analysis has been verified through both simulation and experimental results.

Chapter 3

Parameter Identification for Primary-Side Control

Primary-side control is essential in capacitive wireless power transfer (CPT) systems. In this thesis, z-parameters model is adopted to represent the CPT coupler by approximating it with two constant self-capacitances, thereby simplifying its behavior to closely match that of an inductive system and eliminating coupler complexity. Mutual capacitance and load resistance are identified to enable accurate output-voltage regulation. In this chapter, by incorporating resonant-frequency tracking into the voltage-regulation loop, a novel primary-side control strategy for the CPT system is proposed, eliminating the need for measurement and communication modules at the receiver. A sensitivity analysis and modeling are also presented to guide the design process. The proposed methods are validated through both simulation and experimental results.

3.1 Introduction

Controllers play a crucial role in this context, as they continuously monitor performance and adjust their parameters in real-time to handle variations in operating conditions, such as changes in load or coupler misalignment, thus ensuring optimal power transfer and efficiency [76, 77]. For instance, in a CPT system, the controller can tune both the frequency and matching networks on both the primary and secondary sides to maintain stable operation under varying conditions, ensuring high performance without manual operation [22, 23]. A practical example in CPT systems where load variations cannot be ignored is the behavior of electric vehicle (EV) batteries during regenerative braking [6–8]. This leads to varia-

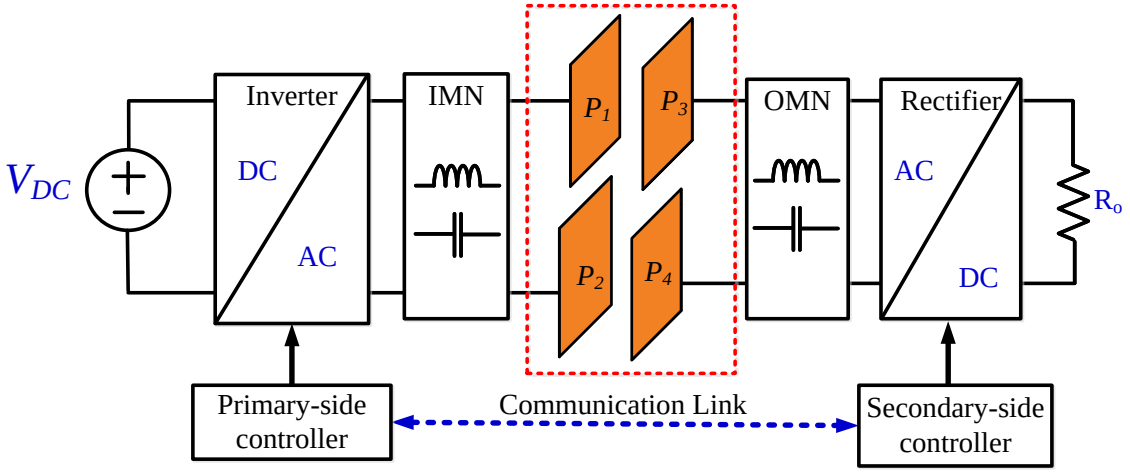


Figure 3-1: Overall CPT system configuration.

tions in the equivalent load resistance, which in turn cause variations in the output power and voltage [78]. As such, closed-loop control for such systems is essential. Depending on the controller's location, closed-loop control techniques described in earlier studies can be divided into three categories: primary-side control, secondary-side control, and dual-side control [45, 79]. In the dual-side control technique, the full-bridge inverter in the primary circuit is often utilized to accomplish frequency tracking. Impedance matching is accomplished by controlling the compensation circuits on the primary and secondary sides, typically through the use of additional controllable inductors [80–82].

The integrated frequency tracking and matching network optimizes the target current to the secondary side under ideal power transfer conditions; however, it requires expensive and challenging-to-manage controllable inductors. Previous research proposed a secondary-side control technique using a half-bridge inverter on the primary side, coupled with a DC-DC buck-boost converter to control equivalent output resistance [37, 83–86]. Although this approach can optimize resistance against load variations by tracking the maximum power point, it adds complexity and cost through additional components. Conversely, primary-side control techniques discussed in studies also face challenges. While Class E inverters are employed in managing power transfer, using additional capacitors increases component count and system complexity [87]. Some papers present a primary-side control technique for the WPT system that does not need additional components or wireless feedback [45, 77, 88]. By using only one voltage sensor, this technique estimates the output voltage from the measured voltage across a primary-side capacitor, regulating it via the full-bridge inverter with modified sine wave control.

Primary-side control can be categorized into three types: fixed frequency, variable frequency, and hybrid control techniques [45, 76]. In fixed frequency control, the operating frequency remains above the resonant frequency, with the duty ratio adjusted for voltage regulation. A key drawback of this method is the potential loss of zero-voltage switching across a wide range of output voltages. In contrast, variable frequency control allows for a broader range of output voltages and enables soft-switching, but it can increase switching losses and complicate compliance with electromagnetic interference (EMI) standards. Hybrid control techniques blend both approaches but necessitate complex algorithms for effective output regulation.

In accordance with the various placements of the controller, the generally utilized control techniques for constant current (CC) and constant voltage (CV) charging of CPT systems may be classified into three groups: the secondary-side control method, the primary-side control method, and control involving both primary and secondary sides [89, 90]. The secondary-side control technique involves configuring the controller on the secondary side, often known as local control. This technique allows for CC and CV charging control by manipulating the DC-DC converter on the secondary side or an actively controlled rectifier [91]. The benefit of the secondary-side control technique is that it eliminates the wireless communication module [92]. Inevitably, the DC-DC converter will increase the secondary side's size, weight, and expense, which might be unfavorable for some specialized applications [93]. In addition, the operation of a secondary-side active rectifier necessitates a sophisticated synchronous rectifier control mechanism and hardware circuit [29, 51, 94]. When it comes to unmanned aerial vehicles (UAVs), autonomous underwater vehicles (AUVs), and other electrical devices with a restricted battery capacity, the receiving side should be kept as small and light as feasible [9–11]. As a result, for these use cases, the primary-side control method is preferred over the secondary-side control technique.

The primary-side control technique involves configuring the controller on the primary side and managing the current or voltage during charging via the primary-side DC-DC converter or full-bridge inverter. For this reason, the primary-side control approach compensates for the deficiencies of the secondary-side control method. Positioning the control circuit on the primary side can significantly minimize both the volume and weight of the secondary side. Nonetheless, the primary-side control technique frequently depends upon the wireless communication component to reply to information of charging, which drives up extra hardware and software expenses, and strong magnetic fields could have an influence on communica-

tion stability. Furthermore, certain applications, such as undersea and aerospace, do not lend themselves to wireless communication [62]. Besides, the system's dynamic adjustment performance could be influenced by the significant time delay of the wireless connection module.

To circumvent the issues of the primary-side control method, the control method depends on primary-side identification of parameters, which has sparked the interest of academics. The fundamental premise of this sort of control technique is to find unknown parameters on the secondary-side via measurement of primary-side signals and then using the acquired identification outcomes to the controller to accomplish output control of the system [95]. This type of control strategy has the advantage of requiring only a single controller on the primary side to attain the system's output control. This eliminates the need for a wireless communication module, thereby lowering both the expense and complications of the system.

3.2 Modeling and Compensation of Capacitive Coupler

The capacitive coupler of CPT system contains four plates $P_1 \sim P_4$ shown in Fig. 3-2, for accuracy six capacitor model is commonly used for capacitive coupler modeling. Moreover,

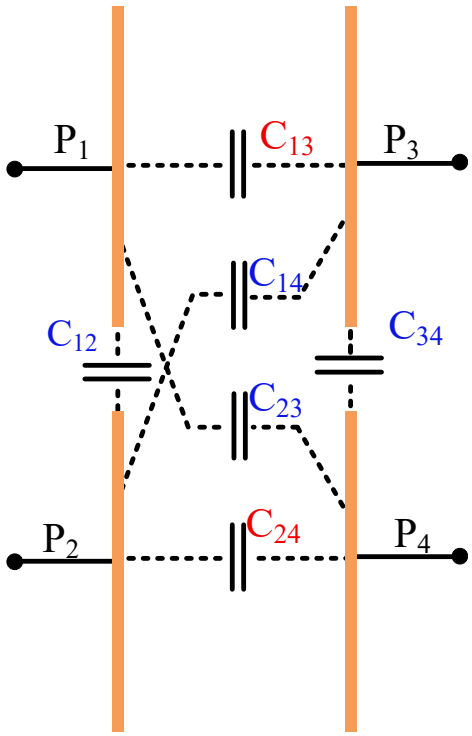


Figure 3-2: Capacitive coupler

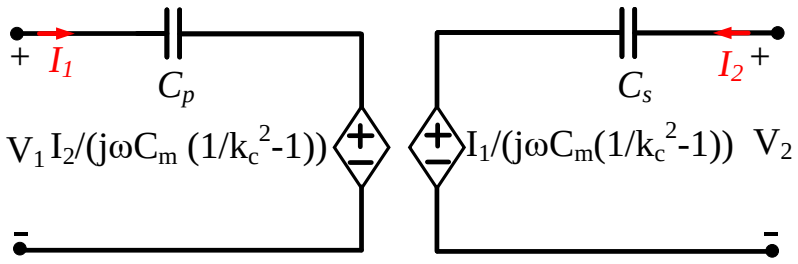


Figure 3-3: Equivalent circuit of capacitive coupler.

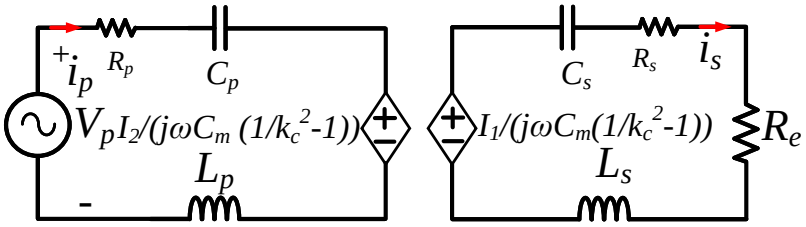


Figure 3-4: Equivalent circuit of SS-compensated CPT system.

it can be simplified by two port model as shown in Fig. 3-3 where C_1, C_2, C_m, C_p, C_s are capacitances and C_m is the equivalent mutual capacitance, and k_c is coupling coefficient [50, 65] which are given by

$$\begin{cases} C_1 = C_{12} + \dfrac{(C_{13}+C_{14})(C_{23}+C_{24})}{C_{13}+C_{14}+C_{23}+C_{24}} \\ C_2 = C_{34} + \dfrac{(C_{13}+C_{23})(C_{14}+C_{24})}{C_{13}+C_{14}+C_{23}+C_{24}} \\ C_m = \dfrac{C_{13}C_{24}-C_{14}C_{23}}{C_{13}+C_{14}+C_{23}+C_{24}} \\ C_p = (1-k_c^2)C_1 \\ C_s = (1-k_c^2)C_2 \\ k_c = \dfrac{C_m}{\sqrt{C_1C_2}} = \dfrac{C_m(1-k_c^2)}{\sqrt{C_pC_s}} \end{cases} \tag{3.1}$$

A detailed derivation are given by Chapter 2. V_1 and V_2 represent the voltages at the terminals of the input and the output of the capacitive coupler, respectively. I_1 and I_2 represent the current at the terminals of the input and the output of the capacitive coupler, respectively.

From the analysis of Chapter 2, the capacitances C_p and C_s are observed to remain almost constant during the misalignment cases and series-series (SS) compensated on both sides is recommended for misalignment mitigation as shown in Fig. 3-4. This stability could be beneficial for misalignment compensation and parameter identification of the primary side

control. By identifying fixed self-capacitances the resulting resonant frequency is naturally independent of coupling. The zero phase angle frequency is given by

$$\omega_o = \frac{1}{\sqrt{L_p C_p}} = \frac{1}{\sqrt{L_s C_s}} \tag{3.2}$$

where ω_o is are the angular resonant frequency of primary and secondary. It should be noted that the zero phase angle of this is also constant during the misalignment. Therefore, the CPT with series-series (SS) compensation is recommended for misalignment mitigation. This feature can be also used for parameters identification for primary side control of CPT system, the variation of capacitive coupler can be simplified by coupling variation only.

3.3 Proposed Primary-Side Estimation Method

3.3.1 CPT System Structure

The circuit diagram of the CPT system is shown in Fig. 3-5. The full-bridge inverter is used to generate the square wave and provide voltage regulation with four switches, S_1-S_4. L_s and L_p are the compensation inductors for the primary and secondary sides, respectively. R_s and R_p represent the equivalent parasitic resistances. Moreover, the key waveforms of the SS-compensated CPT system are shown in Fig. 3-6. A six-capacitor model is used to model the capacitive coupler. A full-wave diode rectifier with four diodes, D_1-D_4, is used to convert the AC to DC, and C_f is used as a filter capacitor. The resistor R_o is used as a load. The equivalent circuit of the SS-compensated CPT system with the capacitive coupler is shown in Fig. 3-4. Applying the fundamental approximation, the equivalent circuit can

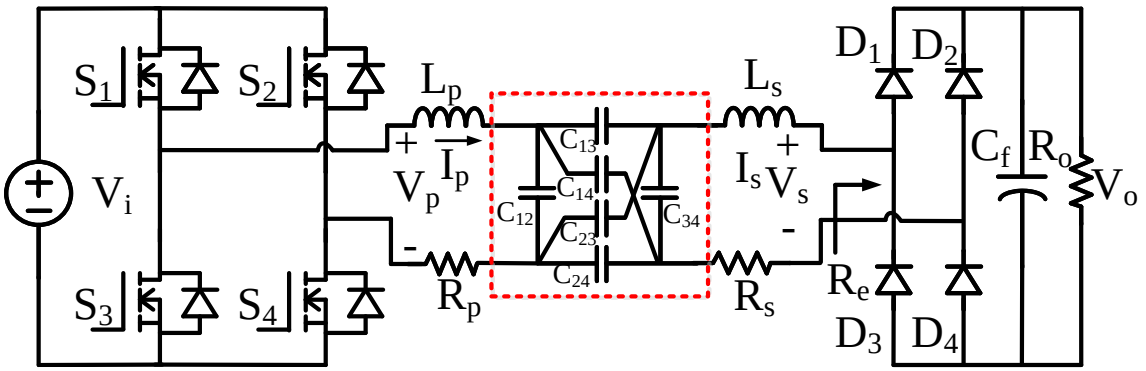


Figure 3-5: Circuit diagram of the SS-compensated CPT system with a full-bridge inverter and full-wave rectifier.

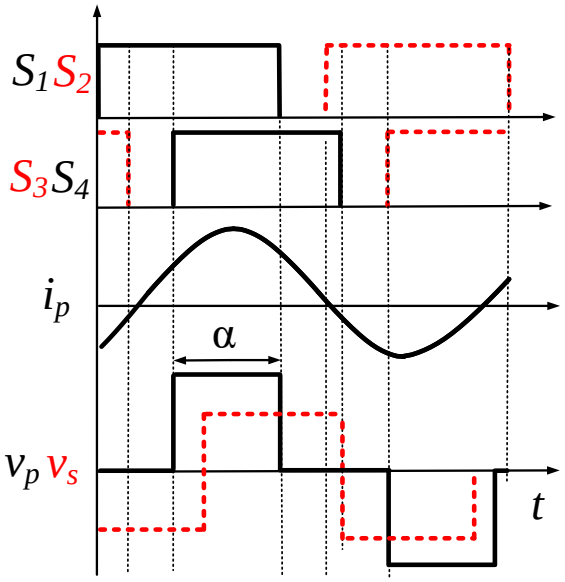


Figure 3-6: Key waveforms of the SS-compensated CPT system.

be described in the frequency domain as follows

$$V_p = \left(R_p + j\omega_s L_p + \frac{1}{j\omega_s C_p}\right) i_p + \frac{i_s}{j\omega_s C_m} \tag{3.3}$$

$$0 = \frac{i_p}{j\omega_s C_m} + \left(R_s + R_e + j\omega_s L_s + \frac{1}{j\omega_s C_s}\right) i_s \tag{3.4}$$

where ω_s is the switching angular frequency of the WPT system. Based on (3.3) and (3.4), the equivalent input impedance of the system, Z_{in} can be calculated as

$$Z_{in} = \frac{V_p}{I_p} = R_{in} + j\mathrm{X}_{in} \tag{3.5}$$

where

$$R_{in} = R_p + \frac{(R_e + R_s)\frac{1}{{C_m}^2{\omega_s}^2}}{\left[(R_e + R_s)^2 + \left(\frac{\omega_s}{\omega_{os}} - 1\right)^2 \frac{1}{C_s^2\omega_s^2}\right]} \tag{3.6}$$

$$X_{in} = \left(\frac{\omega_s^2}{\omega_{op}^2} - 1\right)\frac{1}{C_p\omega_s} - \frac{\left(\frac{{\omega^2}_s}{\omega_{os}} - 1\right)\frac{1}{{C_m}^2 C_s {\omega_s}^3}}{\left[(R_e + R_s)^2 + \left(\frac{{\omega^2}_s}{\omega_{os}} - 1\right)^2 \frac{1}{{C_s}^2{\omega_s}^2}\right]} \tag{3.7}$$

where ω_{op} and ω_{os} are the angular transmitter resonant frequency and angular receiver resonant frequency, respectively. Based on (3.6) and (3.7), we can have the following relationship

$$\frac{\left(\frac{\omega_s^2}{\omega_{op}^2}-1\right)\frac{1}{C_p\omega_s}-X_{in}}{\left(\frac{{\omega^2}_s}{\omega_{os}}-1\right)\frac{1}{{C_m}^2C_s{\omega_s}^3}}=\frac{R_{in}-R_p}{(R_e+R_s)\frac{1}{{C_m}^2{\omega_s}^2}}. \tag{3.8}$$

After some derivation, the equivalent load R_e can be determined as

$$R_e=\frac{(R_{in}-R_p)\left(\frac{{\omega^2}_s}{\omega_{os}}-1\right)\frac{1}{C_s\omega_s}}{\left(\frac{\omega_s^2}{\omega_{op}^2}-1\right)\frac{1}{C_p\omega_s}-X_{in}}-R_s \tag{3.9}$$

Subtracting (3.9) to (3.6), the mutual capacitance C_m can be determined as

$$C_m=\sqrt{\frac{R_e+R_s}{(R_{in}-R_p)\,{\omega_s}^2\left[(R_e+R_s)^2+\left(\frac{{\omega^2}_s}{\omega_{os}}-1\right)^2\frac{1}{C_s^2\omega_s^2}\right]}} \tag{3.10}$$

The mutual capacitance C_m can be obtained by the estimated equivalent resistance R_e. In practical, R_{in} and X_{in} can be determined when I_p and V_p are measured, and which can be calculated by

$$R_{in}=\frac{V_{p,RMS}}{I_{p,RMS}}\cos(\phi) \tag{3.11}$$

$$X_{in}=\frac{V_{p,RMS}}{I_{p,RMS}}\sin(\phi) \tag{3.12}$$

where $V_{p,\mathrm{RMS}}$ and $I_{p,\mathrm{RMS}}$ are the root-mean-square (rms) values of V_p and I_p, respectively, and ϕ is the phase difference between I_p and V_p and these values are measurable in hardware. From the both estimated value of C_m and R_e, subtracting (3.9) and (3.10) to (3.4), the secondary side rms current is given by

$$I_s=\left|\frac{I_p}{j\omega C_m\left(j\omega L_s+\frac{1}{j\omega C_s}+R_s+\mathrm{R}e\right)}\right|. \tag{3.13}$$

Equivalent ac resistor R_e is presented by the full wave rectifier load [96], the output current I_o and the output load resistance are given by

$$I_o=\frac{2\sqrt{2}}{\pi}I_s, R_o=\frac{\pi^2}{8}R_e \tag{3.14}$$

Table 3.1: System parameters.

Symbol	Parameters	Values	Unit
V_s	DC Input Voltage	200	V
V_o	Output Input Voltage	150	V
f_s	Switching frequency	200	kHz
L_s	Resonant tank inductance	300	μH
L_p	Resonant tank inductance	300	μH
C_s	Link capacitance	210	pF
C_p	Link capacitance	215	nF
C_f	Output filler capacitance	500	μF
R_L	Load resistance	50	Ω

Therefore, the output voltage V_s is give by

$$V_s = \frac{\pi}{2\sqrt{2}} I_s R_e \tag{3.15}$$

The output voltage can be estimated directly by measured current and voltage at primary side. Therefore, the output voltage can be regulated with primary side control without communication need.

3.4 Sensitivity Analysis

The proposed parameters identification algorithm relies on the primary-side voltage and current measurement. However, there are unavoidable measurement errors and tolerance component that influence to the accuracy of estimates results. The sensitivity analyses of the main parameter drifts on estimated mutual capacitance and load resistance can be carried out. During the resonant tracking procedure, the amplitude of the induced voltage across the receiver side is strongly influenced by the frequency step size. Therefore, this can affect the accuracy estimation.

In order to analyze the influence on the accuracy of the estimated parameters, a sensitivity analysis is performed. The concept of normalized differential sensitivity is adopted in this chapter [103]. The mathematical definition of sensitivity of y respective to x is shown as

$$S_x^y = \lim_{\Delta x \to 0} \left\{ \frac{\frac{\Delta y}{y}}{\frac{\Delta x}{x}} \right\} = \frac{x}{y} \frac{\partial y}{\partial x}. \tag{3.16}$$

From (3.9) the sensitive analysis is applied for estimated equivalent load resistance R_e.

$$S_{R_{in}}^{R_e} = \frac{R_{in}\left(L_s\omega_s + \frac{1}{C_p\omega_s}\right)}{R_e\left(L_p\omega_s - X_{in} + \frac{1}{C_s\omega_s}\right)} \tag{3.17}$$

$$S_{X_{in}}^{R_e} = \frac{X_{in}\left(L_s\omega_s + \frac{1}{C_p\omega_s}\right)\ (R_{in} - R_p)}{R_e\left(L_p\omega_s - X_{in} + \frac{1}{C_s\omega_s}\right)^2} \tag{3.18}$$

$$S_{L_p}^{R_e} = -\frac{\omega_s L_p\left(L_s\omega_s + \frac{1}{C_p\omega_s}\right)\ (R_{in} - R_p)}{R_e\left(L_p\omega_s - X_{in} + \frac{1}{C_s\omega_s}\right)^2} \tag{3.19}$$

$$S_{L_s}^{R_e} = \frac{L_s\omega_s\ (R_{in} - R_p)}{R_e\left(L_p\omega_s - X_{in} + \frac{1}{C_s\omega_s}\right)} \tag{3.20}$$

$$S_{C_p}^{R_e} = \frac{\sqrt{R_e + R_s}\left(L_s\omega_s + \frac{1}{C_p\omega_s}\right)}{R_e C_p\omega_s^2\sqrt{R_{in} - R_p}A^{3/2}} \tag{3.21}$$

$$S_{C_s}^{R_e} = \frac{\left(L_s\omega_s + \frac{1}{C_p\omega_s}\right)\ (R_{in} - R_p)}{R_e C_s\omega_s\left(L_p\omega_s - X_{in} + \frac{1}{C_s\omega_s}\right)^2} \tag{3.22}$$

where $A = (R_e + R_s)^2 + \left(L_s\omega_s + \frac{1}{C_p\omega_s}\right)^2$. From (3.10) the sensitive analysis is applied for the mutual capacitance C_m

$$S_{R_e}^{C_m} = \frac{R_e\left[\left(L_s\omega_s + \frac{1}{C_p\omega_s}\right)^2 - (R_e + R_s)^2\right]}{2C_m\omega_s\sqrt{R_{in} - R_p}\sqrt{R_e + R_s}A^{3/2}} \tag{3.23}$$

$$S_{R_{in}}^{C_m} = -\frac{R_{in}\sqrt{R_e + R_s}}{2C_m\omega_s(R_{in} - R_p)^{3/2}\sqrt{A}} \tag{3.24}$$

$$S_{L_s}^{C_m} = -\frac{L_s\sqrt{R_e + R_s}\left(L_s\omega_s + \frac{1}{C_p\omega_s}\right)}{C_m(R_{in} - R_p)^{3/2}A^{3/2}} \tag{3.25}$$

$$S_{C_s}^{C_m} = \frac{\sqrt{R_e + R_s}\left(L_s\omega_s + \frac{1}{C_s\omega_s}\right)}{C_m C_s\omega_s^2\sqrt{R_{in} - R_p}A^{3/2}} \tag{3.26}$$

System parameters from Table 3.1 are used for the sensitivity analysis. Normalized parameter sensitivities of the estimated load resistance, R_e, with respect to R_{in}, X_{in}, L_p, C_p, L_s, and C_s are shown in Fig. 3-7. The estimated load resistance R_e exhibits low sensitivity to the measured input parameters R_{in} and X_{in}. Furthermore, parameters on the primary and secondary sides have almost the same magnitude of effect on R_e, as illustrated in Fig. 3-7.

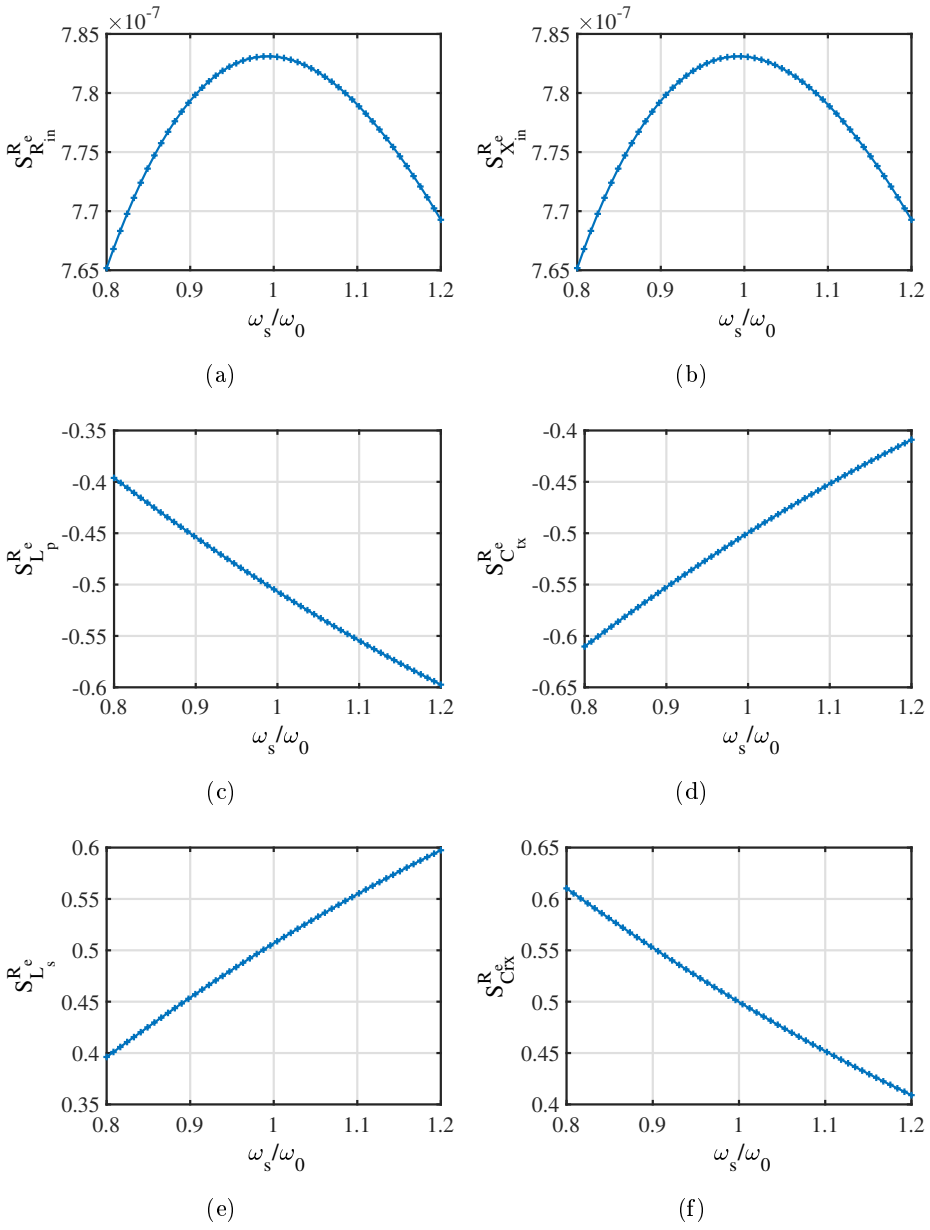


Figure 3-7: Normalized parameter sensitivities of equivalent load resistance respective to (a) R_{in} (b) X_{in} (c) L_p (d) C_p (e) L_s (f) C_s.

Moreover, the inductor and capacitor values have opposite effects on the sensitivity of R_e.

Normalized parameter sensitivities of the estimated mutual capacitance, C_m with respect to R_e, R_{in}, L_s, and C_s are also presented in Fig. 3-8. The estimated mutual capacitance C_m is more sensitive to the measured input resistance R_{in} than to the estimated load resistance R_e; its sensitivity to R_e is comparatively low. Additionally, C_m is less sensitive to the system parameters L_s and C_s compared to its sensitivity to the input parameters R_{in} and R_e.

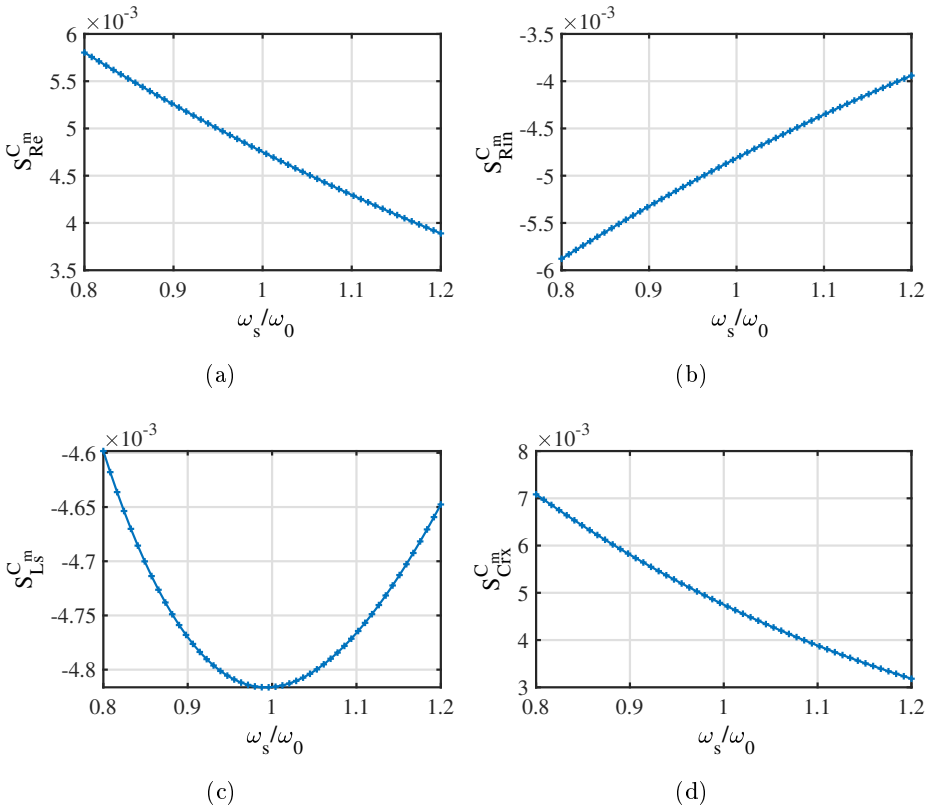


Figure 3-8: Normalized parameter sensitivities of mutual capacitive respective to (a) R_e (b) R_{in} (c) L_s (d) C_s.

3.5 Proposed Primary Side Method of Control Algorithm for CPT System

To control the output voltage V_o or current I_o, a fundamental approximation can be applied to analyze the circuit. The primary-side voltage can be expressed as:

$$V_p = \frac{4V_i}{\pi} \sin\left(\frac{D\pi}{2}\right) \sin\left(\omega_s t\right) \tag{3.27}$$

where D and ω_s are the duty cycle and angular switching frequency of the full-bridge inverter, respectively as shown in Fig. 3-20. A phase-locked loop (PLL) is used to set the operating frequency based on the phase difference between the primary voltage V_p and the primary current I_p. Assuming the primary current is a sine wave, a carrier modulation signal must be generated so that the fundamental component of the primary voltage has the same frequency as, and is in phase with, the primary current. In this work, the second-order generalized integrator frequency-locked loop (SOGI-FLL) algorithm [97] is used to achieve

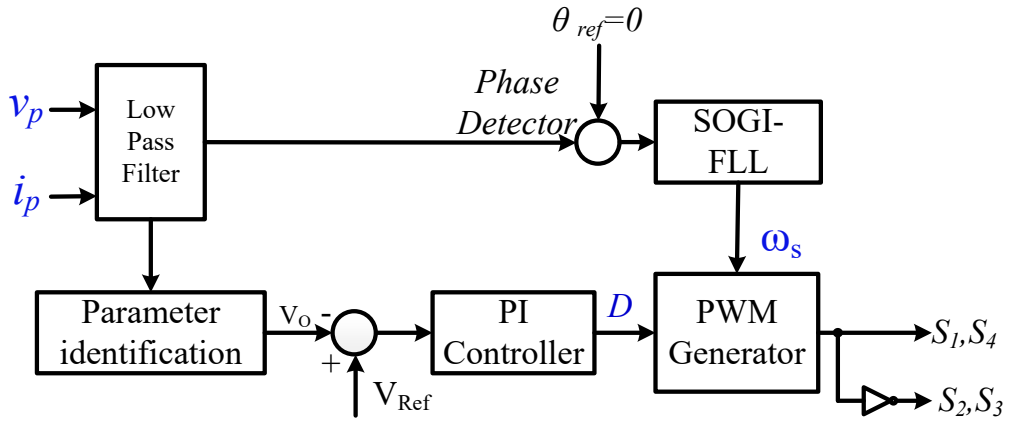


Figure 3-9: Control scheme for both resonant frequency tracking and duty cycle control.

this frequency tracking, as illustrated in Fig. 3-9.

3.5.1 Modeling and Design of Control Loop

Duty Control Using Estimation Value

Small signal model of the SS compensated CPT system is shown in Fig 3-10. The corresponding input-to-output transfer functions G_{vi} of the system are given by [98]

$$G_{vi} = \frac{\hat{v}_o(s)}{\hat{v}_{pc}(s)} = \frac{G_{dc}}{1 + (R_o C_f + \frac{8}{\pi^2} R_o C_{eq})s + L_{eq} C_{eq} s^2 + L_{eq} C_{eq} R_o C_f s^3} \tag{13}$$

where

$$G_{dc} = 4R_o C_2/(\pi^2 \omega_s C_{pm} L_p). \tag{14}$$
$$L_{eq} = 2L_s$$
$$C_{eq} = \frac{2C_2^2}{\omega_s^2 C_{pm}^2 L_s}$$

As established in [99], this dual modulation generates two orthogonal small-signal voltage components for the phase-shift inverter, which is given by

$$\hat{v}_{ps} = \left[2V_i \cos\left(\frac{\pi D}{2}\right)\right] \hat{d} \tag{3.28}$$
$$\hat{v}_{pc} = \left[-2V_i \sin\left(\frac{\pi D}{2}\right)\right] \hat{d}. \tag{3.29}$$

The small-signal model of the SS CPT system decomposes into independent sine and cosine paths [98]. Crucially, since the rectifier and load are coupled exclusively to the cosine path,

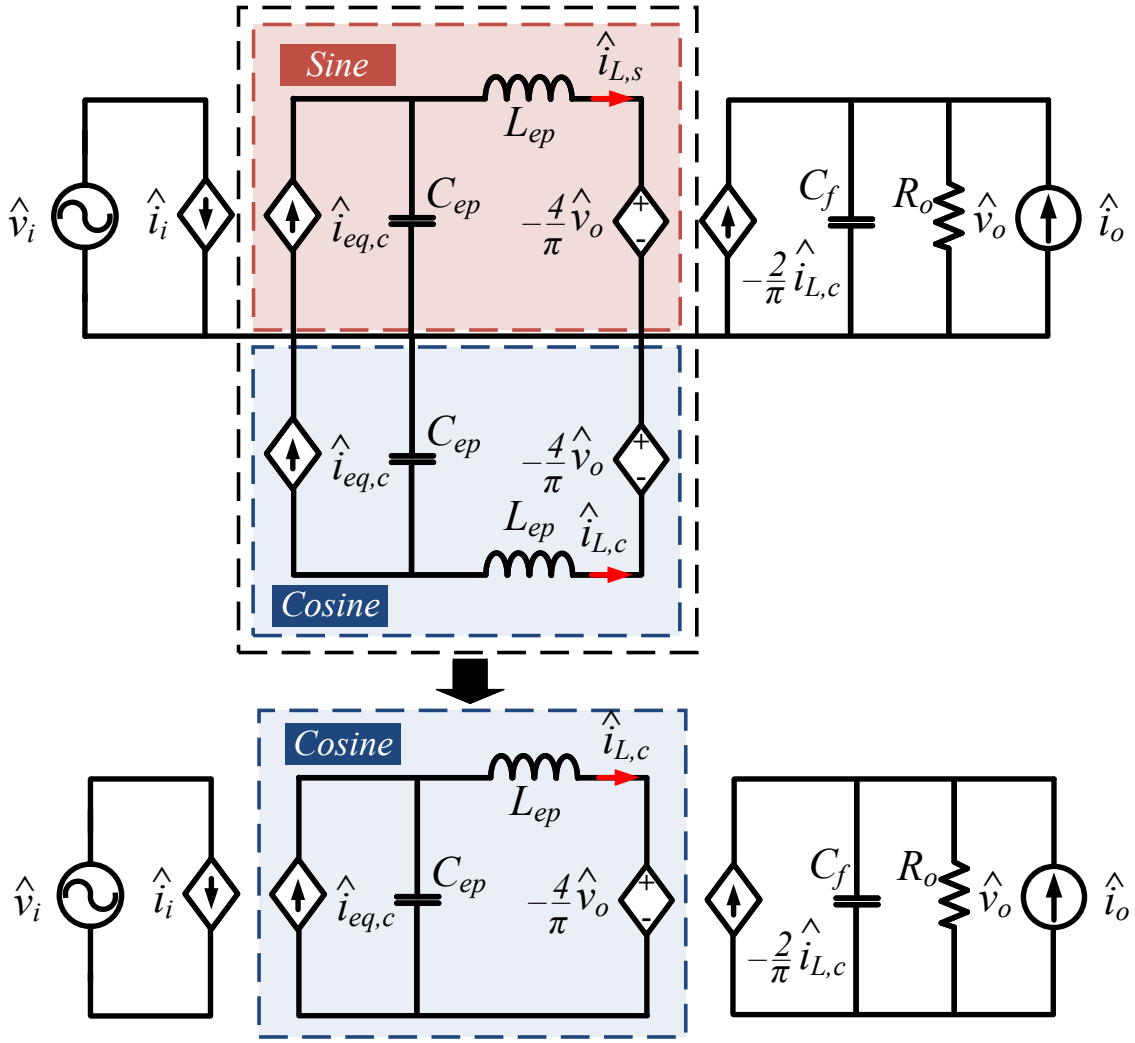


Figure 3-10: Small signal model of SS compensation CPT system [98].

the output voltage $\hat{v}_o$ is only a function of the cosine input, $\hat{v}_{pc}$. The sine path voltage, $\hat{v}_{ps}$, is therefore irrelevant to the output and can be ignored when deriving $G_{vd}(s)$. This duty-to-output transfer function is found by cascading the gains along the cosine path from the input perturbation $\hat{d}$ to the output voltage $\hat{v}_o$

$$G_{vd}(s) = \frac{\hat{v}_o(s)}{\hat{d}(s)} = \underbrace{\left(\frac{\hat{v}_{pc}(s)}{\hat{d}(s)}\right)}_{\text{Stage 1: Inverter Gain}} \cdot \underbrace{\left(\frac{\hat{v}_o(s)}{\hat{v}_{pc}(s)}\right)}_{\text{Stage 2: input-to-output}} \tag{3.30}$$

Substituting the expressions for each stage yields the following transfer function

$$G_{vd}(s) = \left[-2V_i \sin\left(\frac{\pi D}{2}\right)\right] \cdot \frac{G_{dc}}{1 + (R_o C_f + \frac{8}{\pi^2} R_o C_{eq})s + L_{eq} C_{eq} s^2 + L_{eq} C_{eq} R_o C_f s^3} \tag{3.31}$$

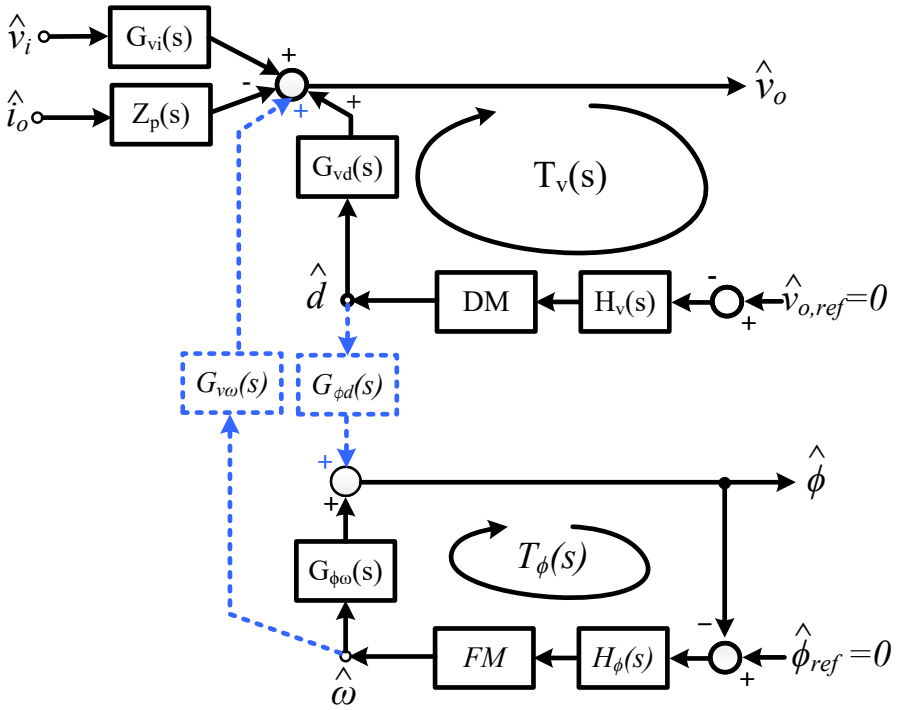


Figure 3-11: Small-signal control loop analysis.

Grouping all the constant gain terms in the numerator yields the final transfer function:

$$G_{vd}(s) = \frac{G_{dc,d}}{1 + (R_o C_f + \frac{8}{\pi^2} R_o C_{eq})s + L_{eq} C_{eq} s^2 + L_{eq} C_{eq} R_o C_f s^3} \tag{3.32}$$

where the DC gain, $G_{dc,d}$, is:

$$G_{dc,d} = -\sin\left(\frac{\pi D}{2}\right)\left[\frac{8 V_i R_o C_2}{\pi^2 \omega_s C_{pm} L_p}\right] \tag{3.33}$$

While accurate, the complexity of this third-order model can obscure insights into the system's dominant behavior. For design and analysis, it is beneficial to simplify the model under practical limiting conditions.

A common condition in such circuits is when the output filter capacitance C_f is significantly larger than the equivalent series capacitance C_{eq}. This assumption is formally stated as:

$$C_f \gg C_{eq} \tag{3.34}$$

Under this condition, we can simplify the coefficients of the denominator polynomial, which

we denote as $D(s)$. Let us examine the coefficient of the first-order term, s^1, from (3.32):

$$\text{Coefficient of } s^1 = R_o C_f + \frac{8}{\pi^2} R_o C_{eq} \tag{3.35}$$

Given the condition in (3.34), the term $R_o C_f$ dominates the sum. Therefore, we can make the following well-justified approximation:

$$R_o C_f + \frac{8}{\pi^2} R_o C_{eq} \approx R_o C_f \tag{3.36}$$

Substituting this approximation back into the denominator of (3.32) yields the simplified polynomial:

$$D(s) \approx 1 + R_o C_f s + L_{eq} C_{eq} s^2 + L_{eq} C_{eq} R_o C_f s^3 \tag{3.37}$$

This simplified third-order polynomial has a structure that allows for convenient factorization by grouping terms:

$$\begin{aligned} D(s) &\approx 1 + R_o C_f s + L_{eq} C_{eq} s^2 + L_{eq} C_{eq} R_o C_f s^3 \\ &\approx (1 + L_{eq} C_{eq} s^2) + (R_o C_f s + L_{eq} C_{eq} R_o C_f s^3) \\ &\approx (1 + L_{eq} C_{eq} s^2) + R_o C_f s (1 + L_{eq} C_{eq} s^2) \\ &\approx (1 + R_o C_f s)(1 + L_{eq} C_{eq} s^2) \end{aligned} \tag{3.38}$$

Finally, by substituting the factored denominator (3.38) back into the original transfer function (3.32), we obtain the simplified model:

$$G_{vd}(s) \approx \frac{G_{dc,d}}{(1 + R_o C_f s)(1 + L_{eq} C_{eq} s^2)} \tag{3.39}$$

The mathematical factorization in (3.38) provides significant physical insight into the system's behavior under the condition $C_f \gg C_{eq}$. The simplification reveals that the complex, interacting third-order system effectively decouples into two simpler, non-interacting subsystems whose dynamics can be analyzed separately:

- A Dominant, First-Order Low-Pass Filter: The term $(R_o C_f s + 1)$ represents a first-order system with a single pole located at a low frequency, $\omega_p = 1/(R_o C_f)$. Because C_f is assumed to be large, this pole is at a very low frequency, making it the dominant pole of the entire system. It dictates the overall response time and provides damping.

- A Second-Order Resonant System: The term $(L_{eq}C_{eq}s^2 + 1)$ represents a double pole. This double pole introduces a pair of complex-conjugate poles on the imaginary axis, corresponding to a high-frequency, undamped resonance at $\omega_r = 1/\sqrt{L_{eq}C_{eq}}$.

In summary, the simplified model (3.39) shows that the system behaves like a fast resonant circuit whose dynamics are then filtered and dominated by a much slower RC low-pass filter. This decoupling is invaluable for controller design, as it allows the designer to address the low-frequency and high-frequency dynamics separately.

To regulate the output voltage, a Proportional-Integral (PI) controller is implemented. The transfer function of a standard PI controller, $G_c(s)$, is given by

$$H_v(s) = K_p + \frac{K_i}{s} = K_p\frac{s + K_i/K_p}{s} = K_p\frac{s + \omega_z}{s} \tag{3.40}$$

where K_p is the proportional gain, K_i is the integral gain, and $\omega_z = K_i/K_p$ is the frequency of the controller's zero. The integral term ensures zero steady-state error, while the zero provides a phase lead to improve stability.

The output impedance, $Z_p(s)$, defines the dynamic relationship between a perturbation in the output load current, $\hat{i}_o(s)$, and the resulting perturbation in the output voltage, $\hat{v}_o(s)$. This is a critical transfer function for assessing load regulation performance and designing the voltage feedback loop. The transfer function of $Z_p(s)$ is given by

$$Z_p(s) = \left.\frac{\hat{v}_o(s)}{\hat{i}_o(s)}\right|_{\hat{v}_i=0} \tag{3.41}$$

The derivation proceeds by setting all independent sources to zero and analyzing the circuit's response to the injected test current $\hat{i}_o$. With the independent input source $\hat{v}_i$ set to zero, we first establish the governing equations for the circuit. Applying KCL at the output node, the sum of currents leaving the node is zero. The current from the test source $\hat{i}_o$ and the dependent current source $-\frac{2}{\pi}\hat{i}_{L,c}$ are treated as entering the node.

$$\frac{\hat{v}_o(s)}{R_o} + sC_f\hat{v}_o(s) - \left(-\frac{2}{\pi}\hat{i}_{L,c}(s)\right) - \hat{i}_o(s) = 0 \tag{3.42}$$

Rearranging to solve for the test current $\hat{i}_o(s)$ gives our primary equation

$$\hat{i}_o(s) = \hat{v}_o(s)\left(\frac{1}{R_o} + sC_f\right) + \frac{2}{\pi}\hat{i}_{L,c}(s) \tag{3.43}$$

This equation shows that the output voltage $\hat{v}_o$ depends on the controlling variable $\hat{i}_{L,c}$. To find an expression for the controlling variable $\hat{i}_{L,c}$, we analyze the "Cosine" block. Since $\hat{v}_i = 0$, the input to this block is short-circuited. Applying Kirchhoff's Voltage Law (KVL) across the series branch containing the inductor L_{ep} and its associated dependent voltage source yields:

$$sL_{ep}\hat{i}_{L,c}(s) - \frac{4}{\pi}\hat{v}_o(s) = 0 \tag{3.44}$$

Solving for $\hat{i}_{L,c}(s)$ provides the necessary relationship with the output voltage

$$\hat{i}_{L,c}(s) = \frac{4\hat{v}_o(s)}{s\pi L_{ep}} \tag{3.45}$$

We now substitute the expression for $\hat{i}_{L,c}(s)$ from (3.45) into our primary KCL equation, (3.43):

$$\hat{i}_o(s) = \hat{v}_o(s)\left(\frac{1}{R_o} + sC_f\right) + \frac{2}{\pi}\left(\frac{4\hat{v}_o(s)}{s\pi L_{ep}}\right) \tag{3.46}$$

Factoring out the common term $\hat{v}_o(s)$:

$$\hat{i}_o(s) = \hat{v}_o(s)\left[\frac{1}{R_o} + sC_f + \frac{8}{s\pi^2 L_{ep}}\right] \tag{3.47}$$

The output admittance of the system, $Y_p(s) = \hat{i}_o(s)/\hat{v}_o(s)$, is therefore

$$Y_p(s) = \frac{1}{R_o} + sC_f + \frac{1}{s\left(\frac{\pi^2}{8}L_{ep}\right)} \tag{3.48}$$

The output impedance $Z_p(s)$ is the reciprocal of this admittance. To express it in the standard form, we first combine the admittance terms over a common denominator

$$Y_p(s) = \frac{R_o + s\left(\frac{\pi^2}{8}L_{ep}\right) + s^2 R_o C_f\left(\frac{\pi^2}{8}L_{ep}\right)}{sR_o\left(\frac{\pi^2}{8}L_{ep}\right)} \tag{3.49}$$

Inverting this expression gives the output impedance $Z_p(s)$

$$Z_p(s) = \frac{sR_o\left(\frac{\pi^2}{8}L_{ep}\right)}{R_o + s\left(\frac{\pi^2}{8}L_{ep}\right) + s^2 R_o C_f\left(\frac{\pi^2}{8}L_{ep}\right)} \tag{3.50}$$

For ease of analysis, the transfer function in (3.50) is normalized to its canonical second-order form. This is achieved by dividing the numerator and denominator by the coefficient

of the s^2 term, which is $R_o C_f L_{refl}$. For clarity, we define a reflected inductance, L_{refl}

$$L_{refl} = \frac{\pi^2}{8} L_{ep} \tag{3.51}$$

The final canonical form of the output impedance is:

$$Z_p(s) = \frac{\frac{s}{C_f}}{s^2 + \frac{s}{R_o C_f} + \frac{1}{L_{refl} C_f}} \tag{3.52}$$

This transfer function exhibits the characteristic of a second-order band-pass filter. The system's dynamic response to a load current step is governed by its undamped natural frequency, ω_n, and its damping factor, ζ

- Natural frequency:

$$\omega_n = \frac{1}{\sqrt{L_{refl} C_f}} \tag{3.53}$$

- Damping factor:

$$\zeta = \frac{1}{2R_o} \sqrt{\frac{L_{refl}}{C_f}} \tag{3.54}$$

The analysis reveals that the output impedance will exhibit a peak at the resonant frequency ω_n, the magnitude of which is determined by the load resistance R_o. A light load condition (large R_o) results in lower damping and a more pronounced impedance peak, indicating a greater sensitivity to load perturbations at that frequency.

The loop gain $T_v(s)$ transfer function of the system, $T_v(s)$, is the product of the controller and the simplified plant model from (3.39), and DM (DM is assumed to be 1, DM=1)

$$T_v(s) = DM \cdot H_v(s) \cdot G_{vd}(s) = \left(K_p \frac{\omega_z + s}{s} \right) \left(\frac{G_{dc,d}}{(1 + R_o C_f s)(1 + L_{eq} C_{eq} s^2)} \right) \tag{3.55}$$

A common and effective design strategy is pole-zero cancellation. The goal is to place the controller's zero, ω_z, to cancel the dominant, low-frequency pole of the plant. From (3.39), the dominant pole is located at $\omega_p = 1/(R_o C_f)$. Therefore, we set:

$$\omega_z = \frac{1}{R_o C_f} \tag{3.56}$$

By applying this cancellation, the term $(s + \omega_z)$ from the controller cancels with the term $(R_o C_f s + 1)$ in the plant denominator (after factoring out the constant $R_o C_f$). The open-loop

transfer function simplifies significantly

$$\begin{aligned} T_v(s) &= \left(K_p \frac{1/(R_o C_f) + s}{s}\right)\left(\frac{G_{dc,d}}{R_o C_f (1/(R_o C_f) + s)(1 + L_{eq} C_{eq} s^2)}\right) \\ &= \frac{K_p G_{dc,d}}{s R_o C_f (1 + L_{eq} C_{eq} s^2)} \end{aligned} \tag{3.57}$$

The controller gains are now determined by setting the desired crossover frequency, ω_c, which defines the control loop's bandwidth. A robust design choice is to set ω_c well below the plant's resonant frequency, $\omega_r = 1/\sqrt{L_{eq} C_{eq}}$, to avoid exciting the resonance. For example, $\omega_c \leq \omega_r/5$.

At the crossover frequency, the magnitude of the open-loop gain must be unity: $|G_{ol}(j\omega_c)| = 1$. Assuming $\omega_c \ll \omega_r$, the resonant term $(L_{eq} C_{eq} (j\omega_c)^2 + 1) \approx 1$. Applying this to (3.57):

$$|T_v(j\omega_c)| \approx \left|\frac{K_p G_{dc,d}}{j\omega_c \cdot R_o C_f \cdot 1}\right| = \frac{K_p G_{dc,d}}{\omega_c R_o C_f} = 1 \tag{3.58}$$

Solving for the proportional gain, K_p, yields:

$$K_p = \frac{\omega_c R_o C_f}{G_{dc,d}} \tag{3.59}$$

The integral gain, K_i, is then found from the definition of the controller zero in (3.56):

$$K_i = K_p \cdot \omega_z = \left(\frac{\omega_c R_o C_f}{G_{dc,d}}\right)\left(\frac{1}{R_o C_f}\right) = \frac{\omega_c}{G_{dc,d}} \tag{3.60}$$

Based on a desired crossover frequency ω_c, the PI controller parameters are:

- Proportional Gain: $K_p = \frac{\omega_c R_o C_f}{G_{dc,d}}$
- Integral Gain: $K_i = \frac{\omega_c}{G_{dc,d}}$

This design methodology results in a phase margin approaching 90°, ensuring a very stable and robust system. The crossover frequency ω_c becomes the primary tuning parameter to balance response speed with stability margins.

Fig. 3-11 shows the overall small-signal block diagram for the controller. The upper part of the diagram illustrates the duty-control loop, where DM represents the PWM gain and $H_v(s)$ is the duty compensator to be designed. The closed-loop audio susceptibility is given by

$$A_{u,CL}(s) = \frac{G_{vi}(s)}{1 + T_v(s)} \tag{3.61}$$

This indicates that variations in the input voltage are effectively rejected. The loop gain is shaped by designing the compensator, $H_v(s)$, as a PI controller. This design approach is based on a low-frequency approximation of the plant's transfer functions, $G_{vi}(s)$ and $G_{vd}(s)$.

To maintain a constant output voltage, the closed-loop transfer function from the load current to the output voltage is considered and given by:

$$Z_o(s) = \frac{Z_p(s)}{1 + T_v(s)} \tag{3.62}$$

Frequency Control Using Frequency Locked Loop

It is advisable to examine the dynamics of the frequency control loop in detail. As a first step, the admittance seen from the primary side, derived from Fig. 3-10, is given by

$$Y(j\omega) = j\omega C_{\text{eq}} + \frac{1}{j\omega L_{\text{eq}} + \frac{8}{\pi^2}\left(\frac{R_o}{1+j\omega R_o C_f}\right)} \tag{3.63}$$

Assuming the output filter capacitor C_f is effective at the switching frequency ω_s, its impedance $(1/(\omega_s C_f))$ is much smaller than the load resistance R_o $(\omega_s R_o C_f \gg 1)$, allowing the input admittance to be simplified as follows:

$$Y(j\omega) = j\left(\omega C_{eq} - \frac{\omega C_{refl}}{\omega^2 L_{eq} C_{refl} - 1}\right) \tag{3.64}$$

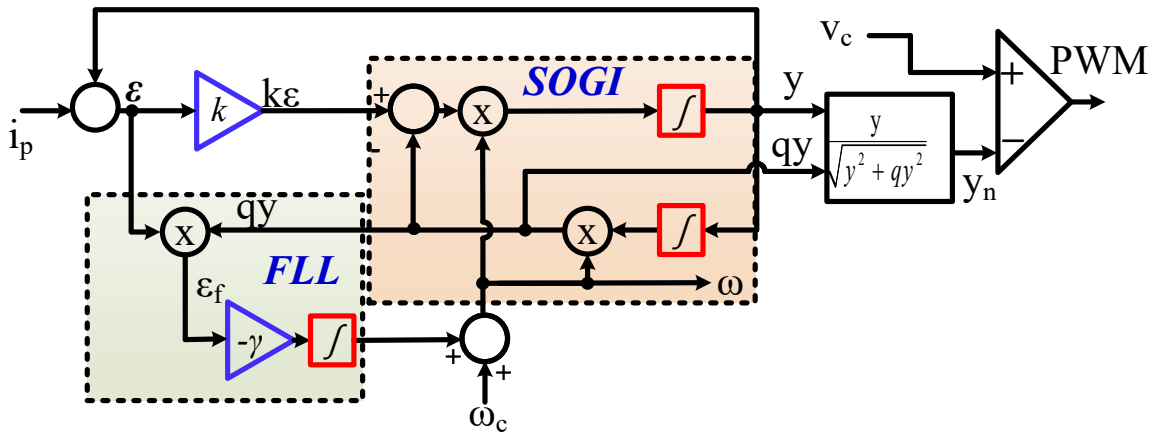


Figure 3-12: Schematic diagram of parameter identification mode of SS-compensated of CPT system with full-bridge inverter and full-wave rectifier.

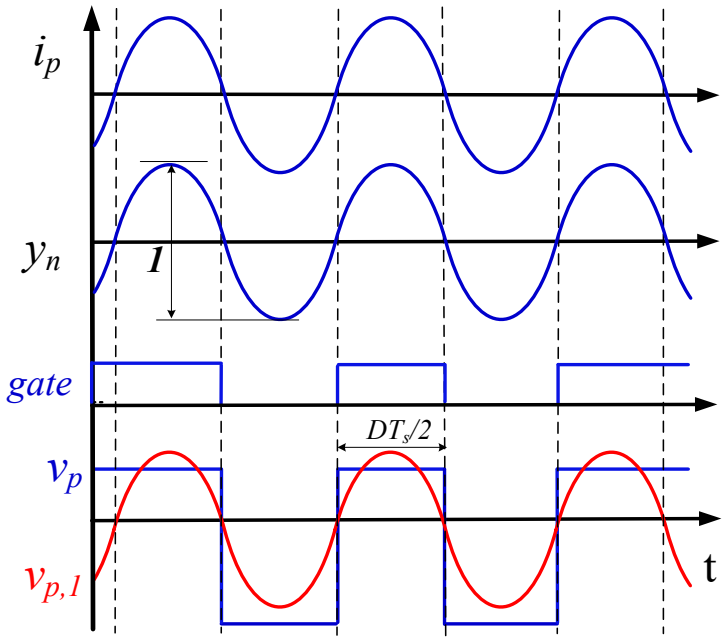


Figure 3-13: Frequency tracking waveform.

where $C_{refl} = \frac{\pi^2}{8} C_f$. The simplified model is purely reactive, as the approximation neglected the resistive component required for power transfer. Although this model is useful for understanding reactive behavior, determining the phase slope requires reintroducing a small damping resistance, R_s. The resulting input admittance is

$$Y(j\omega) = j\omega C_{eq} + \frac{1}{R_s + j(\omega L_{eq} - 1/(\omega C_{refl}))} \tag{3.65}$$

The phase angle of the input admittance, ϕ, represents the phase difference between the primary voltage V_p and the resonant current I_p and it is given by

$$\phi(\omega) = tan^{-1}\left(\frac{\frac{1}{\omega C_{refl}} - \omega L_{eq}}{R_s}\right) \tag{3.66}$$

The lower part of Fig. 3-11 shows the small-signal block diagram of the frequency control loop, which includes the frequency-to-phase-angle transfer function $G_{\phi\omega}(s)$, given by

$$G_{\phi\omega} = \left.\frac{\hat{\phi}}{\hat{\omega}_s}\right|_{\omega=\omega_s} = \frac{-R_s\left(\frac{1}{\omega_s^2 C_{refl}} + L_{eq}\right)}{R_s^2 + \left(\frac{1}{\omega_s C_{refl}} - \omega_s L_{eq}\right)^2} \tag{3.67}$$

where FM is the gain of the voltage-controlled oscillator and $H_\phi(s)$ is the frequency compensator. A single integrator can give the frequency tracking loop a low-pass filter characteristic. In practice, a phase-locked loop (PLL) sets the operating frequency based on the phase difference between the primary voltage v_p and the resonant inductor current i_p. Assuming the resonant tank current is sinusoidal, a carrier modulation signal must be generated to ensure the fundamental component of the primary voltage is synchronized in frequency and phase with the resonant current. In this work, a second-order generalized integrator frequency-locked loop (SOGI-FLL) algorithm [97, 100] is employed to achieve this frequency tracking, as illustrated in Fig. 3-14.

Fig. 3-13 shows the time-domain operation of the frequency tracking loop. The input to the FLL is the sensed resonant current. From this input, the FLL generates three key outputs: an in-phase signal y, a quadrature signal q_y, and the estimated operating frequency ω. The magnitude of the in-phase signal, y, is then normalized using the following formula:

$$y_n(t) = \frac{y(t)}{\sqrt{y(t)^2 + qy(t)^2}} \tag{3.68}$$

This signal is then fed to the PWM generator as the carrier. A comparator then generates the gate signals by comparing this carrier with the control signal v_c. As a result, the primary voltage and resonant current are brought into phase, which locks the operating frequency to the resonant frequency.

According to [97, 100], the transfer function of the SOGI-FLL exhibits an approximate first-order low-pass response, with a cutoff frequency given by

$$\omega_{comp} = \frac{\gamma}{k\omega} {I_p}^2 \tag{3.69}$$

where I_p is the magnitude of the resonant current. The parameters γ and k represent the user-defined gains for the FLL and SOGI, respectively. The settling time of the FLL can be approximated as

$$t_s = \frac{4.6}{\omega_{comp}} \tag{3.70}$$

Consideration on the Coupling of the Two Control Loops

Although the two control loops are often analyzed separately, they can be coupled. As shown in Fig. 3-11, this coupling occurs through two transfer functions: $G_{v\omega}(s)$ and $G_{\phi d}(s)$. The

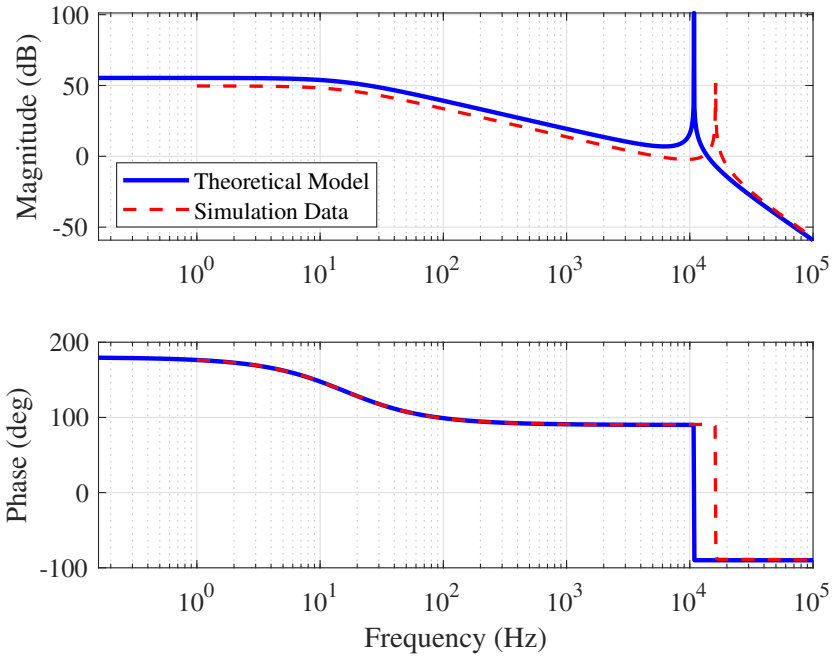


Figure 3-14: Simulation and theoretical comparison of control-to-output transfer function $G_{vd}(s)$.

frequency-to-voltage transfer function, $G_{v\omega}(s)$, is typically non-zero, as a sudden change in frequency affects the instantaneous output voltage. However, the duty-cycle-to-phase transfer function, $G_{\phi d}(s)$, can be eliminated by employing a symmetric PWM technique, such as dual-edge modulation. This technique ensures that changes in the duty cycle do not alter the phase relationship between the resonant current and the primary voltage. Therefore, it is reasonable to treat the two loops as fully decoupled when symmetrical modulation is used, which is the assumption made in this work.

Closed loop Performance

The Bode plots of the output-to-control transfer function $G_{vd}(s)$ of both the theoretical model and simulation data (SIMPLIS simulation) are shown in Fig. 3-14. A slight discrepancy in simulation data is observed compared to the theoretical analysis, primarily due to the assumptions made in the theoretical model for transformation between a capacitor and inductor where $s << \omega_s$ was assumed [101, 102]. From the design guidelines for the PI controller, the controller gains $K_i = 23.2$ and $K_p = 1.16$ are used for output voltage regulation. Moreover, the SOSI-PLL with $k = 0.1$ and $\gamma = 50e^3$ are used for resonant frequency tracking.

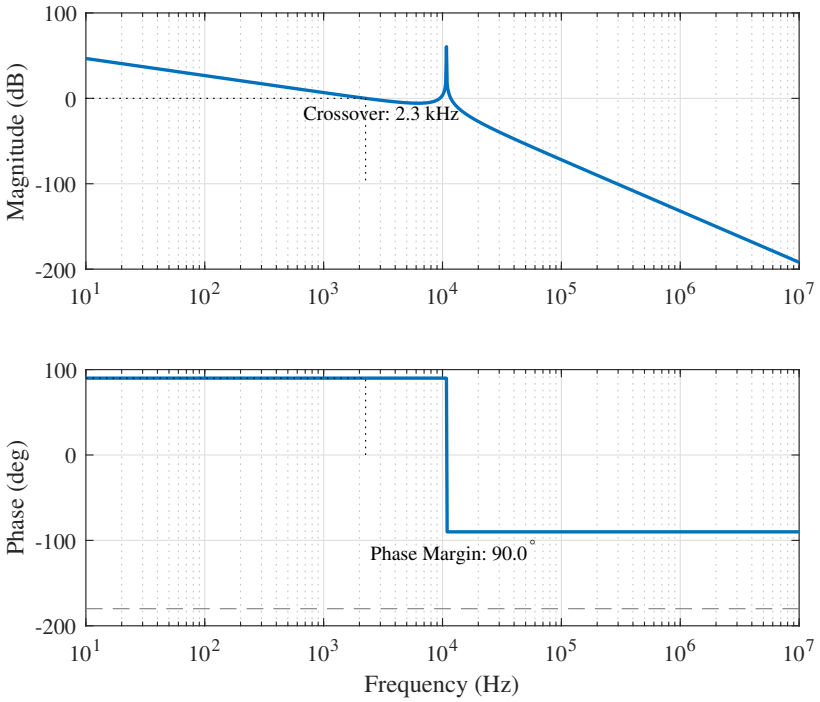


Figure 3-15: Bode plot of the calculated loop gain, $T_v(s)$, for the voltage regulation loop.

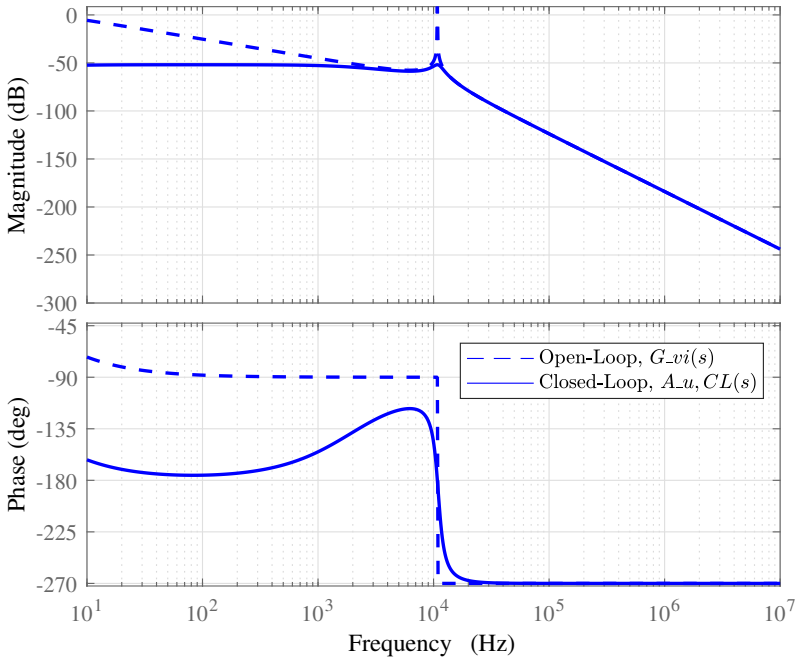


Figure 3-16: Comparison of the open-loop $G_{vi}(s)$ (dashed line) and closed-loop $A_u, CL(s)$ (solid line) audio susceptibility.

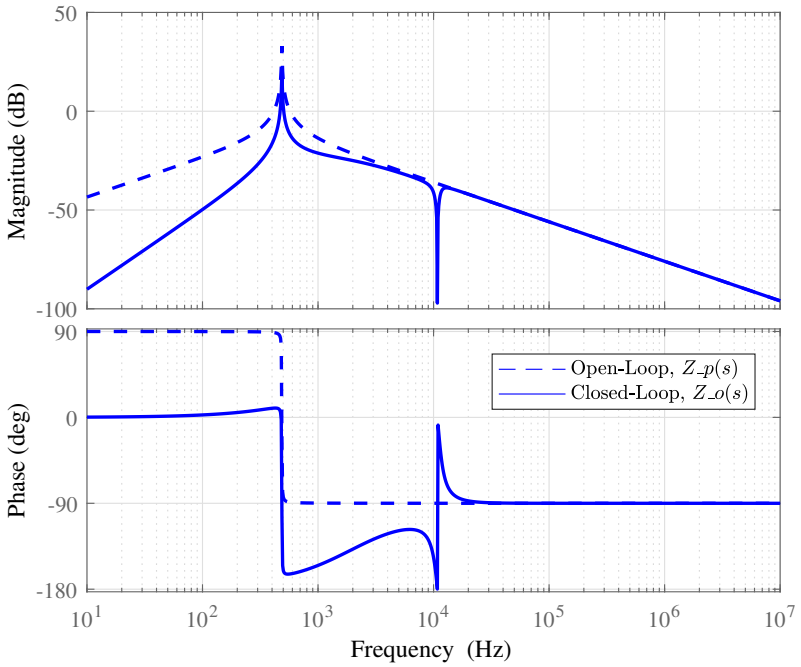


Figure 3-17: Comparison of the open-loop $Z_p(s)$ (dashed line) and closed-loop $Z_o(s)$ (solid line) output impedance.

The system exhibits a crossover frequency of 28.2 kHz and a phase margin of 85.1^o, indicating a highly stable and robust design. The gain margin is infinite, as the phase does not cross -180^o after the gain crossover as shown in Fig 3-15. The feedback loop provides significant rejection of input voltage disturbances within its bandwidth, with an attenuation of over 60 dB at the 120 Hz line ripple frequency as shown in Fig. 3-17. The control loop effectively reduces the output impedance at low frequencies. The peak closed-loop impedance is well-damped, occurring near the crossover frequency, which ensures a stable response to dynamic load changes as shown in Fig. 3-17.

3.6 Simulation Results

Simulation-based case studies are carried out on a direct SS-compensated CPT system using PSIM. The specifications of the system are provided in Table 3.1. The resonant frequency of the system is 200 kHz. R_o=25 Ω is the nominal equivalent load condition. The nominal coupling coefficient of the capacitive coupler is 2.9 %. The system is tested under load step change from 25 Ω to 50 Ω.

The estimated value agrees well with actual value as shown in Fig. 3-18. To reduce the

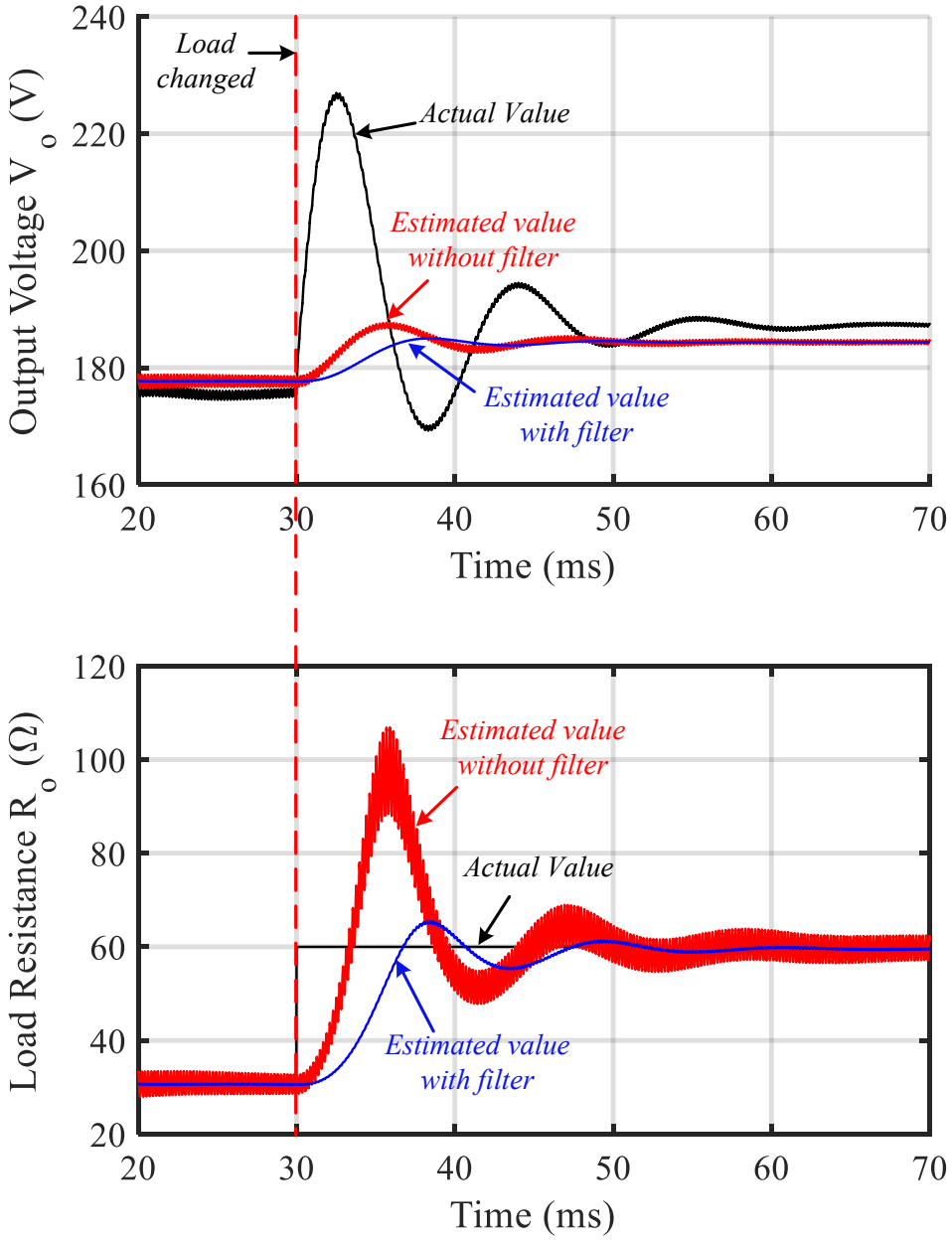


Figure 3-18: Simulation results of the proposed identification method system in a load step change from 30 Ω to 60 Ω with filter and without filter.

overshoot in the estimation of output voltage and load resistance observed after the load change, the estimator dynamics must be carefully tuned, considering the system's transient response characteristics. Moreover, synchronization of voltage and current measurements is essential to avoid temporal misalignment, which can lead to erroneous resistance spikes. Incorporating transient-aware mechanisms, such as gain scheduling or adaptive observers

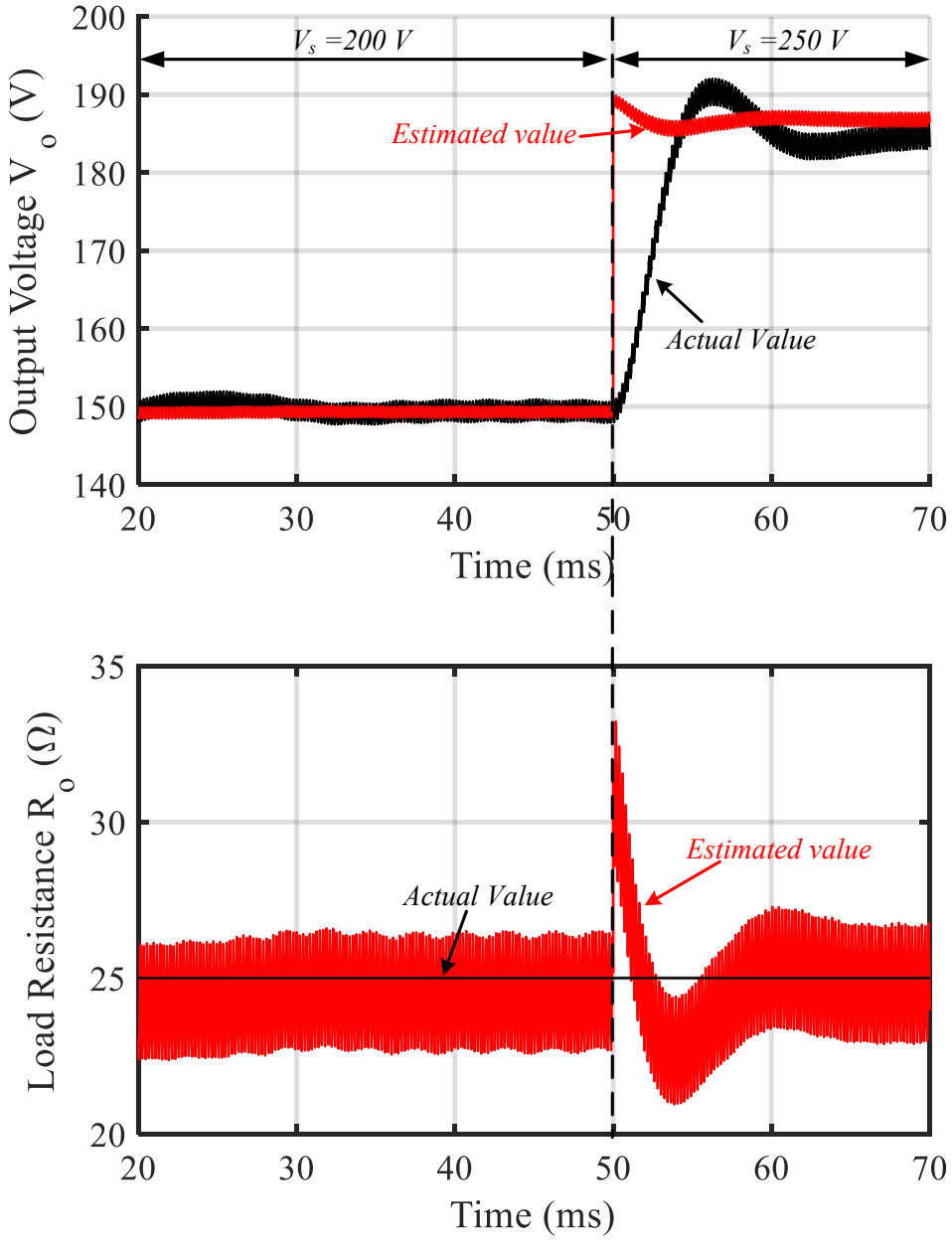


Figure 3-19: Simulation results of the proposed identification method system in input voltage step change from 200 V to 250 V.

that respond to detected load steps, can further improve robustness [104]. If the load change is modeled as an ideal step, using a finite slew-rate or incorporating system parasitic in the simulation can yield more realistic transitions, enabling the estimator to track changes with reduced overshoot [105].

Modeling a system with parasitic elements increases its complexity and requires complex

equations, leading to a higher computational burden. To address this issue, a simple low-pass filter can be applied to remove high-frequency components, thereby reducing the overshoot in the estimated values [106]. Fig. 3-18 presents a comparison of the estimated value with and without the filter. As shown, applying the filter significantly reduces overshoot. However, this comes at the cost of slower dynamic performance in the estimator. Therefore, the filter design must strike a balance between minimizing overshoot and maintaining a fast dynamic response. Table 3.2 summarizes design trade-off of selecting the cutoff frequency of low pass filter f_c for measurement filter of resonant tank current I_p. The proposed identification method was also tested under a varying input voltage. When V_s was changed from 200 V to 250 V, the estimated output voltage matched the actual value well, as shown in Fig. 3-19.

The identified parameters can be used in a closed-loop control system to regulate the output voltage. The simulation results for this closed-loop system are shown in Figs. 3-21 and 3-22, where the output voltage reference is set to 150 V. To test the system's dynamic response, the input voltage was changed from 200 V to 300 V. The identification algorithm detected this change and updated the controller, which in turn reduced the full-bridge inverter's duty cycle from 0.28 to 0.18. As a result, the output voltage was well regulated, remaining close to the 150 V reference. However, minor inaccuracies in the identified parameters introduced a small steady-state error. As shown in Fig. 3-21, the error between the actual and reference voltage is approximately 4%, which is considered an acceptable level of

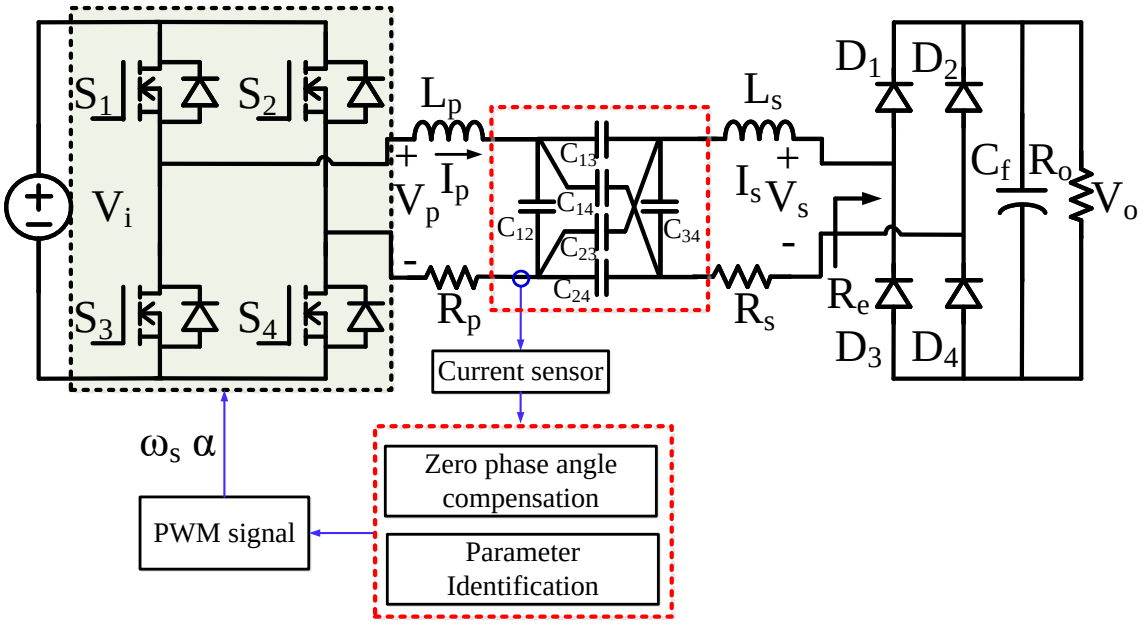


Figure 3-20: Schematic diagram of parameter identification mode of SS-compensated CPT system with a full-bridge inverter and a full-wave rectifier.

performance.

The system was also tested under a load change, where the load current was increased from 6 A to 9 A. As shown in Fig. 3-22, the proposed system regulated the output voltage well.For the misalignment case, the frequency tracking loop should be maintained to follow the resonant frequency, while the voltage regulation loop will mostly reject the disturbance and maintain an almost constant duty cycle as shown in Fig. 3-23.

Table 3.2: Design guidelines for the cutoff frequency f_c of a low-pass measurement filter.

Constraint	**Design Rule**	**Purpose**
Switching Frequency (f_s)	$f_c \leq \frac{f_s}{10}$	Attenuates high-frequency switching noise
Control Bandwidth ($f_{crossover}$)	$f_c \geq (5{-}10) \times f_{crossover}$	Minimizes phase lag to maintain stability.

3.7 Conclusion

In this chapter, a primary-side output current and output voltage control is proposed for CPT system operating at varied frequencies. This self-commissioning control scheme is established based on a new primary-side mutual capacitance and output resistance monitoring scheme by only measuring the transmitter-side voltages and currents. Both the primary-side control and mutual capacitance monitoring are communication-free. The proposed control scheme can minimize the receiver components by eliminating dc regulators or battery management systems since the current or voltage control mode can be selected at the primary side. The proposed control algorithm is simple and intuitive and can be easily implemented using inexpensive digital controllers. Simulation results validate the effectiveness of the proposed control in achieving accurate output regulations and high efficiencies. Experimental verification will be carried out in future work to confirm the analysis of the proposed system.

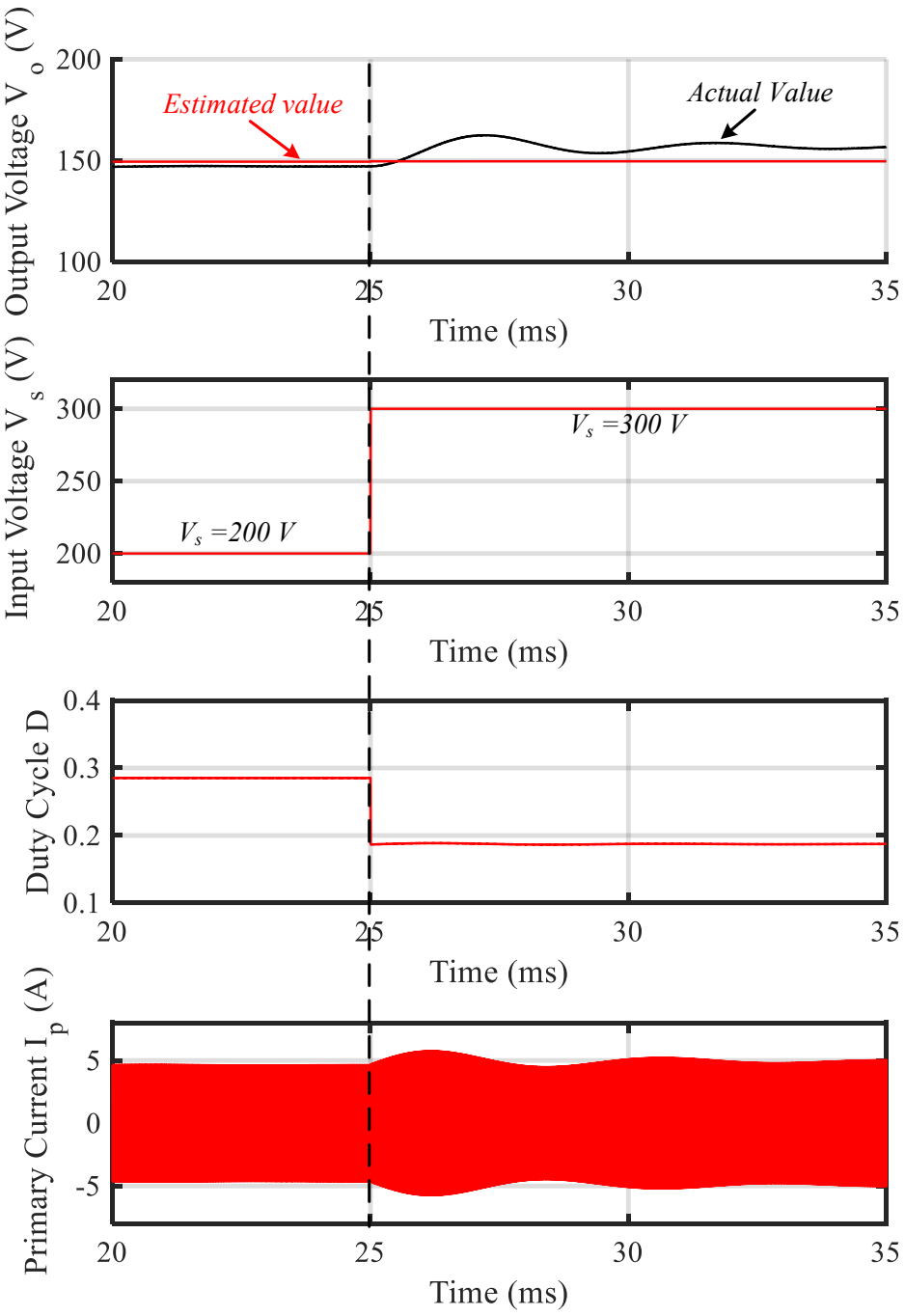


Figure 3-21: Simulation results of closed loop control in input voltage step change from 200 V to 300 V.

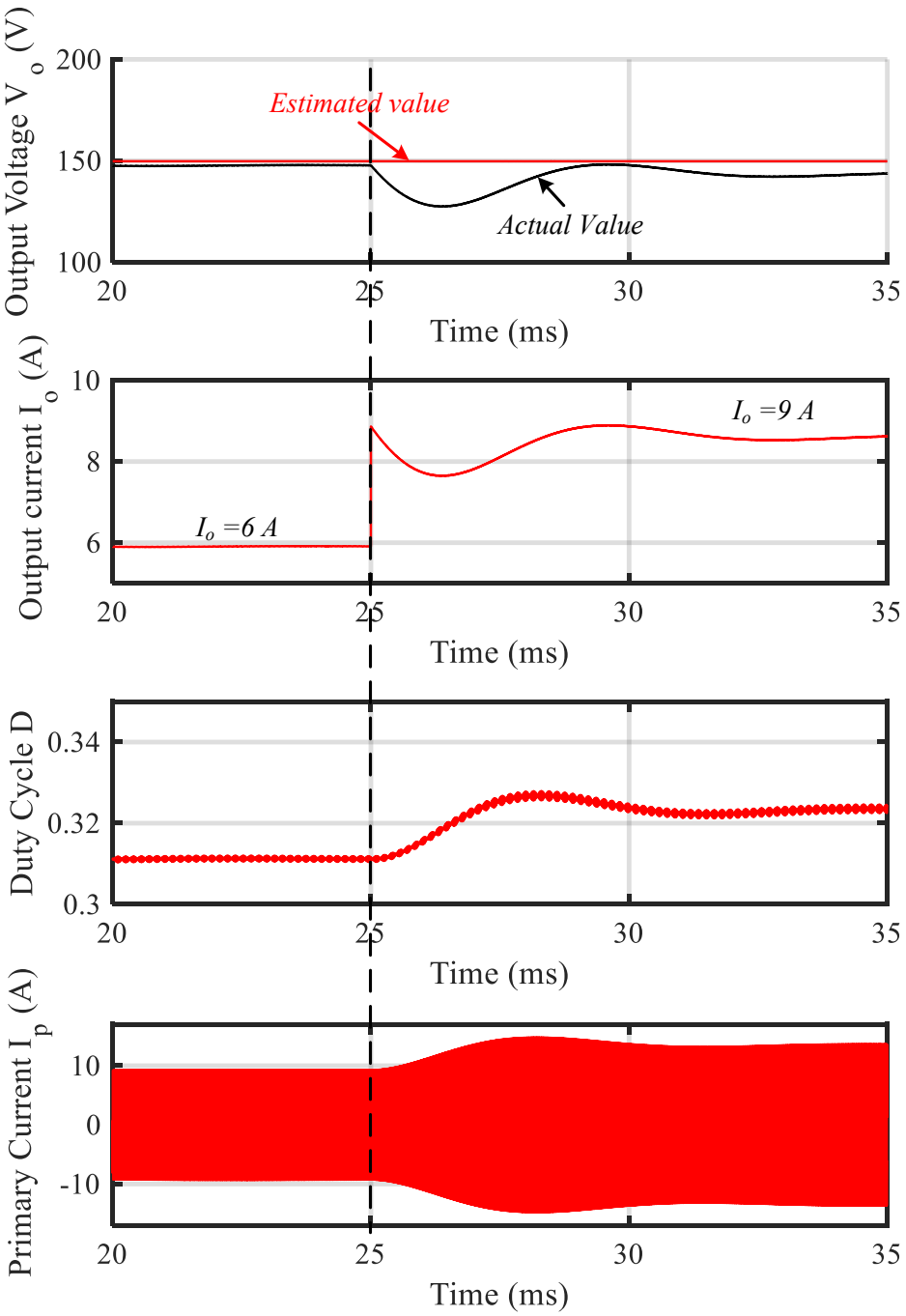


Figure 3-22: Simulation results of closed loop control in load change condition from 6 A to 9 A.

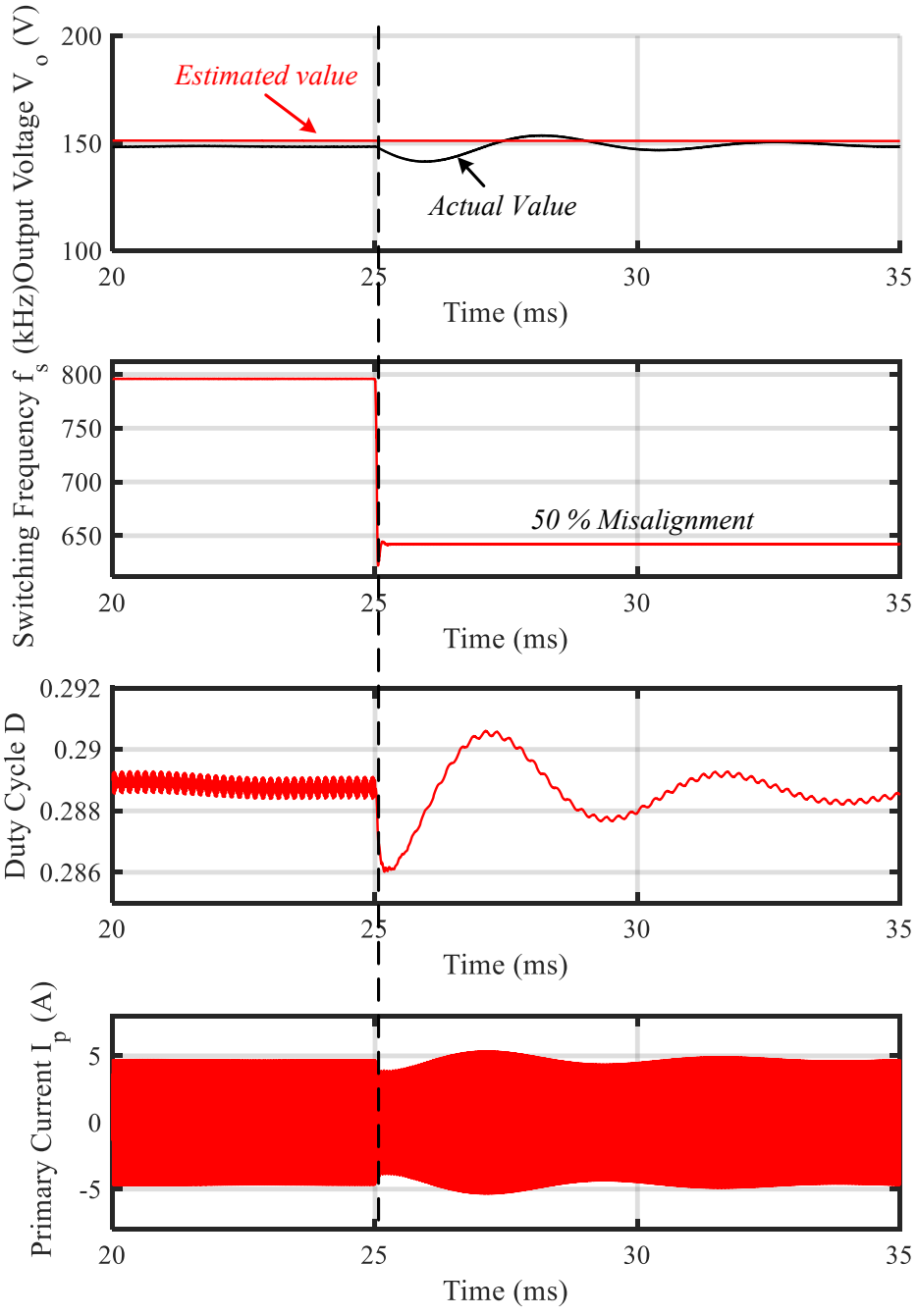


Figure 3-23: Simulation results of closed loop control in 50% misalignment case.

Chapter 4

Voltage Regulation Control Scheme with Wide Input Capability and Extended ZVS Range

This chapter presents a new architecture that makes CPT systems even simpler and easier to control. In the proposed scheme, a wide input voltage range is achieved by duty control while the output voltage is inherently load-independent, and this eliminates the need for an extra DC-DC converter. The system also provides an extended zero-voltage-switching (ZVS) range to deal with both input and load variations. ZVS analysis for each MOSFET switch and an optimal design was presented.

4.1 Introduction

Typical CPT systems for low cost, off-line applications are constructed as shown in Fig. 4-1(a). The power from an AC utility is converted to DC using a diode rectifier and a capacitor smoothing filter. The DC voltage is then converted to a high frequency (HF) AC voltage using a HF inverter. An input matching network (IMN) is required to compensate for the capacitance of the coupler to reduce the volt-ampere rating of the circuit while an output matching network (OMN) is used to boost the current. A rectifier is then used to recover the DC voltage that supplies the load.

Since the HF inverter usually cannot afford to regulate wide control range, the output voltage regulation is achieved using either a front-end or back-end DC-DC converter. Two-

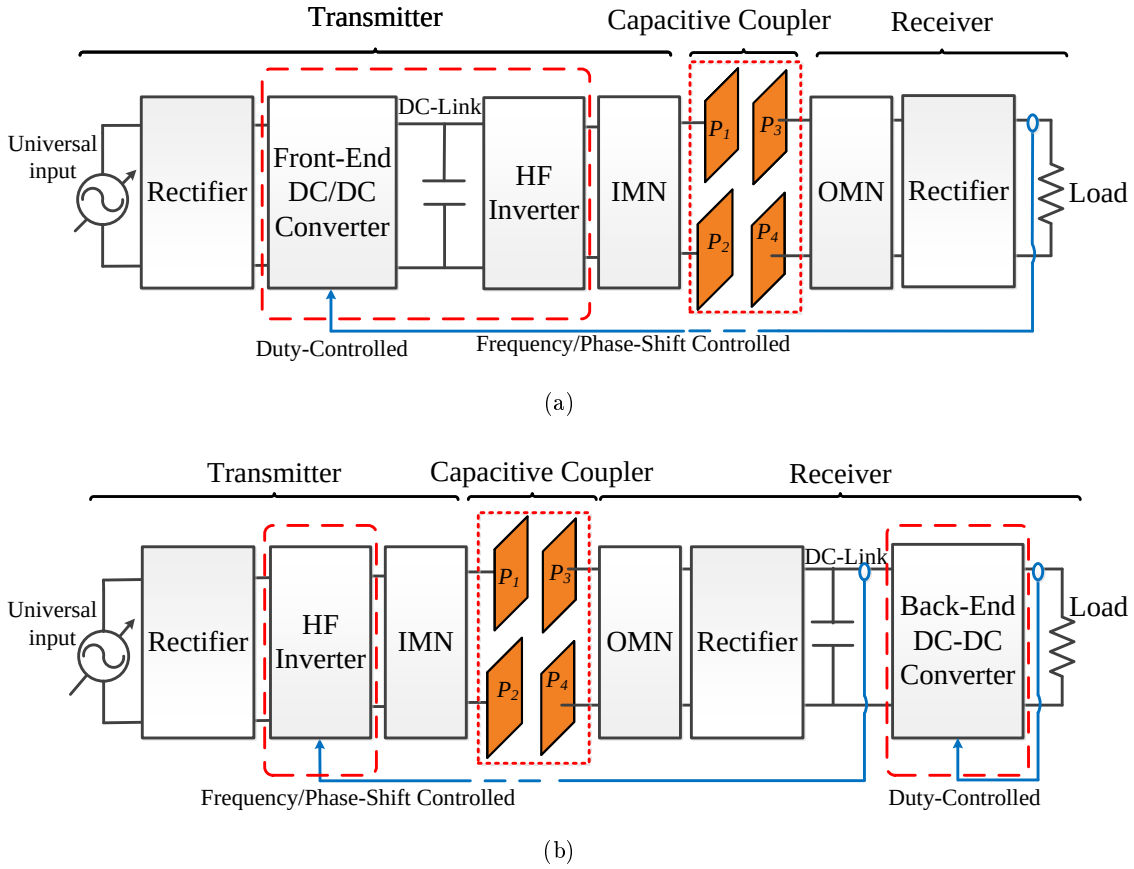
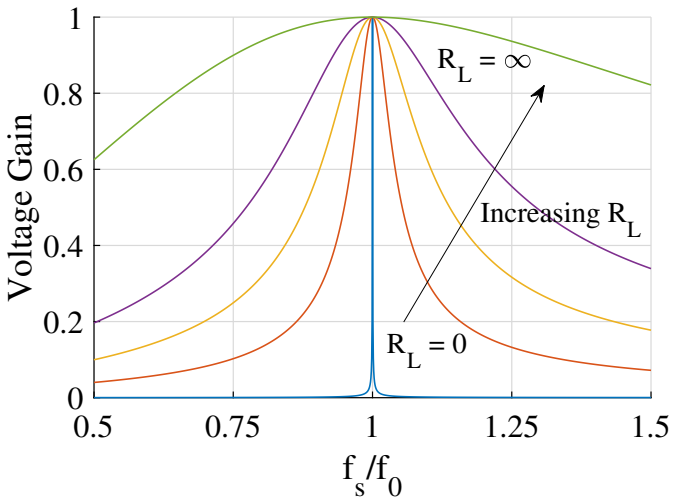


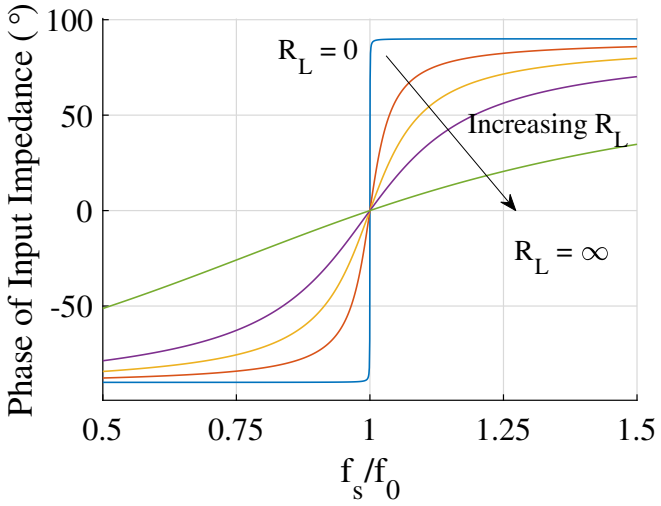
Figure 4-1: Conventional two-stage CPT system architecture using (a) font-end converter (b) back-end converter.

stage architecture is mostly used in CPT systems as shown in Fig. 4-1(b). However, due to two conversion stages, the overall system becomes expensive and complicated. Moreover, the system efficiency is reduced. Therefore, a single-stage structure is a solution for a small size, high efficiency, and more reliable CPT system. However, in this case, the HF inverter has to deal with the wide voltage regulation, which could be a challenge for the existing HF inverter.

Various topologies are available for the HF inverter in CPT systems [107–111], the phase-shift full-bridge configuration is usually regarded as the most suitable topology because it can control both the magnitude and frequency of the primary voltage [112–115]. However, it requires four power switches and gate drivers, which makes the system complex and expensive. On the other hand, to achieve zero-voltage-switching (ZVS), the operating frequency should be adjusted so as to be in the inductive region above the resonant frequency [116]. When ZVS is achieved, the current should lag the voltage. It means that the input impedance should be inductive where the phase angle is positive. Under light load conditions, the ZVS



(a)



(b)

Figure 4-2: Conventional series-compensated CPT system (a) Voltage gain is highly dependent on the load when the system is operated above the resonant frequency (b) ZVS cannot be maintained under light load conditions.

region becomes considerably narrower than normal. Furthermore, the typical gain curve of the CPT system with simple series-series resonant compensation is heavily dependent on the load, which makes load regulation even more difficult when using frequency control to regulate the output voltage, as shown in Fig. 4-2.

In [29–31, 73], special IMNs and OMNs are introduced to improve gain and ZVS characteristics, but these require multiple LC networks that make the system more complex. Their fundamental limitation is that they only step down the voltage and thus cannot cover variations over a wide input voltage range using an inverter alone.

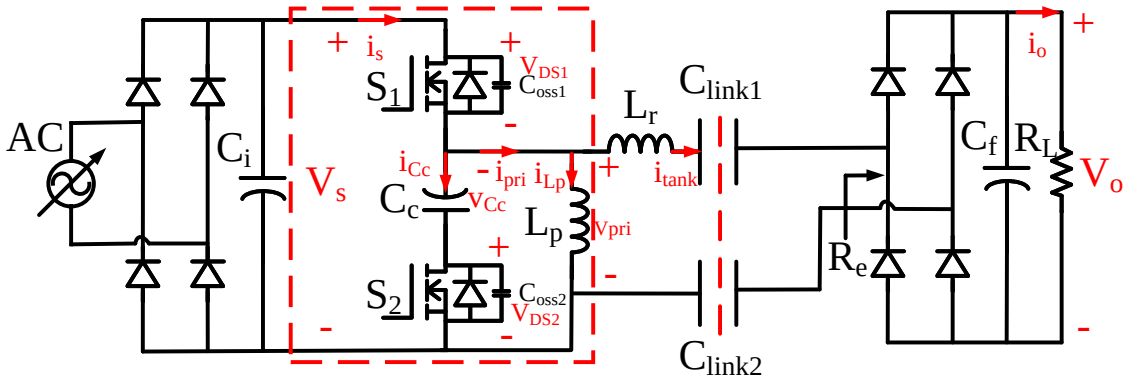


Figure 4-3: Proposed single-stage structure (red box) for low-cost CPT system.

The issue of current research can be listed as follows:

1) The extra DC-DC converter needs to be eliminated to reduce the complexity, volume, and cost of the system.

2) ZVS condition should be achieved for all load conditions for reducing switching losses and EMI.

3) Voltage gain variation should be wide enough to regulate output voltage when the single-stage structure is used.

To overcome these problems, I introduce a single-stage half-bridge structure incorporating a buck-boost for the HF inverter, as shown in Fig. 4-3. The active clamping circuit in [117] was adopted into the proposed single-stage structure. The output voltage of the proposed structure can be regulated with buck and boost mode operations using only duty ratio control, so it can accommodate a wide input or output voltage range. The proposed structure provides a wide ZVS range for both power switches by utilizing a parallel inductance, L_p, and operates exactly at the resonant frequency of system where inherent load regulation is provided. Due to the constant frequency operation the proposed topology is suitable even for a very HF inverter using multi-MHz switching frequencies, where the strict regulation requires the operating frequency being exactly tuned to the Industrial, Scientific, and Medical (ISM) band. In these cases, using duty control instead of frequency control has strong inherent advantages.

4.2 Operational Principles

Fig. 4-3 shows the proposed structure, here two switches, S_1 and S_2, are driven by asymmetrical pulse-width-modulated (APWM) gating pulses. A clamp capacitor, C_c, together

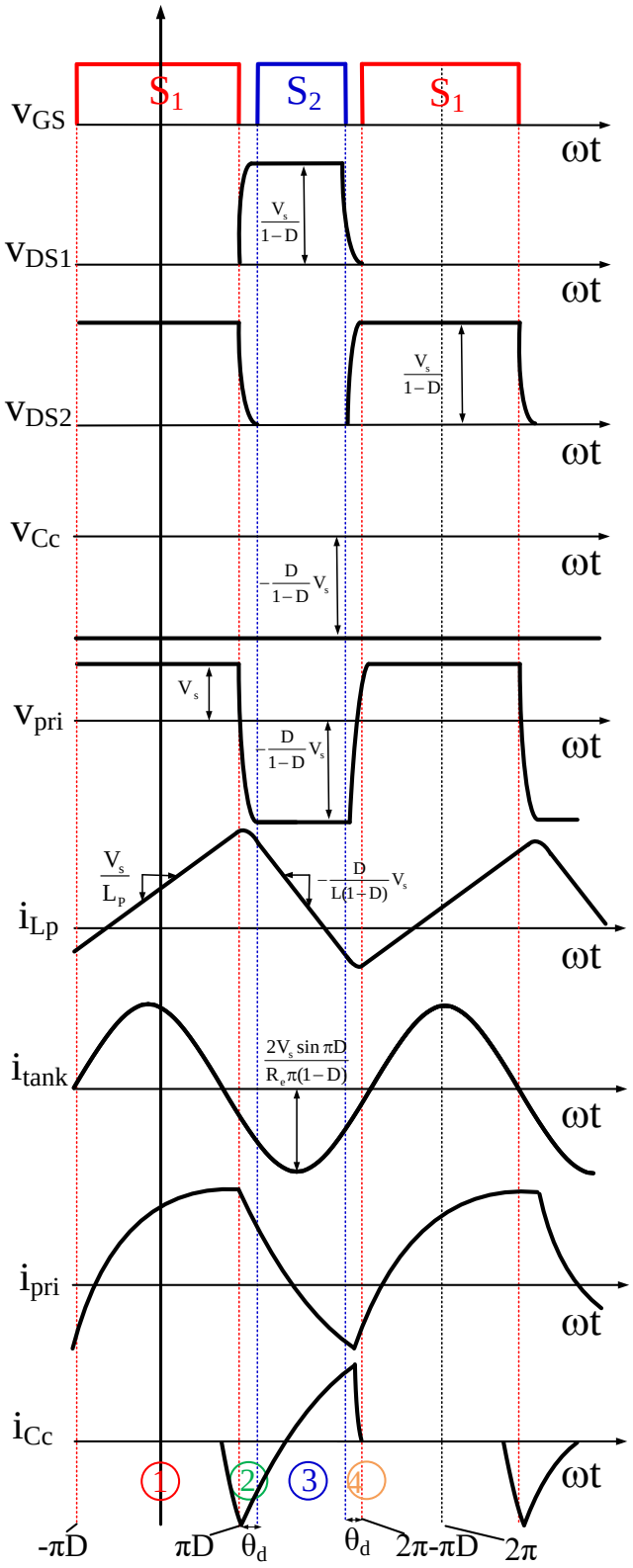


Figure 4-4: Key waveforms of the buck-boost half bridge topology.

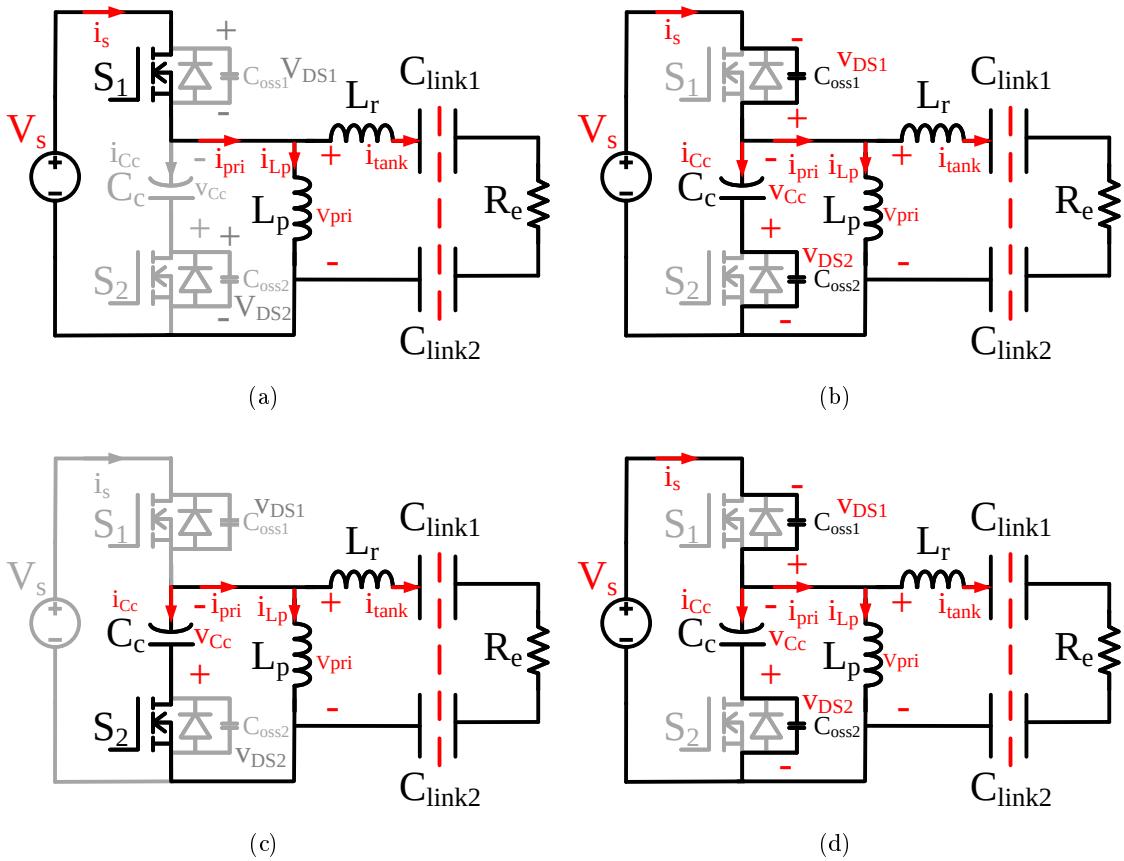


Figure 4-5: Operation stages of the buck-boost half bridge topology.

with a parallel inductor, L_p, form a buck-boost configuration. In the resonant tank, a compensation inductor L_r acting as the IMN is connected to the primary side to compensate for the link capacitances, C_{link1} and C_{link2} as described in [118]. To keep the receiver circuit compact, no OMN is adopted. Before we illustrate the operation of the buck-boost half bridge topology, the following assumptions are made:

1) The clamp capacitor voltage V_{C_c} is considered constant due to a sufficiently large C_c.

2) The two switches, S_1 and S_2, have identical characteristics.

3) All parasitic components except the output capacitances C_{oss1} and C_{oss2}, of the switches are neglected.

4) The quality factor of the resonant tank is high enough to make a sinusoidal current assumption.

5) The output voltage is constant due to a sufficiently large C_f.

6) Only main coupling effect between the electrodes is considered for simplicity.

The gating signal and key operating current and voltage waveforms are synchronously

shown in Fig. 4-4. The operation stages of the buck-boost half bridge topology is shown in Fig. 4-5 with the equivalent AC resistance, $R_e = \frac{8}{\pi^2} R_L$ following the derivation in [119]. The detailed operation can be illustrated as follows:

Stage 1 $[-\pi D < \omega t < \pi D]$: Switch S_1 is turned on while switch S_2 is off. The current in L_p linearly increases as shown by (4.1), the source current is given by (4.2). The drain-to-source voltage of switch S_2 is clamped as shown in (4.3), the primary voltage, v_{pri}, is clamped to the input voltage, V_s.

$$i_{L_p}(\omega t) = \frac{V_s}{L_p}(\omega t - (-\pi D)) + i_{L_p}(-\pi D) \tag{4.1}$$

$$i_s(\omega t) = i_{L_p}(\omega t) + i_{tank}(\omega t) \tag{4.2}$$

$$v_{DS2}(\omega t) = \frac{V_s}{1-D} \tag{4.3}$$

Stage 2 $[\pi D < \omega t < \pi D + \theta_d]$: This stage starts when switch S_1 is turned off while switch S_2 remains off. The energy stored in the inductors, L_p and L_r, simultaneously charges and discharges the parasitic output capacitors of S_2 and S_1, respectively, which makes ZVS of S_2 possible.

Stage 3 $[\pi D + \theta_d < \omega t < 2\pi - \pi D - \theta_d]$: This stage starts when switch S_2 is turned on while switch S_1 is off. At $\omega t = \pi D + \theta_d$, the parasitic output capacitor of S_2 is already fully discharged. Thus, S_2 turns on in a ZVS condition, the drain-to-source voltage of switch S_1 is clamped as shown in (4.4), the currents flowing in L_p, L_r, and C_c are summed to be zero as shown in (4.5).

$$v_{DS1}(\omega t) = \frac{V_s}{1-D} \tag{4.4}$$

$$i_{L_p}(\omega t) + i_{tank}(\omega t) + i_{C_c}(\omega t) = 0 \tag{4.5}$$

Stage 4 $[2\pi - \pi D - \theta_d < \omega t < 2\pi - \pi D]$: This stage starts when the switch S_2 is turned off while S_1 is also off. In this stage, the energy stored in the inductors L_p and L_r are used to charge the parasitic output capacitor S_1 and discharge the output capacitor S_2, thus ZVS of switch S_1 can be achieved.

4.3 Analysis of The Proposed System

In this section, features of the proposed system are investigated.

4.3.1 Voltage Gain Analysis

Based on the basic operation principles outlined in the previous section and applying flux balance for L_p, the average voltage of the clamp capacitor, V_{C_c}, and the peak-to-peak current in the parallel inductor can be derived as follows:

$$V_{C_c} = \frac{D}{1-D} V_s \tag{4.6}$$

and

$$\Delta I_{Lp} = \frac{D}{L_p f_o} V_s, \tag{4.7}$$

where D is the duty cycle. The buck-boost half bridge topology is controlled by a PWM gating signal at the resonant frequency, f_0, where

$$f_0 = \frac{1}{2\pi\sqrt{L_r C_{link}}} \tag{4.8}$$

and

$$C_{link} = \frac{C_{link1} C_{link2}}{C_{link1} + C_{link2}}. \tag{4.9}$$

Under the high-quality factor assumption, the primary voltage waveform, v_{pri}, can be decomposed by Fourier series. It can be seen that the waveform of primary voltage, V_{pri}, is even-function symmetry as shown in Fig. 4-4. Therefore, the Fourier coefficients can be calculated as

$$\begin{aligned} a_v &= \frac{2}{\pi}\left(\int_0^{\pi D} V_s d(\omega t) + \int_{\pi D}^{\pi} -\frac{D}{1-D} V_s d(\omega t)\right) \\ &= 0 \\ a_k &= \frac{2}{\pi}\left(\int_0^{\pi D} V_s d(\omega t) + \int_{\pi D}^{\pi} -\frac{D}{1-D} V_s \cos\omega t d(\omega t)\right) \\ &= \frac{2V_s \sin\pi D}{\pi(1-D)}. \end{aligned} \tag{4.10}$$

Where only the fundamental component needs to be considered. Thus, v_{pri} is well approximated by

$$v_{pri}(\omega t) = \frac{2V_s \sin\pi D}{\pi(1-D)} \cos(\omega t). \tag{4.11}$$

Where system is operated at its resonant frequency, the tank current can be represented

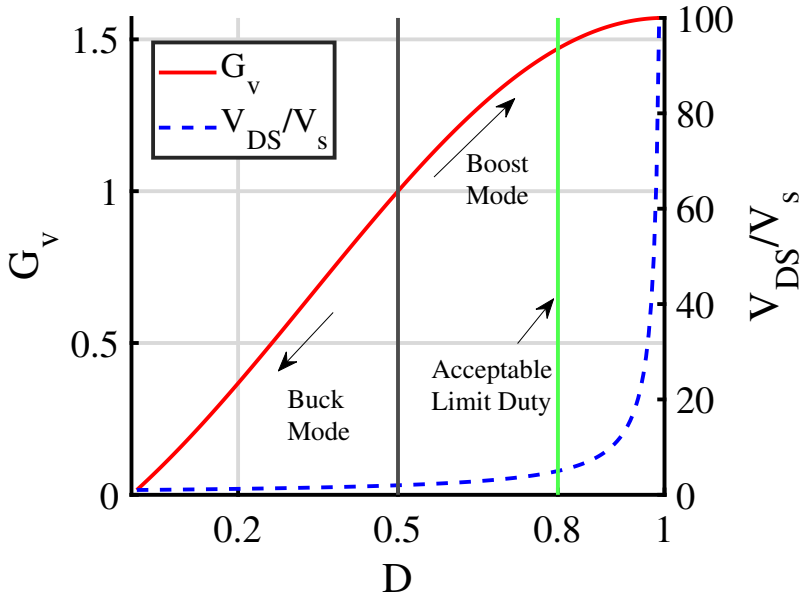


Figure 4-6: The DC voltage gain, G_v, and normalized switch voltage stress, V_{DS}/V_s, of the buck-boost half bridge topology versus the duty cycle, D.

as

$$i_{tank}(\omega t) = \frac{2V_s sin(\pi D)}{R_e \pi (1-D)} cos(\omega t + \phi), \tag{4.12}$$

when ϕ is the phase-shift between the primary voltage and the tank current. Since the buck-boost converter and the half-bridge are merged together, the output voltage can be directly regulated by changing the duty ratio, and the overall DC voltage gain with a full wave rectifier is given by

$$G_v = \frac{V_o}{V_s} = \frac{\sin \pi D}{2(1-D)}. \tag{4.13}$$

Fig. 4-6 shows that the voltage gain and switch voltage stress. It can be seen that the voltage gain with the buck-boost half bridge topology is wider than with conventional half-bridge and full-bridge. Moreover, the maximum voltage gain of the buck-boost half bridge topology is equal to $\frac{\pi}{2}$ that is larger than conventional topology providing a maximum DC voltage gain of 0.5 and 1, respectively. The voltage gain G_v is almost linearly dependent on duty cycle D. The output voltage of the proposed structure can be regulated by any digital pulse-width modulated (PWM) controller, where the input voltage, V_s, is sensed to generate a duty ratio adjusting the primary voltage, v_{pri}. However, since the switch voltage stress increases as the voltage gain increases, the maximum allowable duty cycle should be limited.

4.3.2 ZVS Condition

In order to analyze the ZVS conditions, the parallel inductor current, i_{Lp}, should be identified. This can be expressed as follows:

for $-\pi D < \omega t \leq \pi D$

$$i_{L_p}(\omega t) = V_s \left(\frac{\omega t}{\omega L_p} + K \right) \tag{4.14}$$

and for $\pi D < \omega t \leq 2\pi - \pi D$

$$i_{L_p}(\omega t) = V_s \left(\frac{D(\pi - \omega t)}{(1-D)\omega L_p} + K \right) \tag{4.15}$$

where the definition of K and a detailed derivation are given in Appendix. During the dead times (stages 2 and 4), the output capacitor, C_{oss}, of switches S_1 and S_2 is charged or discharged simultaneously by the primary current, i_{pri}. Since the value of the clamp capacitor, C_c, is much larger than the C_{oss} of the switches, it can be neglected during the ZVS analysis.

Due to asymmetry in the waveform of i_{Lp}, as shown in Fig. 4-4, (4.14), and (4.15), the ZVS conditions for the two switches, S_1 and S_2, need to be considered separately. The total stored charges in the output capacitor of S_1 and S_2 are identical, which can be calculated as

$$Q_{oss1,2} = C_{eq,Q} \frac{V_s}{1-D}, \tag{4.16}$$

where $C_{eq,Q}$ is charge-linear capacitance as defined in [120]. This is dependent on the duty cycle, D, and the input voltage, V_s. To achieve the ZVS condition, the primary current has to fully discharge the output capacitor of the switches during the dead-time angle, θ_d. Therefore, the condition sufficient to achieve ZVS in switches S_1 and S_2 can be expressed as follows:

$$Q_{i_{pri}} \geq Q_s \tag{4.17}$$

where $Q_{i_{pri}}$ is the maximum swept charge by the primary current during the dead time and Q_s is the total stored charge given by $Q_s = Q_{oss1} + Q_{oss2}$. However, $Q_{i_{pri}}$ is different for the two switches and can be calculated respectively as follows:

During stage 4, $Q_{i_{pri}}$ is given by

$$\begin{aligned} Q_{i_{pri}} &= \int_{-\pi D}^{-\pi D+\theta_d} i_{pri}(\omega t)d(\omega t) \\ &= V_s\theta_d\left(\frac{2\sin\pi D}{R_e\pi(1-D)}\cos(\pi D-\frac{\theta_d}{2})+\frac{\theta_d-2\pi D}{2\omega L_p}+K\right) \end{aligned} \tag{4.18}$$

and it is used for the ZVS condition of switch S_1. On the other hand, during stage 2, $Q_{i_{pri}}$ is given by

$$\begin{aligned} Q_{i_{pri}} &= \int_{\pi D+\theta_d}^{\pi D} i_{pri}(\omega t)d(\omega t) \\ &= V_s\theta_d\left(\frac{-2\sin\pi D}{R_e\pi(1-D)}\cos(\pi D+\frac{\theta_d}{2})+\frac{\theta_d}{(1-D)\,2\omega L_p}-K\right) \end{aligned} \tag{4.19}$$

which is utilized for the ZVS condition of switch S_2.

Substituting (4.18), (4.19) into (4.17) and then the condition for achieving ZVS condition for switched S_1 and S_2 with respect to the parallel inductor, L_p, can be given respectively by

$$L_p \le \frac{\theta_d-2\pi D}{2\omega\left(\frac{C_{eq,Q}}{\theta_d(1-D)}-\frac{2\sin\pi D}{R_e\pi(1-D)}\cos(\pi D-\frac{\theta_d}{2})-K\right)} \tag{4.20}$$

$$L_p \le \frac{\theta_d}{(1-D)2\omega\left(\frac{C_{eq,Q}}{\theta_d(1-D)}+\frac{2\sin\pi D}{R_e\pi(1-D)}\cos(\pi D+\frac{\theta_d}{2})+K\right)}. \tag{4.21}$$

4.3.3 Efficiency Consideration

It should be noted that the primary current, i_{pri}, needs to be large enough to achieve the ZVS conditions during the dead time. Since the tank current, i_{tank}, is the same for a given load, i_{Lp} has a dominant effect on the ZVS condition. In order to increase i_{Lp}, achieving the small L_p is helpful. However, a small L_p causes higher copper losses from the parallel inductor, L_p, and increased conduction losses from switches. Therefore, L_p should be designed optimally for achieving the ZVS conditions as well as for minimizing losses. During the L_p design process, system efficiency should be considered in all operating ranges.

System efficiency is given by

$$\eta = \frac{P_o}{P_o + P_{inv,loss} + P_{tank,loss} + P_{rec,loss}}, \tag{4.22}$$

where P_o is the output power of the system; $P_{inv,loss}$ is the power loss from the inverter including the conduction and switching loss of switches and the copper loss of the inductor L_p; $P_{tank,loss}$ is the power loss from the passive element from the resonant tank; $P_{rec,loss}$ is the power loss from the full-wave rectifier.

When the optimal L_p is chosen, the switching losses are greatly reduced and only conduction loss needs to be considered. Therefore, the system efficiency can be expressed as

$$\eta = \frac{R_L}{\left(\frac{I_{rms,L_p}}{V_o}\right)^2 R_{Lp} {R_L}^2 + R_L + R_{tank}} \tag{4.23}$$

where R_{Lp} is the equivalent parasitic resistance of the parallel inductor, L_p; $R_{tank} = R_{Lr} + R_{Clink}$ is sum of the equivalent parasitic resistance of the compensation inductor, L_r and capacitive coupler, C_{link}; I_o is output current in the load resistance and I_{rms,L_p} is the parallel inductor rms currents as given by (11) in Appendix A. Substituting (11) and (4.13) into (4.23), the system efficiency can be rewritten as

$$\eta = \frac{R_L}{\frac{R_{L_p}}{3}\left(\frac{(1-D)D}{\sin(\pi D)L_p f_0}\right)^2 R_L^2 + (1 + R_{L_p})R_L + R_{tank}} \tag{4.24}$$

The optimal load can be calculated by differentiating η with respect to R_L and solving

$$\frac{\partial \eta}{\partial R_L} = 0. \tag{4.25}$$

The optimum load resistance value $R_{L,opt}$ is given by

$$R_{L,opt} = \frac{\sin(\pi D)L_p f_0}{(1-D)\,D}\sqrt{\frac{3R_{tank}}{R_{L_p}}} \tag{4.26}$$

By substituting (4.26) into (4.24), the maximum system efficiency can be given by

$$\eta_{max} = \frac{1}{\frac{2(1-D)D\sqrt{R_{L_P}R_{tank}}}{\sqrt{3}\sin(\pi D)L_p f_0} + 1 + R_{L_p}} \tag{4.27}$$

The maximum system efficiency and optimal load resistance value are achieved maximum

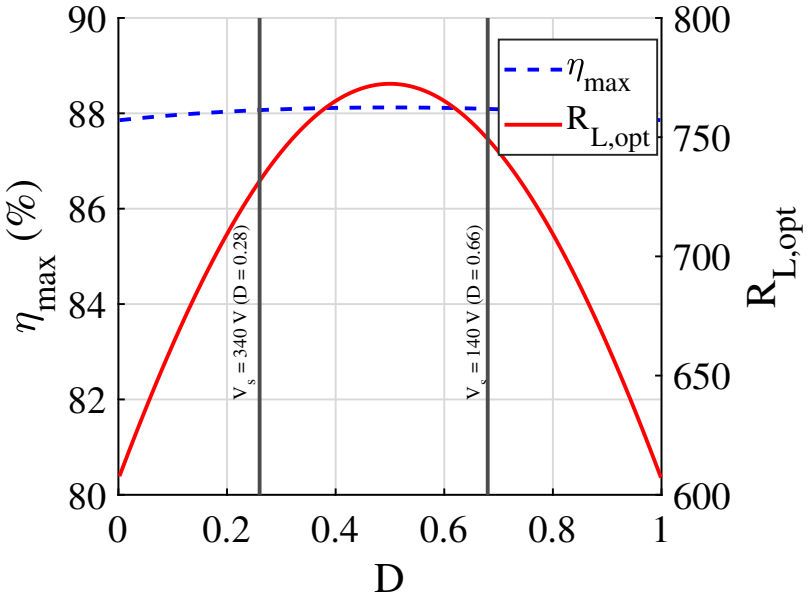


Figure 4-7: Maximum system efficiency, η_{max}, and optimal load resistance, $R_{L,opt}$, versus the duty cycle, D.

value at $D = 0.5$. Moreover, the maximum system efficiency is almost flat according to the change of duty cycle, D, as shown in Fig. 4-7. It means that when the system is properly designed, the maximum system efficiency can be kept almost constant even with the change of duty cycle, D.

4.4 Design Procedure

This subchapter describes the component design procedure for the buck-boost half bridge topology. Firstly, the DC input voltage considering the rectified universal AC voltage range is given by

$$V_{s,\min} \leq V_s \leq V_{s,\max}, \tag{4.28}$$

and the maximum output power is considered as

$$P_o \leq P_{o,\max}. \tag{4.29}$$

For line regulation, the duty cycle range can be obtained by (4.13) and the minimum load resistance is obtained as follows:

$$R_L \geq \frac{{V_o}^2}{P_{o,max}}. \tag{4.30}$$

According to the system specifications, the circuit components can be designed as follows:

The Resonant Components, L_r and C_{link}

The total link capacitance, C_{link}, is measured from the capacitive coupler structure. From the fundamental design equation of CPT given in [32], the resonant angular frequency, ω_o, is chosen as larger than the following value

$$\omega_0 \geq \frac{1}{C_{link} V_{Clink,p}} \sqrt{\frac{2P_o}{\eta_{rec} R_e}} \tag{4.31}$$

where $V_{Clink,p}$ is the peak link capacitor voltage, and η_{rec} is the estimated rectifier efficiency. Then the inductance, L_r, should be chosen as

$$L_r = \frac{1}{{\omega_0}^2 C_{link}}. \tag{4.32}$$

The peak tank inductor current and peak link capacitor voltage are both approximately proportional to the maximum load current, $I_{o,max}$. So, the peak tank inductor current is expressed as

$$I_{tank,p} = \frac{\pi}{2} I_{o,\max} = \frac{\pi}{2} \frac{P_{o\max}}{V_o}, \tag{4.33}$$

and the peak link capacitor voltage is related to the peak tank inductor current by the tank impedance as

$$V_{Clink,p} = I_{tank,p} \sqrt{\frac{L_r}{C_{link}}} = \frac{\pi}{2} \frac{P_{o\max}}{V_o} \sqrt{\frac{L_r}{C_{link}}}. \tag{4.34}$$

The Shunt Inductor, L_p

L_p is designed according to the ZVS conditions and efficiency consideration. The maximum current rating of the inductor can be calculated as

$$I_{Lp,p} = V_s \left(\frac{\pi D}{\omega L_p} + K \right) \tag{4.35}$$

The Clamp Capacitor, C_c

The value of the clamp capacitor can be chosen approximately as larger than the minimum value given by

$$C_c \geq C_{c,\min} = \frac{D(1-D)V_s}{L_p f_0^2 \Delta V_C} \tag{4.36}$$

where ΔV_C is the target ripple voltage in the clamp capacitor C_c.

Switches, S_1 and S_2

The voltage rating for the switches S_1 and S_2 can be calculated as

$$V_{DS,p} = \frac{V_s}{1-D}. \tag{4.37}$$

The Rectifier Diode

The voltage rating of the diode in the rectifier is given by

$$V_{D,p} = V_o, \tag{4.38}$$

and the average current rating of the diode can be expressed as

$$I_{D,avg} = \frac{1}{2} I_{o,max}. \tag{4.39}$$

4.5 Performance Verification

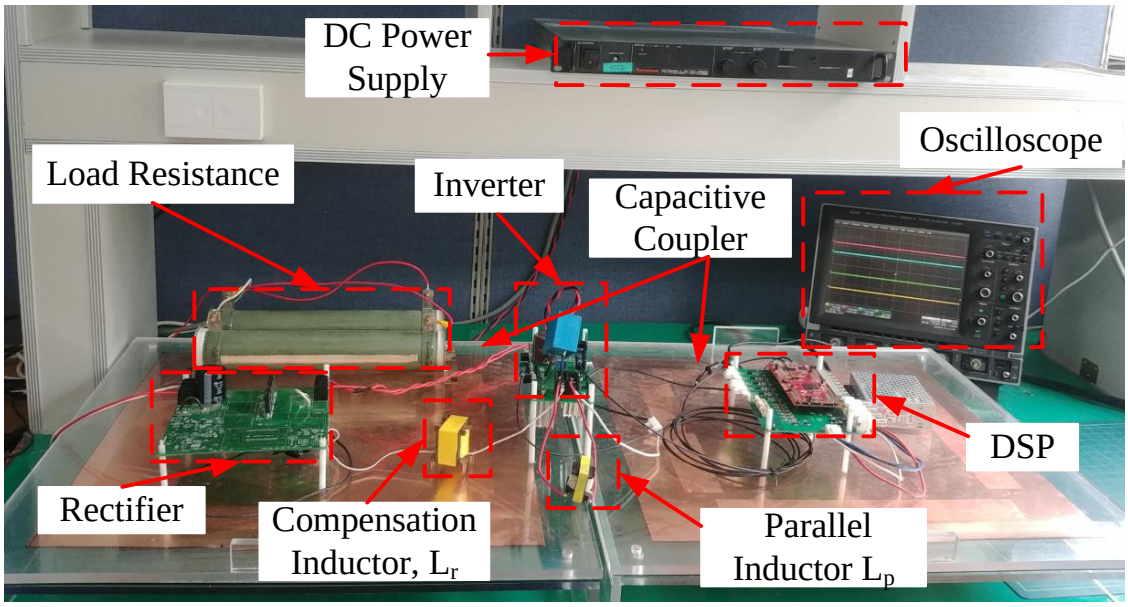
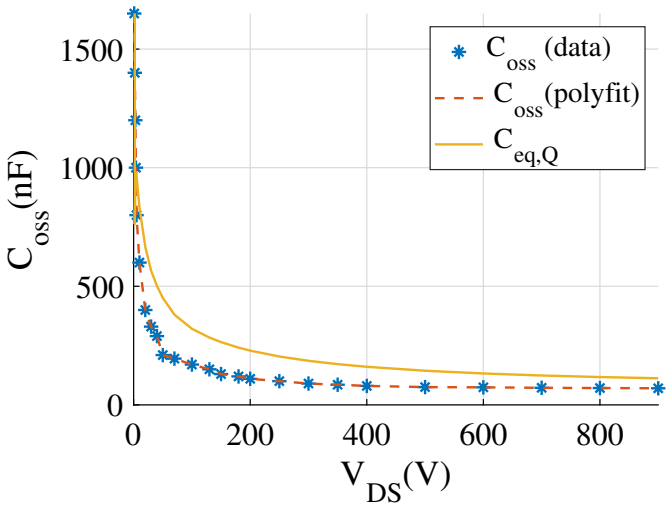
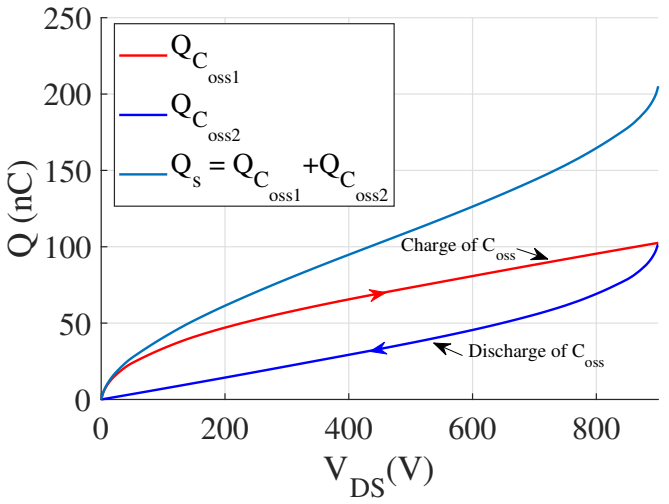


Figure 4-8: Experimental setup of the proposed CPT system.



(a)

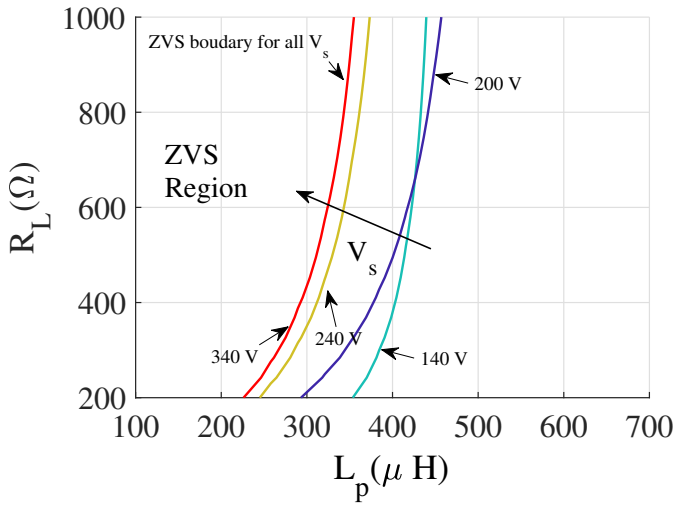


(b)

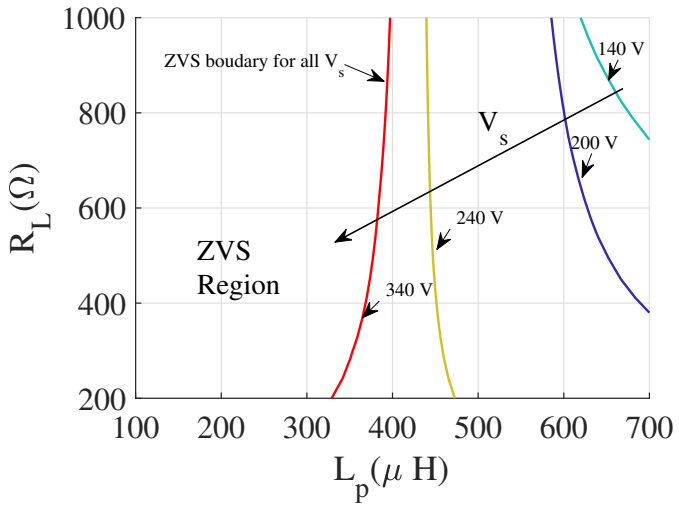
Figure 4-9: Nonlinear output capacitance characteristics of the MOSFETs (a) C_{oss} and $C_{eq,Q}$ (b) Q_{oss} for C3M0065090D (CREE).

4.5.1 Hardware Implementation

The experimental setup is shown in Fig. 4-8. Four copper plates of capacitive coupler are identical (500 mm x 500 mm). The dielectric medium between the two plates is glass and the distance between two plates is 4 mm. The capacitance is measured using the Agilent 4263B LCR meter. Silicon Carbide (SiC) power MOSFETs (C3M0065090 CREE) are used as the switches. The output capacitor C_{oss} and charge-linear capacitance, $C_{eq,Q}$, can be plotted as a function of drain-source voltage in Fig. 4-9(a) while the total charge of the output capacitor for the switch, Q_{oss}, is shown in Fig. 4-9(b). The UCC21530 gate driver from Texas Instrument was used for driving the switches. SiC Schottky diodes (C3D16060D



(a)



(b)

Figure 4-10: ZVS boundary with various input voltage ,V_s , resistive loads, R_L, and inductance, L_p, for (a) switch S_1 (b) switch S_2.

CREE) with forward voltage $V_f = 1$ V are utilized for the output rectifier.

In the calculation of total stored charge, Q_s in S_1 and S_2, the MOSFET characteristics in Fig. 4-9 were utilized. The ZVS boundaries for S_1 and S_2 under input voltages from 140 to 340 VDC were calculated as shown in Fig. 4-10 with various values for L_p. It can be seen that the ZVS range is wider under a low input voltage of $V_{s,min} = 140$ V and the narrowest ZVS range occurs with the highest input voltage of $V_{s,max} = 340$ V. It should also be noted that the ZVS region of S_1 is narrower than that of S_2, this is due to the critical inductance at the ZVS boundary of S_1 and S_2 being 220 μH and 340 μH, respectively. The ZVS region shrinks with increasing L_p and also contracts under heavy loads. Therefore, the

Table 4.1: System parameters for the experiment.

Symbol	Parameters	Values	Unit
V_s	DC Input Voltage (100 to 240 VAC)	140-340	V
V_o	DC Output Voltage	180	V
f_s	Switching frequency	83	kHz
L_p	Parallel inductance	220	μH
L_r	Resonant tank inductance	2.77	mH
C_{link}	Total link capacitance	2.5	nF
C_c	Clamp capacitance	20	μF
t_d	Dead time	0.15	μs
R_{L_p}	Parallel inductor resistance	0.1	Ω
R_{Lr}	Compensation inductor resistance	0.2	Ω
$R_{C_{link}}$	Capacitor tank resistance	5.8	Ω

optimal inductance L_p is chosen such that both switches S_1 and S_2 achieve ZVS for all load conditions.

To maximize efficiency, the switching and conduction losses should be minimized. As discussed above, the inductance L_p should be chosen optimally to meet the ZVS conditions. The efficiency as a function of inductance L_p was calculated using (4.22) and then plotted for four operating cases in Fig. 4-11. When L_p is lower than the critical value of the ZVS boundary for S_1 and S_2, ZVS is achieved, however, the efficiency is poor because of large conduction and copper losses in the switches and L_p, respectively. On the contrary, in the higher L_p region, the efficiency is also reduced due to the failure of ZVS. As such, maximum efficiency is achieved near the ZVS boundary. Accordingly, an inductance value, L_p, of 220 μH is choose, this is the boundary value where both S_1 and S_2 achieve ZVS. Following the design procedure in subchapter 2.1, the experimental parameters were obtained as shown in Table 4.1.

The system is operated at its resonant frequency without a phase-shift between the current and voltage in the resonant tank. The buck-boost half bridge topology is tested at four extreme operating points with input voltage of $V_{s,min}$ = 140 V and $V_{s,max}$ = 340 V and $R_{L,min}$ = 200 Ω and $R_{L,max}$ = 1000 Ω for the load resistance. The target output voltage, V_o, is fixed as 180 V by duty cycle modulation. Measurements was made using oscilloscopes (WaveSurfer 24MXs-B, Teledyne LeCroy). The recorded waveforms are shown in Fig. 4-12 and 4-13.

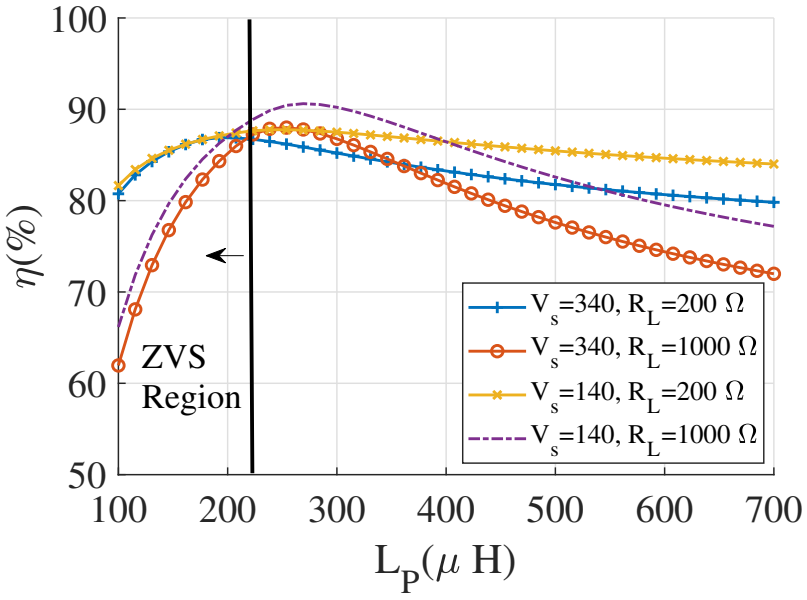


Figure 4-11: Calculated efficiency for four cases of extreme operating conditions with various values for L_p.

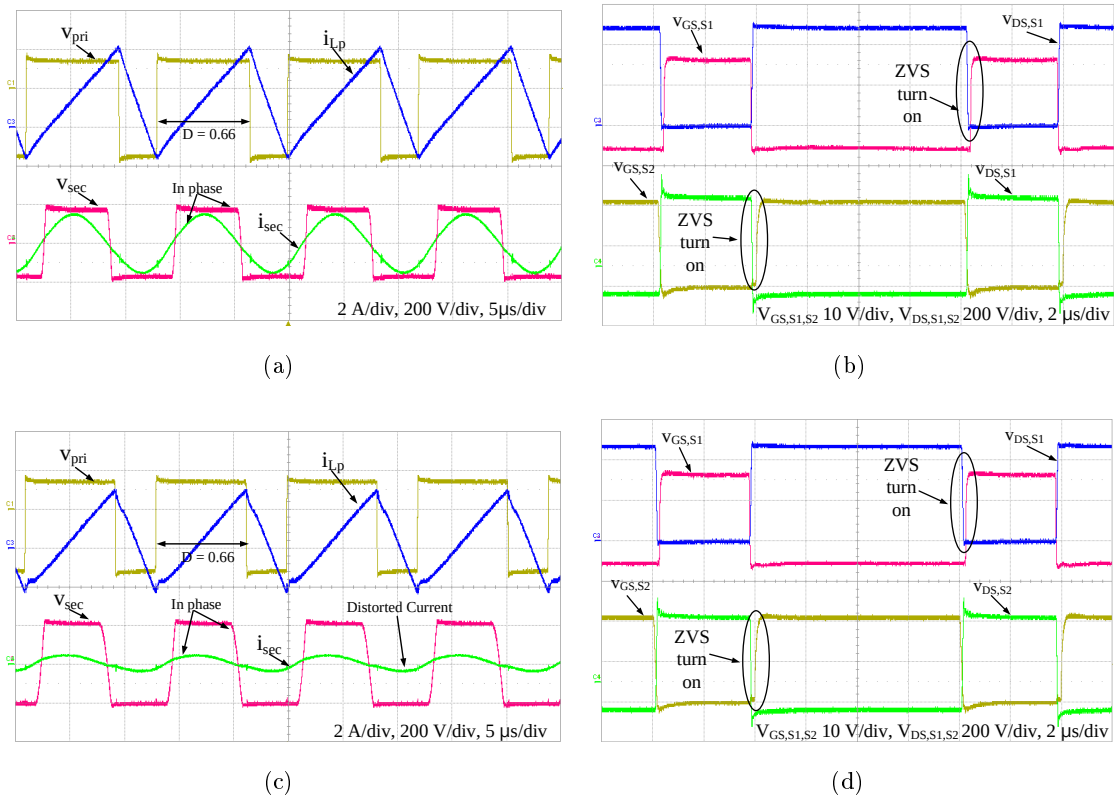


Figure 4-12: Experimental waveforms in boost mode (V_s = 140 V) (a) v_{pri}, i_{L_p}, v_{sec}, and i_{tank} for R_L = 200 Ω (b) waveforms of S_1 and S_2 for R_L = 200 Ω (c) v_{pri}, i_{L_p}, v_{sec}, and i_{tank} for R_L = 1000 Ω (d) waveforms of S_1 and S_2 for R_L = 1000 Ω

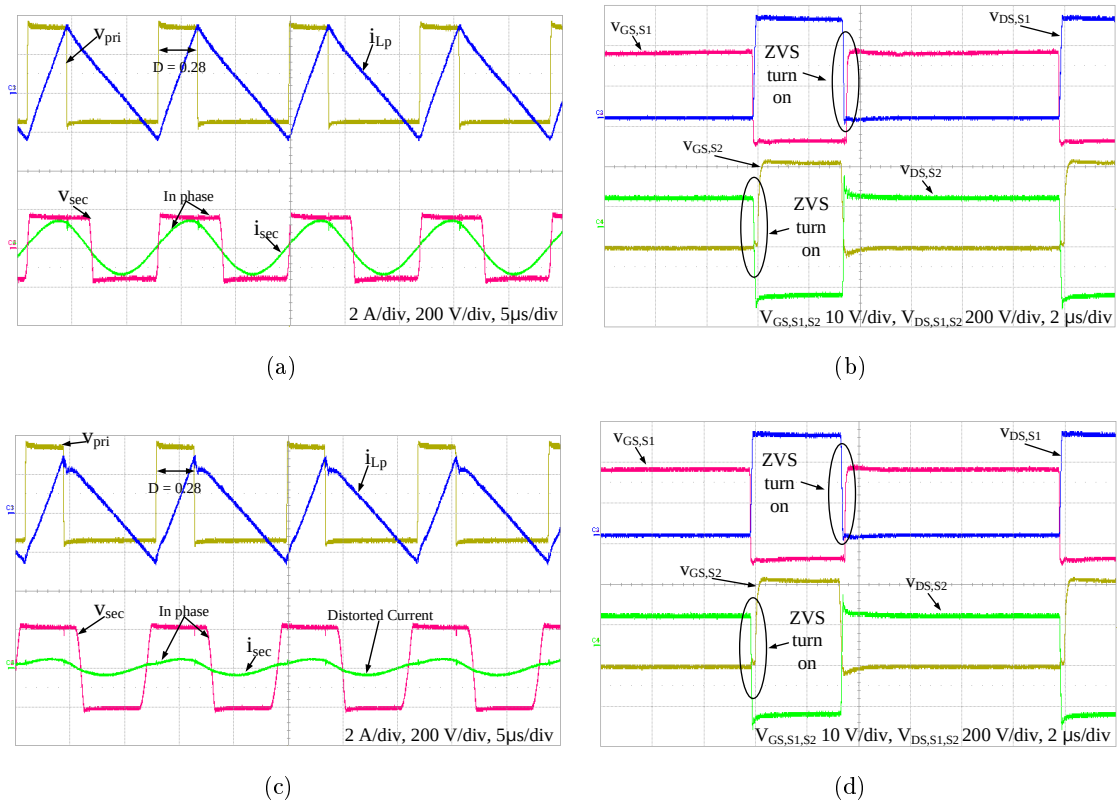


Figure 4-13: Experimental waveforms in buck mode (V_s = 340 V) (a) v_{pri}, i_{L_p}, v_{sec}, and i_{tank} for R_L = 200 Ω (b) waveforms of S_1 and S_2 for R_L = 200 Ω (c) v_{pri}, v_{L_p}, v_{sec}, and i_{tank} for R_L = 1000 Ω (d) waveforms of S_1 and S_2 for R_L = 1000 Ω.

4.5.2 Experiment Results

Line Regulation

The buck-boost half bridge topology was operated in boost mode ($D \geq 0.5$) when the input voltage, V_s, was 140 V, while the duty cycle, D, was set to 0.66 for both cases of R_L = 200 Ω and 1000 Ω. Fig. 4-12(a) and 4-12(d) show that the primary voltage, v_{pri}, is 140 V in the positive period and 304 V in the negative period. The current in the parallel inductor, i_{L_p}, linearly increases and decreases. Meanwhile, the secondary voltage, v_{sec}, and the secondary current, i_{sec}, are in phase, which shows resonant frequency operation. The secondary current is slightly distorted due to the low load quality factor at R_L = 1000 Ω as shown in Fig. 4-12(d).

The system was operated in buck mode ($D \leq 0.5$), as shown in Fig. 4-13, under an input voltage of 340 V, while the duty cycle was set to D = 0.28 to regulate output voltage.

ZVS Operation

ZVS was achieved for all operating cases as shown in the waveforms of switches S_1 and S_2 in Fig. 4-12 and 4-13. It is also possible to further improve the efficiency by varying the inductance of L_p according to operation conditions as in [80], but in this chapter we adopted a constant inductance value.

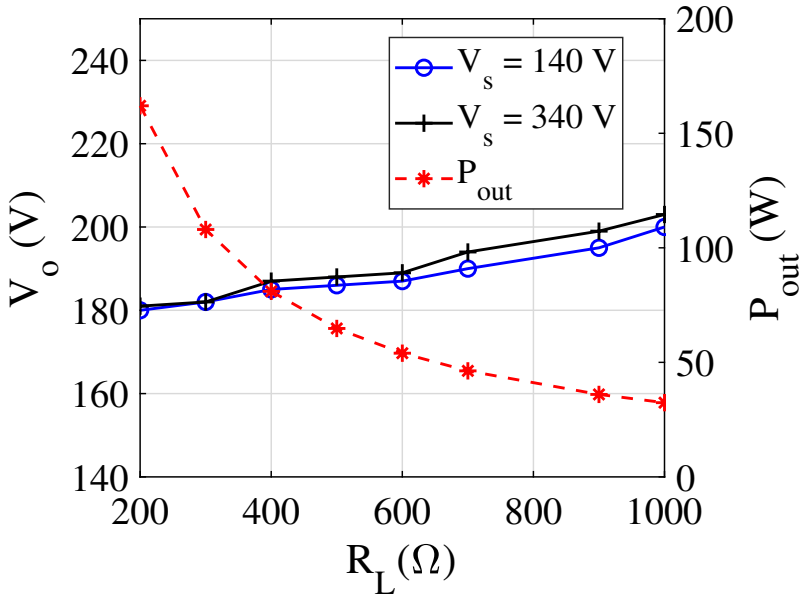


Figure 4-14: Measurement of the load regulation.

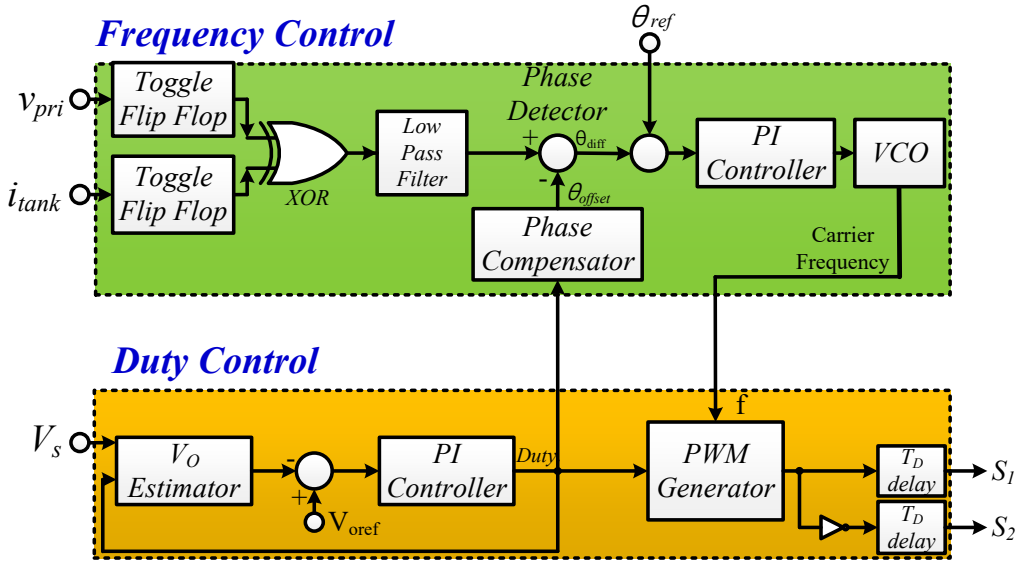


Figure 4-15: The dual-mode control scheme.

Load Regulation

Fig. 4-14 shows the inherent load regulation. This illustrates the output voltages of the two cases with V_s = 140 V and 340 V are almost the same. The voltage differences, ΔV, at 200 Ω and 1000 Ω are just 20 V and 21 V for V_s = 140 V and 340 V, respectively. This is because R_L = 1000 Ω will produce a slightly higher secondary voltage compared with R_L= 200 Ω due to the low voltage drop from parasitic resistance. Even though these test results only contain open loop characteristics, these kinds of inherent load regulation features can alleviate the burden of load regulation in the additional DC-DC converter. If the duty cycle is further adjusted by the output feedback control, load regulation will be further improved. In this case, it will eliminate the necessity of the addition of a DC-DC converter to the secondary stage.

The output voltage tends to rise under light-load conditions under open-loop control as shown in Fig. 4-14. This behavior can be attributed to two primary reasons. First, the voltage gain characteristics change as the load resistance increases, leading to a higher quality factor; this results in a voltage gain greater than one [121], [122]. Second, the parasitic capacitance of the rectifier diodes due to their inherent junction capacitance becomes more significant at high switching frequencies. Under light-load conditions, this capacitance can store and transfer energy to the output, contributing to a gradual increase in output voltage [123] [124]. Additionally, it can shift the effective resonant frequency, further increasing the voltage gain unintentionally. These combined effects can cause the output voltage to exceed expected levels, which must be carefully considered in the design and control of resonant converters.

Series resonant performance under light-load conditions is significantly influenced by the parasitic junction capacitance of the rectifier diodes (C_j) [125] as shown in Fig. 4-16. Crucially, the total parasitic junction capacitance of the rectifier diodes, C_j, is included in parallel with the load. The resulting AC model is shown in Fig. 4-17 which is a LCC resonant converter [126, 127].The complete transfer function of the SRC including parasitic capacitance C_j is:

$$G_v(s) = \frac{sR_{ac}C_r}{s^3(L_rC_rR_{ac}C_j) + s^2(L_rC_r) + s(R_{ac}C_j + R_{ac}C_r) + 1} \tag{4.40}$$

The critical behavior is observed under the no-load condition, where $R_{ac} \to \infty$. To analyze

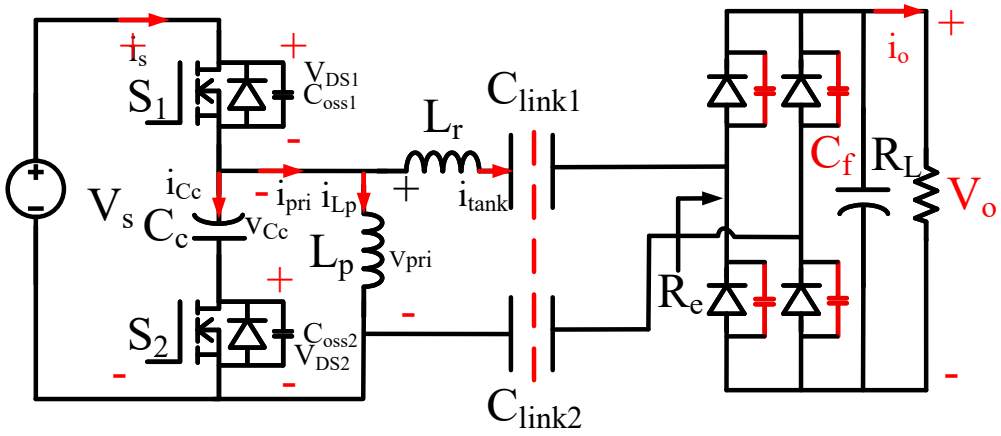


Figure 4-16: The proposed CPT system including parasitic junction capacitance C_j of secondary side diode rectifier.

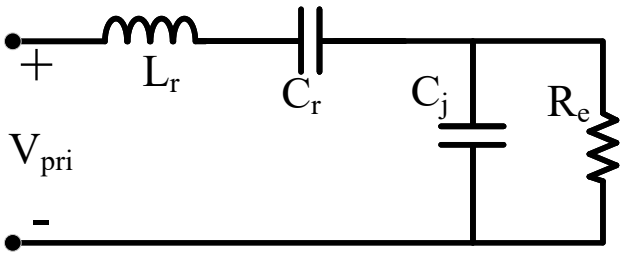


Figure 4-17: AC equivalent circuit of the proposed CPT system including parasitic junction capacitance C_j of diode rectifier.

this, we take the limit of Eq. (4.40) as R_{ac} approaches infinity.

$$G_v(s)\Big|_{\text{No-Load}} = \lim_{R_{ac}\to\infty} G_v(s) = \frac{1}{s^2 L_r C_j + \frac{C_j}{C_r} + 1} \tag{4.41}$$

Rearranging this into the canonical second-order low-pass filter form gives:

$$G_v(s)\Big|_{\text{No-Load}} = \frac{\frac{C_r}{C_r+C_j}}{s^2 L_r \frac{C_r C_j}{C_r+C_j} + 1} = \frac{K_{dc}}{s^2/\omega_{n,NL}^2 + 1} \tag{4.42}$$

The absence of a first-order term (s^1) in the denominator of (4.42) indicates a Quality Factor (Q) of infinity. This results in a theoretically infinite gain peak at the no-load resonant frequency, $\omega_{n,NL}$, presenting a severe overvoltage risk. However, the gain remains unity at the resonant frequency ω_o. Therefore, the operating frequency should be carefully designed to accurately track the resonant frequency tp prevent the overvoltage at high frequency.

To improve output voltage regulation under light-load conditions, closed-loop control can be implemented [128] [129]. Fig. 4-15 shows the block diagram of the dual-loop controller,

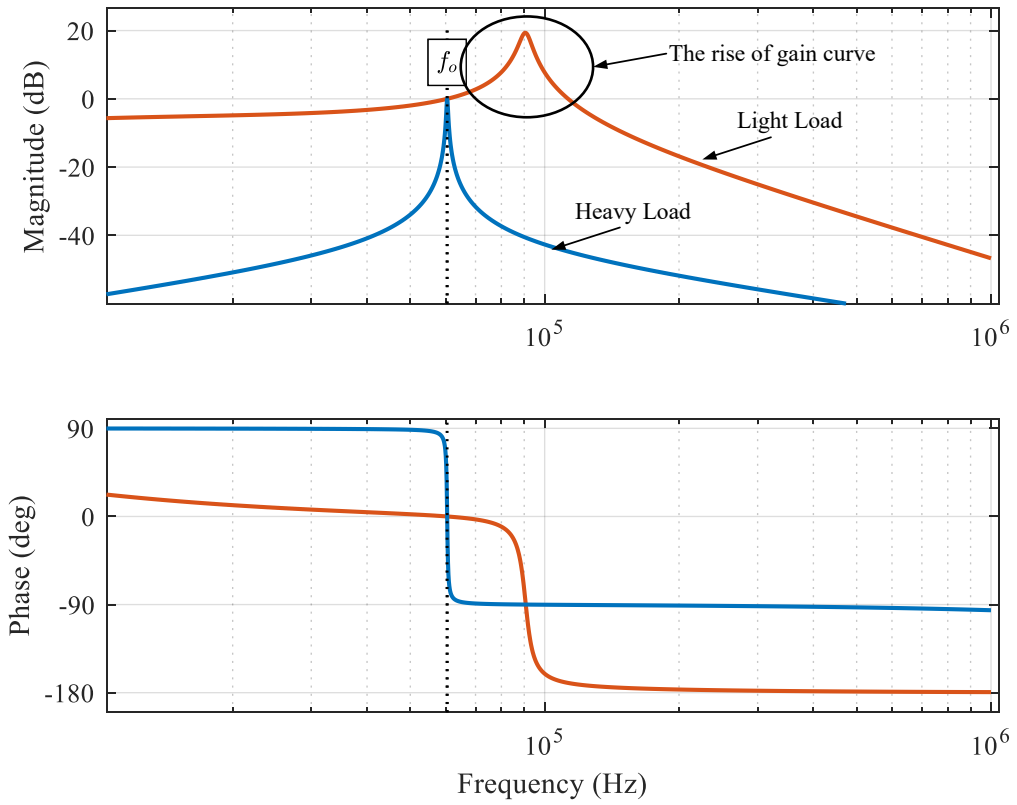


Figure 4-18: Bode plot of proposed CPT system with C_j under heavy load and light load.

which consists of a frequency control loop and a duty control loop [129]. The frequency control loop employs a Phase-Locked Loop (PLL) to maintain operation at the resonant frequency. It works by minimizing the phase difference (ϕ_{diff}) between the primary voltage (V_{pri}) and the resonant current (i_{Lr}). A Proportional-Integral (PI) controller drives this phase difference to zero, and its output adjusts a Voltage-Controlled Oscillator (VCO) to generate the precise switching frequency. To prevent PLL malfunctions caused by asymmetric input waveforms, additional components, including two toggle flip-flops and a phase compensator, are included [129].

In parallel, the duty control loop regulates the output voltage. It uses the DC input voltage and the carrier frequency from the frequency controller as inputs. The control tasks are decoupled: the frequency loop tracks shifts in the resonant frequency (addressing load regulation and alignment errors), while the duty loop regulates the output voltage. Although these two loops operate almost independently, they are weakly coupled through gain deviations caused by latency in the frequency loop and phase delays arising from primary-side voltage asymmetry.

In this work, the second-order generalized integrator frequency control loop algorithm (SOGI-FLL) is used to achieve frequency tracking as shown in Fig. 4-19 [100, 130]. Tuning the SOGI-FLL involves adjusting two main parameters: k and γ. The SOGI gain k controls the trade-off between filtering quality (better with smaller k) and the dynamic response of the SOGI's orthogonal outputs. The FLL gain γ determines the speed and stability of the frequency tracking loop, where a larger γ yields faster frequency estimation but can reduce noise immunity and stability. Optimal tuning requires balancing these factors through simulation and iterative adjustments based on specific application needs like signal quality and desired tracking performance. The tuning parameter effects for the SOGI-FLL are shown in Table 4.2.

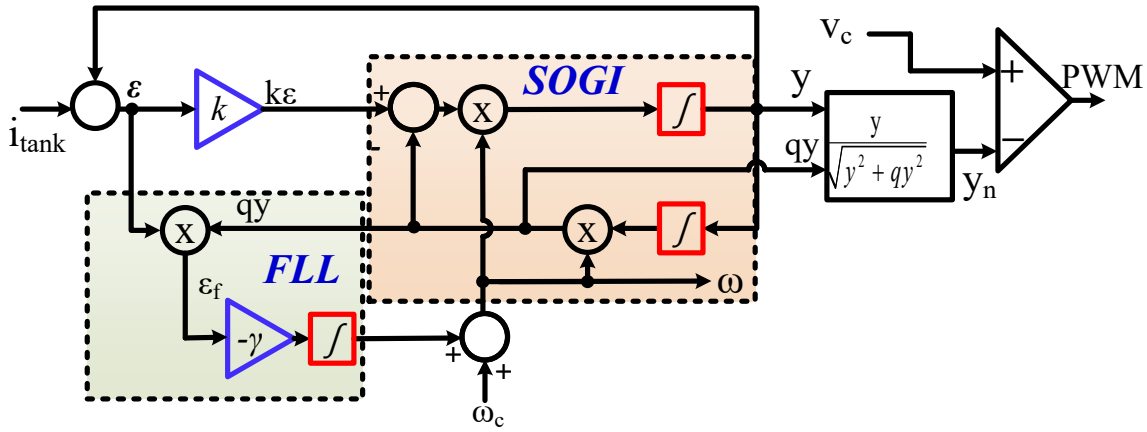


Figure 4-19: Schematic diagram of SOGI-FLL.

Table 4.2: Tuning Parameter Influence on SOGI-FLL Dynamics and Filtering

Parameter	Change	Overall Dynamics	SOGI Filtering
SOGI Gain (k)	↑	Faster (+)	Worse (-)
	↓	Slower (-)	Better (+)
FLL Gain (γ)	↑	Faster (+)	No Direct Impact (0)
	↓	Slower (-)	No Direct Impact (0)

- '(+)': Improvement (e.g., faster dynamics, better filtering).
- '(-)': Degradation.
- '(0)': No primary direct impact.

The simulation is tested under condition where the load is varied from 900 Ω to 300 Ω under a 50 % misalignment condition. Stabilizing the system by appropriately tuning the

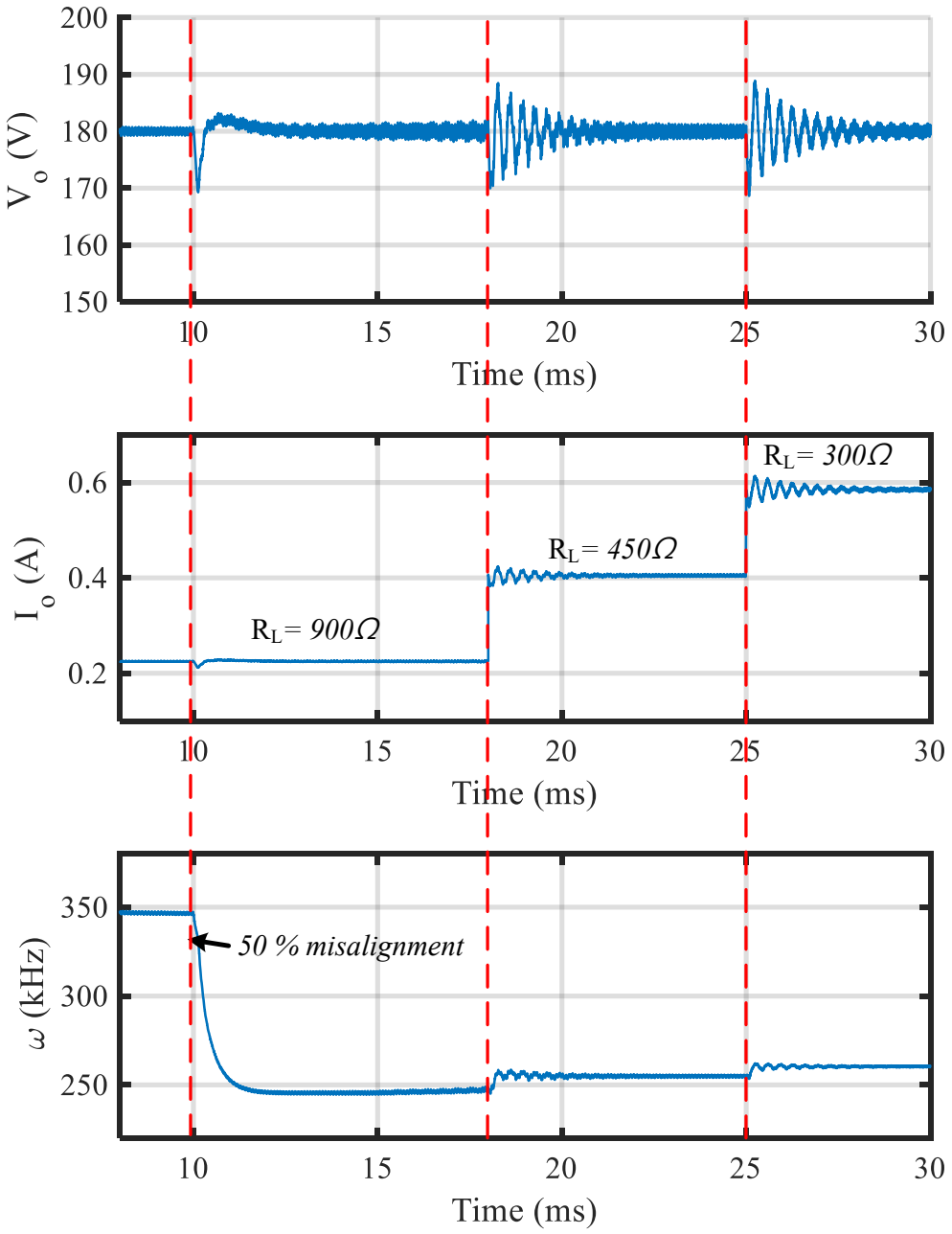


Figure 4-20: Simulation results with dual-mode control scheme under misalignment and load change.

controller gains specifically the parameters of the SOGI-FLL is essential. The SOGI-FLL relies on the tuning of its gain parameter (k, γ) to balance between dynamic response speed and stability. Therefore, careful optimization of the SOGI-FLL parameters in simulation allows for the identification of suitable gain values that ensure stable and accurate estimation of the system frequency. Therefore, SOGI Gain k and FLL Gain γ are designed at k = 0.1

and γ= 50000. The simulation result achieves a balance between dynamic response speed and stability as shown in Fig. 4-20, demonstrating good performance. The average of the output voltage is kept at 180 V, which is significantly improved compared with open-loop.

Efficiency and Power Losses

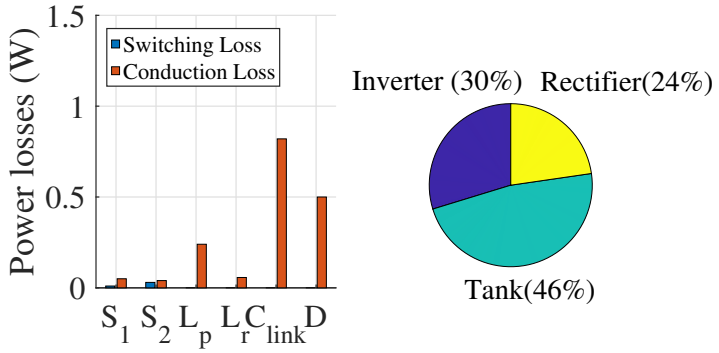
The losses from the proposed structure for optimal load condition were calculated using LTspice software as shown in Fig. 4-21. The power losses from the switches in all cases are very small due to ZVS operation. The losses come mainly from the conduction loss of the capacitive coupler. System efficiency under variable load conditions was measured by a PPA5530 power analyzers, and the results are shown in Fig. 4-22. When V_s = 140 ($D = 0.66$) the system efficiency and optimal load resistance is slightly higher than in case V_s = 340 (D = 0.28), which matches well with calculated value shown in Fig. 4-7. The values of optimal load resistance for both cases are around 700 Ω at maximum efficiency 88.2 %. The efficiency can be further improved by parameter optimization of resonant link and capacitive coupler [131, 132]. Moreover, maximum efficiency tracking [108] can be used to keep the system operating at maximum efficiency.

4.5.3 Comparison and Discussion

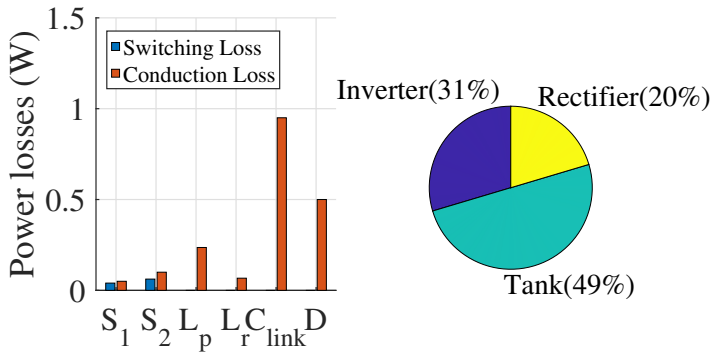
Table 4.3 shows the comparisons of the proposed HF inverter with the previous topology. The most previous CPT systems consist of two-stage architecture with additional DC-DC converter [108–110]. However, limitation of the two-stage system is the increased volume and reduced efficiency. Class E topology used in [111] has the metric of single switch operation. However, it is just suitable for low power and low voltage input application due to the high voltage stress. Furthermore, HF inverters in [108–111] require that the switching frequency should be kept above the resonant frequency to achieve ZVS, which makes the voltage gain dependent on the load resistance and ZVS operation lost at light load condition.

The single-stage structure of this chapter has advantages of high overall efficiency and simple circuit. Besides, inherent load regulation due to the resonant frequency operation and wider ZVS range are additionally obtained. Those features at together make the high efficiency in the proposed system with 88.2 % in peak value.

In practical cases, the misalignment of the capacitive coupler is unavoidable. In that case, the frequency regulation can be used for tracking the resonant frequency of system [14]. The design procedure and analysis in this chapter can be also applied in that case with



(a)



(b)

Figure 4-21: Theoretical loss-breakdown at the optimal load condition ($R_L = R_{L,opt}$) (a) $V_s = 140$ V (b) $V_s = 340$ V.

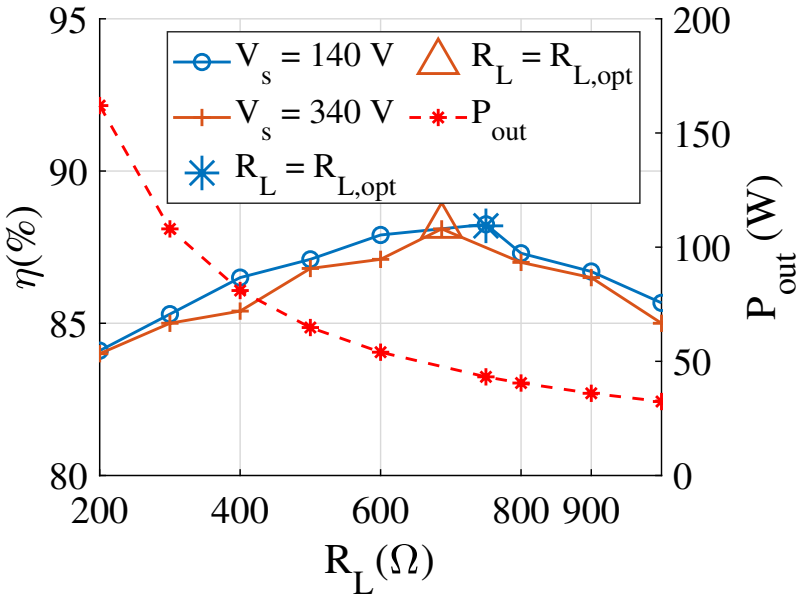


Figure 4-22: Measurement of the DC-DC efficiency.

the additional condition of the frequency range. However, a detailed analysis of the variation of the air gap is beyond the scope of this chapter.

Table 4.3: Comparisons with the previous HF inverter for CPT system.

Ref.	Driving topology	No. of additional DC-DC converters	Inherent load regulation	ZVS at light load condition	Input/output Voltage (V)	Output Power (W)	Maximum efficiency (%)
[108]	Half Bridge	1	No	Partial switches	50/22-33	27.5	75
[109]	Full Bridge	2	No	Partial switches	120/120	300	84
[110]	Full Bridge	1	No	Partial switches	35/5	3.7	80
[111]	Class E	0	No	Partial switches	24/20	10	77
This chapter	Buck-boost Half Bridge	0	Yes	All switches	140-340/180	160	88.2

4.6 Conclusion

This chapter proposes a single-stage topology for low-cost capacitive wireless power transmission. The proposed single-stage structure was tested with a wide input voltage range that is compatible with the universal AC input voltage range and a wide load range to verify my theoretical analysis and show its performance. Test results showed that the proposed system features wide voltage gain, simple gate driving, wide ZVS range, less active components, and inherent load regulation. The excellent characteristics shown above further strengthen the merit of the proposed single-state CPT systems over conventional systems, particularly in terms of cost-effectiveness, simple control, and reduced volume.

Chapter 5

Tapped-Inductor Inverter/Rectifier Structure with Integrated Matching Networks for Capacitive Power Transfer System

In conventional capacitive wireless power transfer (CPT) system, high frequency (HF) inverter and matching network are separately considered for system design. Moreover, front-end or back-end dc-dc converters are usually added for voltage regulation. However, the multi-stage of conventional system becomes costly and complex. By combining the wide voltage gain advantage of buck-boost inverter and tapped-inductor, a family of inverter is presented, which merges the functions of HF inverter and impedance matching network. By duality of inverter and rectifier, a family of rectifier is also proposed which provides impedance matching network as well. Thereby, front-end or back-end dc-dc converter is eliminated due to wide voltage gain voltage feature of the proposed topology. In this thesis, the operation principle and gain properties of the proposed system are presented for both constant current (CC) output and constant voltage (CV) output modes.

5.1 Introduction

A general two-stage CPT system architecture is shown in Fig. 5-1. The high frequency (HF) inverter is used to produce ac voltage. The input match network (IMN) and the output

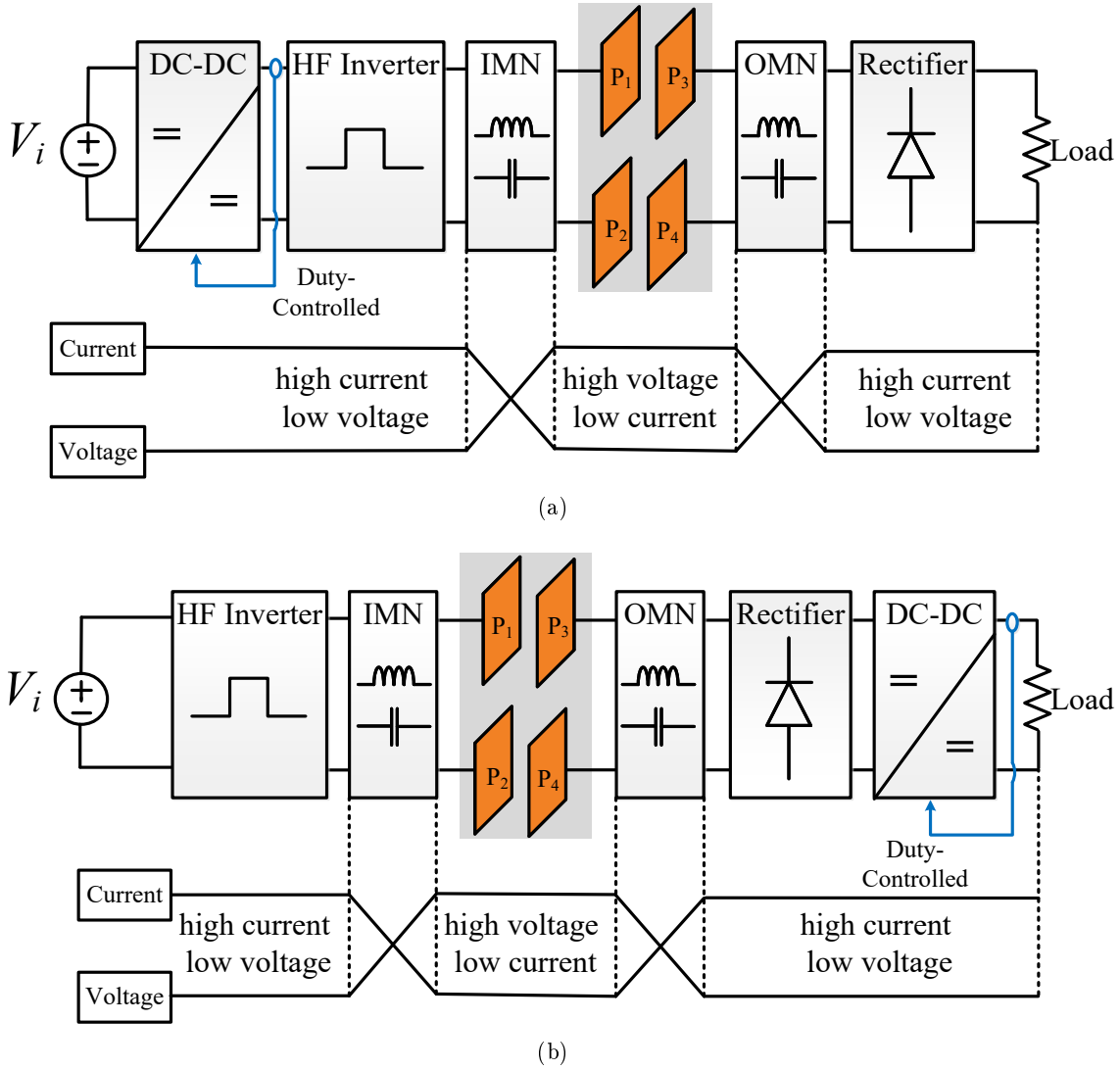


Figure 5-1: Conventional two-stage CPT system architecture with (a) front-end dc-dc converter (b) back-end dc-dc converter.

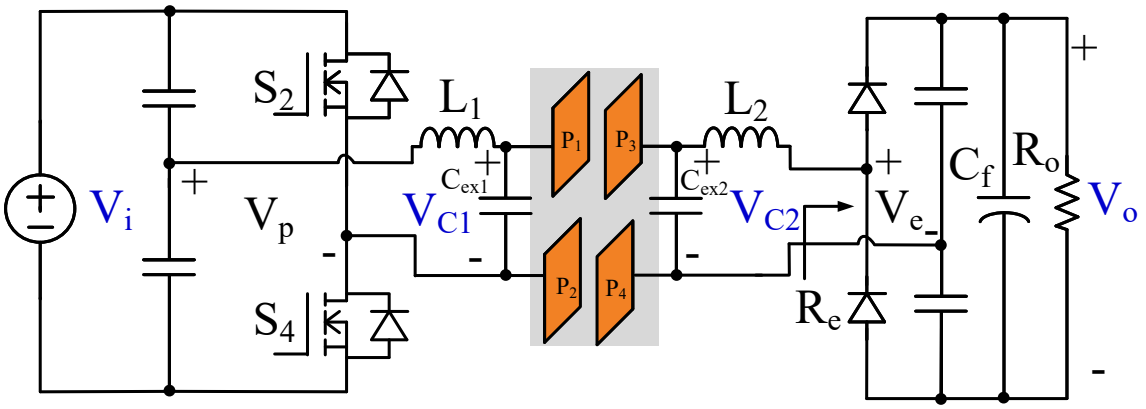
matching network (OMN) are used as compensation circuits. The rectifier circuit is used to convert ac voltage to dc voltage. The front-end or back-end dc-dc converter is mostly used to regulate the input or output voltage [37]. The capacitance of a CPT coupler is usually from a hundred picofarads to a few nanofarads due to the naturally low permittivity of the vacuum and air. This results in high impedance of a CPT coupler, which makes the high voltage stress in the coupler and it is the most significant limitation of CPT system. According to IEEE standard for safety level with respect to human exposure to electric, the electric field strength should be limited at 614 V/m with frequency range from 0.1 to 1.34 MHz [133]. To reduce coupler voltage stress, there are two common solutions in literature. First, switching frequency is increased to reduce the impedance of the capacitive coupler. However,

due to the limited switching characteristics of power semiconductor devices, the switching frequency could not be easily increased beyond a few megahertz. Second, the IMN at the primary is utilized to boost the voltage before the capacitive coupler to reduce the current through the capacitive coupler and then voltage is reduced back to the output voltage by OMN as shown in Fig. 5-1, which is considered more realistic way than the first one.

Various types of matching networks have been proposed in the literature to accommodate the second solution, such as L, LC, LCL, LCLC, and double-sided transformers. The advantage of the series L-compensation is its simplicity [28]. However, it still requires switching frequency to be in MHz range to provide sufficient power capability. The advantage of the double-sided LC compensation circuit is its feasibility in long distance application [29]. The LCL compensation is the combination of L and LC [30]. Double-side LCLC can maintain a high coupling coefficient for efficiency consideration. However, the complex design of the double-sided LCLC compensating circuit is a disadvantage [31] because the circuit has eight passive components. Furthermore, adding more components to the circuit can result in additional power losses, lowering system efficiency. As demonstrated in [32, 134], the double-sided transformer compensation network can also be utilized for impedance transformation. However, due to the bulkiness of the transformer, the size of the system increases. Other high order compensation networks have been proposed in [20, 33], increasing complexity and component count. Some special shape of compensation network has been proposed in the literature [34–36, 135]. The drawbacks of conventional compensation can be summarized low voltage gain (L, CL), design complexity, component count (LCLC, double-sided LCLC), and bulkiness (double-sided transformer).

To reduce the burden of matching network it is advisable to adopt the high gain HF inverter/rectifier. However, the half-bridge and full-bridge topology are most commonly used [20] and those kinds of buck type inverters cannot afford a wide control range, and thus front-end or back-end dc-dc converter are usually added for the voltage regulation, as shown in Fig. 5-1 [37]. However, the multi-stage the system becomes costly and complex. The buck-boost inverter has been proposed to overcome this issue [117, 136]. However, the output voltage gain of the buck-boost inverter is limited by the voltage stress of main power switches. Therefore, buck-boost topology is not enough to obtain the voltage-boosting required for the CPT system.

In the literature, it is reported that the tapped-inductor topology can extend the control range and increase voltage gain of the converter [137, 138]. Therefore, by combining the



(a)

Figure 5-2: Conventional CPT systems double side LC compensation with half bridge inverter and half bridge rectifier.

buck-boost inverter and tapped-inductor, a new family of inverter can be presented with the integrated impedance matching network. By the duality of inverter and rectifier, a new family rectifier can be also proposed with the integrated impedance matching network. The complex compensation network and the additional dc-dc converter can be eliminated. In other words, the function of the compensation network and the dc-dc converter can be merged into a a single-stage HF inverter located on the primary side and the function of the compensation network and the rectifier can be merged into a single rectifier on the secondary side.

5.2 Tapped-Inductor Inverter/Rectifier Structure with Integrated Matching Network for CPT System

5.2.1 Problem Definition

The capacitive coupler of CPT system in Fig. 5-2 containing four plates, $P_1 - P_4$ is used for the analysis. In the CPT system, the capacitance of a capacitive coupler is usually from a hundred picofarads to a few nanofarads due to the naturally low permittivity of air. This results in high impedance of a CPT coupler, which introduces the high voltage stress in the coupler.

To solve this issue, the most common solution is to put the reactive component on both sides of the capacitive couplers to step up the voltage before and step it down after the capacitive coupler. For that purpose, double-sided LC compensation is most common way

due to the simplicity and low component count as shown in Fig. 5-2 where C_{ex1} and C_{ex2} are external capacitor [31, 139]. For low and medium power application, half-bridge inverter and half-wave rectifier are frequently used in CPT system [20, 34, 39, 140]. The output voltage of inverter and the input voltage of rectifier are given by

$$V_p = \frac{\sqrt{2}V_i}{\pi} \sin\left(\frac{\pi(2D-1)}{2}\right), V_e = \frac{\sqrt{2}}{\pi} V_L \tag{5.1}$$

where V_i is the dc input voltage of high frequency inverter, V_e is the ac input voltage of rectifier, V_o is the dc output voltage at load resistance R_o, and D is duty cycle of half-bridge inverter. However, this kinds of buck type inverters cannot afford the wide control range, and thus front-end or back-end dc-dc converter are usually added for voltage regulation. The voltage before and after capacitive coupler are give by

$$V_{C1} = V_p + V_{L1}, \tag{5.2}$$

$$V_{C2} = V_e + V_{L2} \tag{5.3}$$

where V_{L1} and V_{L2} are voltage applied to the inductor L_1 and L_2, respectively.

In this chapter, the inverter, resonant tank, and rectifier are considered together to boost the voltage gain, thereby further reducing the voltage stress on the capacitive coupler. By merging the functions of the IMN and the front-end dc–dc converter into an HF inverter, and the OMN and the back-end dc–dc converter into a rectifier, the overall system can be simplified as shown in Fig. 5-3.

5.2.2 Circuit Topology of Tapped-Inductor Inverter/Rectifier with Integrated Matching Network

To achieve such a functionality, the novel inverter/rectifier configuration is presented in Fig. 5-4, featuring two switches, S_1 and S_2, which are controlled by asymmetrical pulse-width-modulated (APWM) gating pulses. The proposed configuration is formed by the combination of a clamp capacitor, C_{c1}, and a tapped-inductor, L_1. Tapped-inductor L_1 contains inductor L_{1a} and L_{1b} which are used for voltage boost as well as compensation for the capacitive coupler. Tapped-inudctor rectifier is also employed in secondary side to restore the voltage. Therefore, the proposed configuration with double-side tapped-inductor consists of a high-gain inverter with compensation on the primary side and a high-gain rectifier with

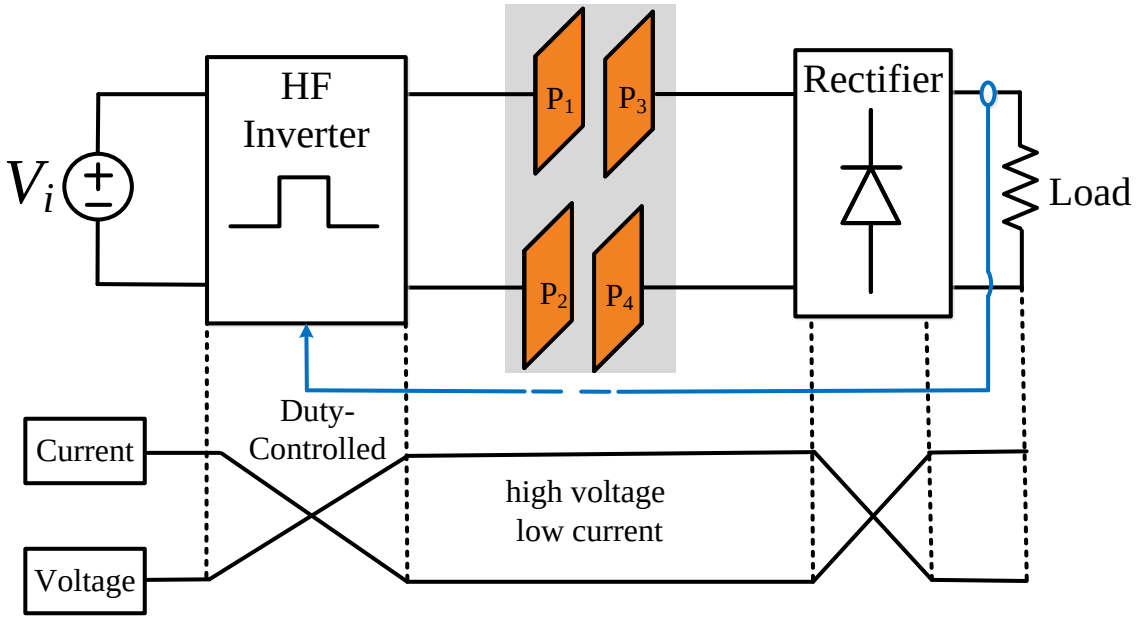


Figure 5-3: The proposed tapped-inductor inverter/rectifier integrated matching network structure for CPT system.

compensation on the secondary side as shown in Fig. 5-4. The various tapped-inductor inverter topologies can be derived as shown in Fig. 5-5, where the voltage V_p can be boosted up by the tapped-inductor.

By changing the configuration of topology in a similar manner as the tapped-inductor dc-dc converters [137, 138], the family of tapped-inductor inverter with integrated matching network is derived as shown in Fig. 5-5. The new-derived tapped-inductor inverter structure with integrated matching network for CPT system can be categorized in six ways: switch-to-tap in Fig. 5-5(a); switch and capacitor-to-tap in Fig. 5-5(b); output-to-tap in Fig. 5-5(c); output and capacitor-to-tap in Fig. 5-5(d); ground-to-tap in Fig. 5-5(e); ground and capacitor-to-tap in Fig. 5-5(f). By duality between inverter and rectifier, six versions of rectifier can also be derived as shown in Fig. 5-6.

5.3 Analysis of the Proposed Circuit

The topology shown in Fig. 5-4 is used as an example to describe the operation principles of the proposed topologies, where the inverter in Fig. 5-5(b) and the rectifier in Fig. 5-6(b) are integrated as a building block.

Before illustrating the operation and characteristics of the proposed system topology, the following assumptions are made:

1) The clamp capacitor voltage in both inverter and rectifier are considered constant due to a sufficiently large capacitance of C_{c1} and C_{c2} .

2) The two switches, S_1 and S_2, have identical characteristics.

3) All parasitic components except the output capacitance, C_{oss1} and C_{oss2}, of the switches are neglected.

4) The quality factor of the resonant tank is high enough to make a sinusoidal current assumption.

5) The output voltage is constant due to a sufficiently large C_f.

5.3.1 Operation Analysis of Inverter

The winding ratio of the tapped-inductor is a function of the inductances and is defined as

$$N_1 = 1 + \frac{M_1^2}{L_{1a}}, N_2 = 1 + \frac{M_2^2}{L_{2a}} \tag{5.4}$$

where M_1 is the mutual inductance between L_{1a} and L_{1b} for the primary tapped-inductor L_1 and M_2 is the mutual inductance between L_{2a} and L_{2b} for the secondary tapped-inductor L_2. The key operation waveforms of the proposed system are shown in Fig. 5-7. The operation of the proposed typology can be divided into four stages:

Stage 1 $[-\pi D \leq \omega t < \pi D]$: During this time interval, switch S_1 is on and switch S_2 is off as shown in Fig. 5-8(a). The primary voltage, v_p, is clamped to the input voltage, V_i, and the drain-to-source voltage of the switch S_2 is clamped as indicated in (5.5). The current in

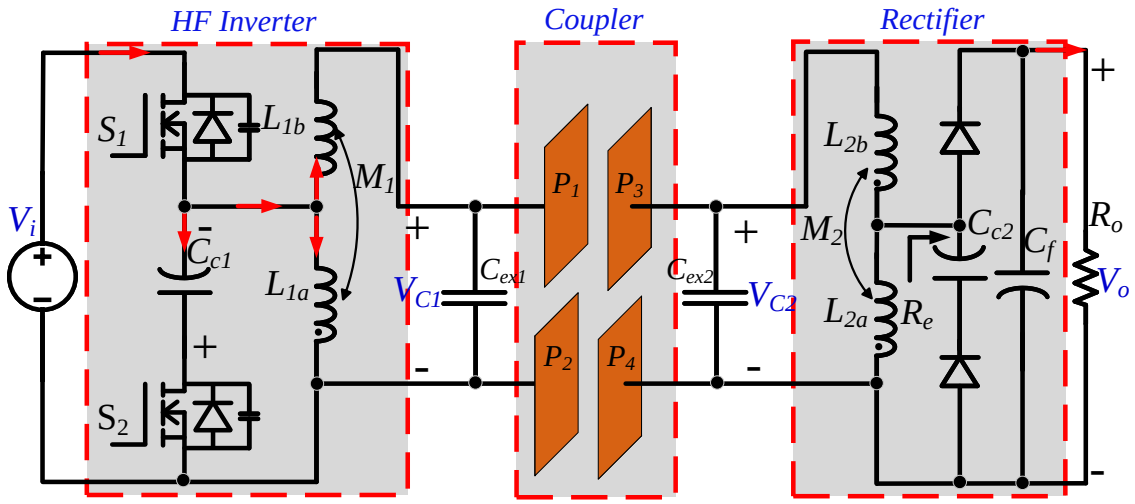


Figure 5-4: The proposed tapped-inductor inverter/rectifier system for CPT system.

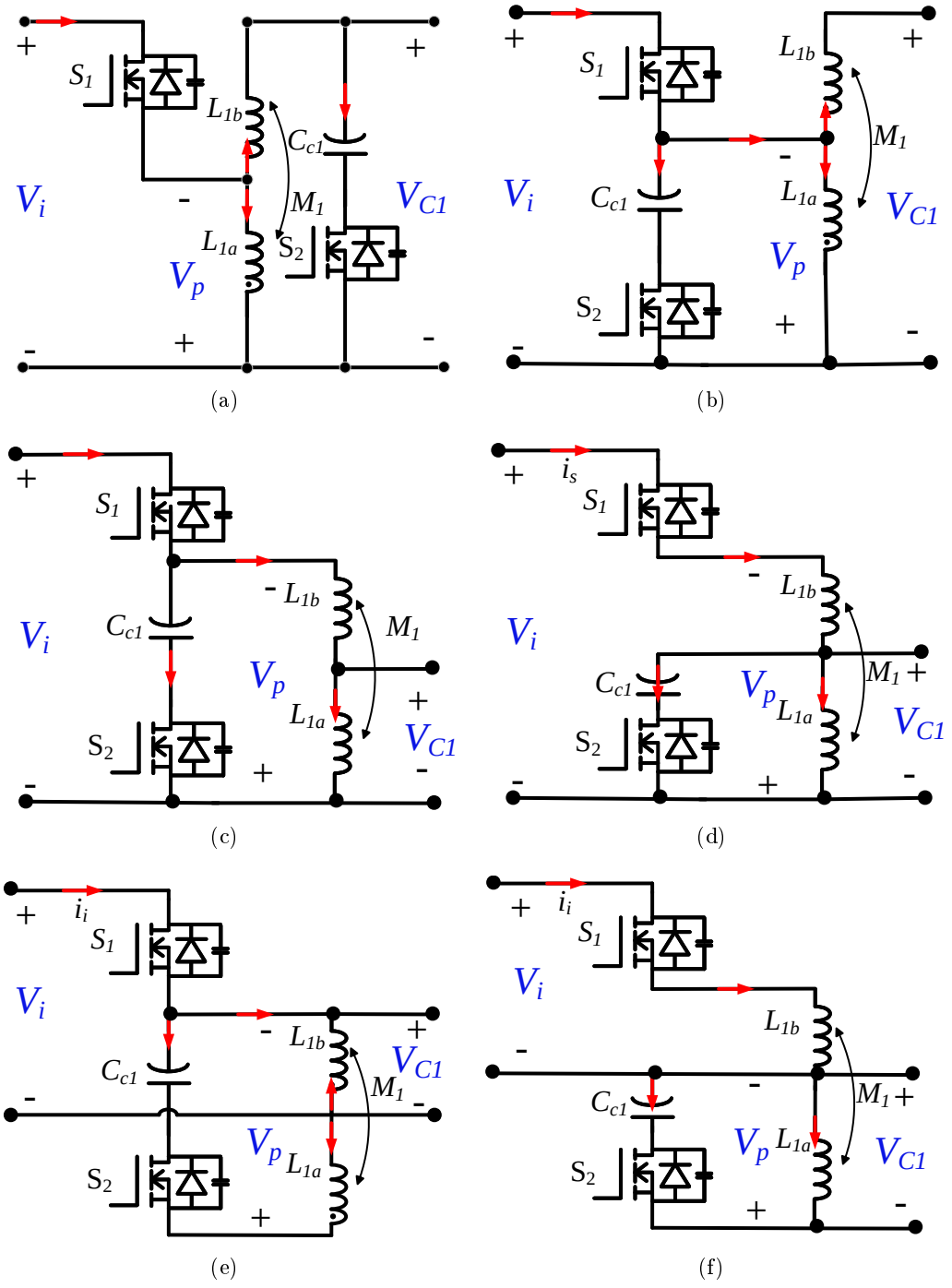


Figure 5-5: The family of tapped-inductor inverter with integrated matching network (a) switch-to-tap (b) switch and capacitor-to-tap (c) output-to-tap (d) output and capacitor-to-tap (e) ground-to-tap (f) ground and capacitor-to-tap.

inductor L_{1a} is given by (5.6).

$$v_{DS2}(\omega t) = \frac{V_i}{1-D} \tag{5.5}$$

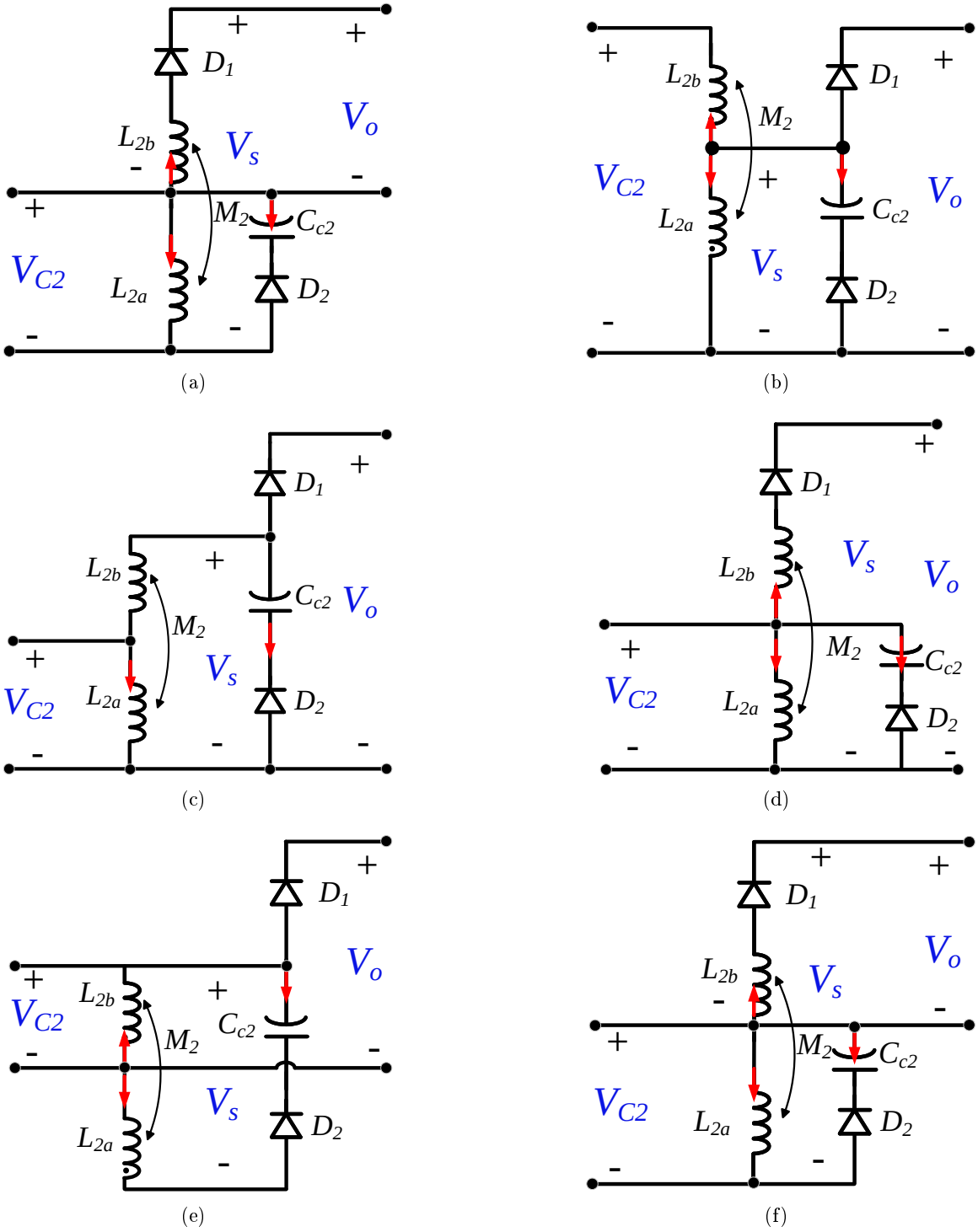


Figure 5-6: The family of tapped-inductor rectifier with integrated matching network (a) switch-to-tap (b) switch and capacitor-to-tap (c) output-to-tap (d) output and capacitor-to-tap (e) ground-to-tap (f) ground and capacitor-to-tap.

$$i_{L1a}(\omega t) = \int_{-\pi D_e}^{\omega t} -\frac{V_i d(\omega t)}{\omega L_{1a}} + \int_{-\pi D_e}^{\omega t} \frac{M_1 d(I_{L1b})}{L_{1a} d(\omega t)} d(\omega t) + i_{L1a}(-\pi D_e) \tag{5.6}$$

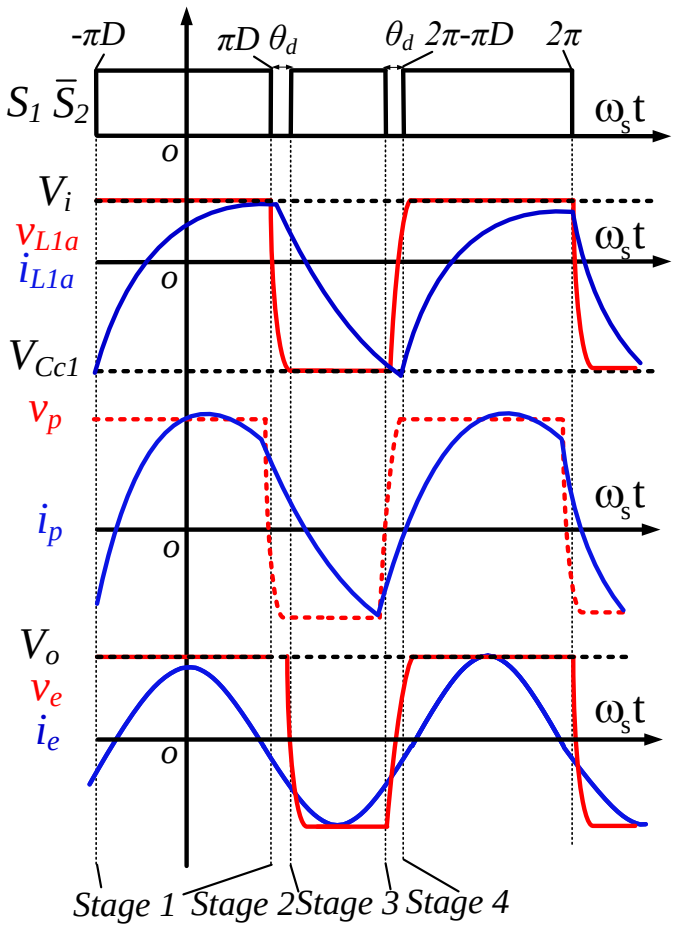
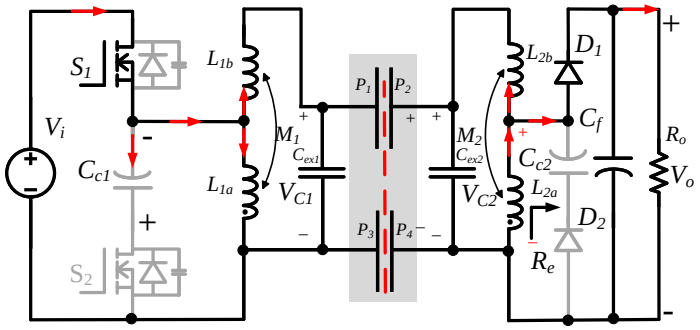


Figure 5-7: Key operation waveforms of the proposed tapped-inductor inverter/rectifier with integrated matching network for CPT system.

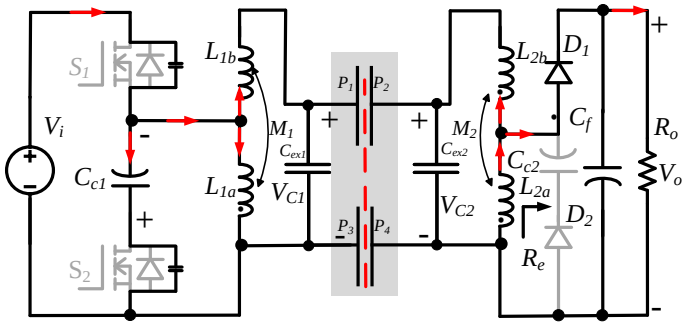
where D is the duty cycle. The polarity of input current of rectifier current changes from negative to positive, the diode D_1 conducts.

Stage 2 $[\pi D \leq \omega t < \pi D + \theta_d]$: During the dead time interval θ_d when both switches S_1 and S_2 are off, as shown in Fig. 5-8(b), zero-voltage-switching (ZVS) of S_2 is achieved by the energy stored in the tapped-inductors L_1, which simultaneously charges and discharges the parasitic output capacitors of switches S_2 and S_1, respectively. The diode D_1 still conducts due to phase lagging of the diode current compared with the diode voltage for the soft switching.

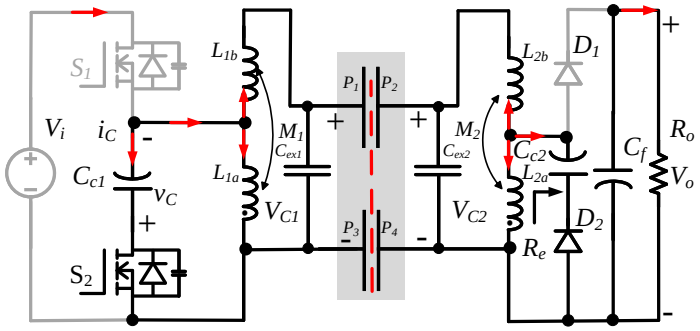
Stage 3 $[\pi D + \theta_d \leq \omega t < 2\pi - \pi D - \theta_d]$: During this time interval, switch S_2 is on and switch S_1 is off as shown in Fig. 5-8(c). Since the parasitic output capacitor of S_2 is already completely discharged at $\omega t = \pi D + \theta_d$, S_2 activates in a ZVS condition, the switch S_1 drain-to-source voltage is clamped as indicated by (5.7), and the currents flowing in L_{1a},



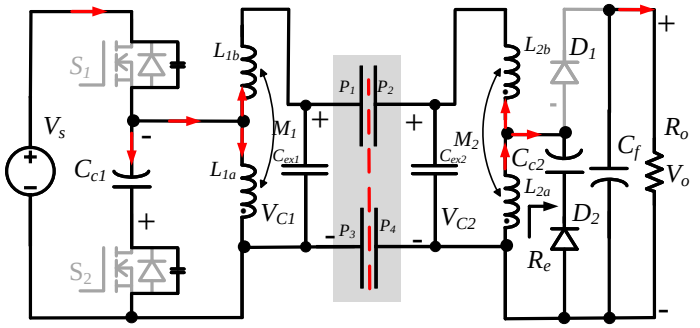
(a)



(b)



(c)



(d)

Figure 5-8: Operation stages of the switch and capacitor topology (a) Stage 1 (b) Stage 2 (c) Stage 3 (d) Stage 4.

Table 5.1: Voltage gain of tapped inductor in different topologies in Fig. 5-5.

Figures	Topologies	Voltage gain
5-5(a)	Switch-to-tap	$\frac{\sqrt{2}N_1 \sin \pi D}{\pi(1-D)}$
5-5(b)	Switch and capacitor-to-tap	$\frac{\sqrt{2}N_1 \sin \pi D}{\pi(1-D)}$
5-5(c)	Output-to-tap	$\frac{\sqrt{2} \sin \pi D}{N_1(1-D)}$
5-5(d)	Output and capacitor-to-tap	$\frac{\sqrt{2} \sin \pi D}{\pi N_1(1-D)}$
5-5(e)	Ground-to-tap	$\frac{\sqrt{2}(N_1-1) \sin \pi D}{\pi(1-D)}$
5-5(f)	Ground and capacitor-to-tap	$\frac{\sqrt{2}(N_1-1) \sin \pi D}{\pi(1-D)}$

L_{1b}, and C_{cc1} are added up to zero as indicated by (5.8).

$$v_{DS1} = \frac{V_i}{1-D} \tag{5.7}$$

$$i_{L1a}(\omega t) + i_{L1b}(\omega t) + i_{cc1}(\omega t) = 0 \tag{5.8}$$

where i_{L1b} and i_{cc1} are the current in resonant tank and clamp capacitor, respectively. The polarity of input current of rectifier current i_e changes from negative to positive, the diode D_2 conducts.

Stage 4 $[2\pi - \pi D - \theta_d \leq \omega t < 2\pi - \pi D]$: During this time interval both switches S_1 and S_2 are off, as shown in Fig. 5-8(d). ZVS of the switch S_1 can be performed in this step by using the energy stored in the inductors L_{1a}, L_{1b} and L_{2b} to charge the parasitic output capacitor of S_1 and discharge the output capacitor of S_2.

Based on the operation principles of the proposed topologies, the voltage gain can be derived. Applying the flux balance condition for L_{1a}, the average voltage of the clamp capacitor, V_{cc1}, and the peak-to-peak current in the inductor L_{1a} can be derived as follows:

$$V_{cc1} = \frac{D}{1-D} V_i \tag{5.9}$$

and

$$\Delta I_{L1a} = \frac{D}{L_{1a} f_s} V_i. \tag{5.10}$$

The proposed inverter can be controlled by a pulse width modulation (PWM) gating signal at the switching frequency, f_s. Under the high-quality factor assumption, the primary voltage can be approximated by its fundamental component. It can be seen that the waveform of

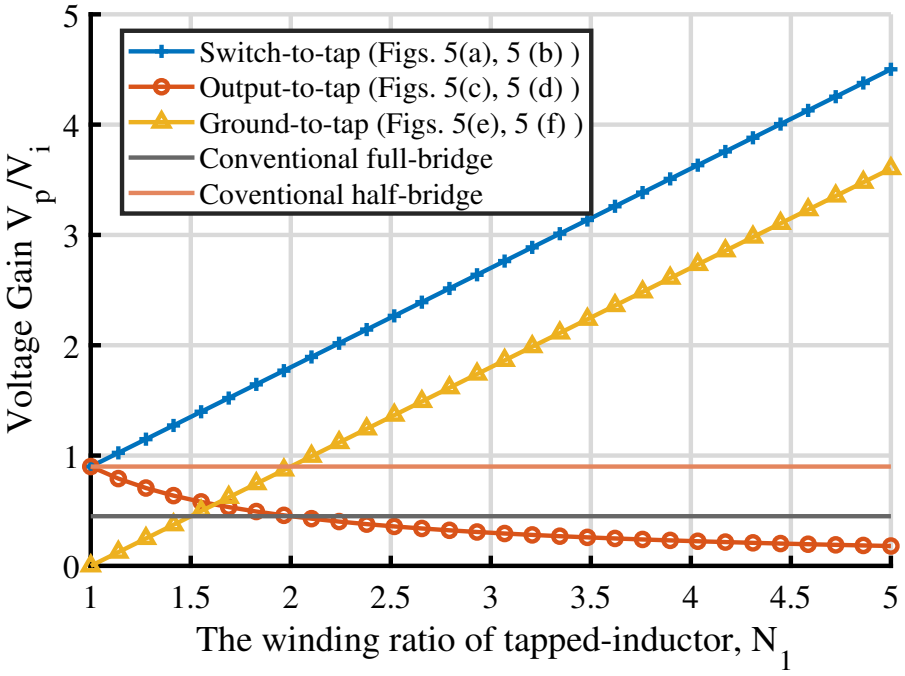


Figure 5-9: Voltage gain comparison of the proposed family of the tapped-inductor half-bridge inverter for CPT system when duty cycle $D = 0.5$.

the primary voltage, V_p, has even symmetry as shown in Fig. 5-7. Thus, the primary voltage is well approximated by

$$V_{p,1} = \frac{\sqrt{2}N_1 V_i \sin \pi D}{\pi(1-D)}. \tag{5.11}$$

In a similar way, voltage gains of all the proposed inverter topologies can be calculated as shown in Table 5.1 and are plotted in Fig. 5-9. As can be seen in Fig. 5-9, the voltage gain of the switch-to-tap and the ground-to-tap is much higher than the conventional full-bridge and half-bridge configuration. The ground and capacitor-to-tap and ground-to-tap have the widest voltage gain, and thus is suitable for application that requires wide voltage variation such as photovoltaic converter, battery charger, and uninterruptible power supplies. The output-to-tap is more suitable for the application with a relatively small voltage variation such as consumer electronics, and LED lighting applications. Switch-to-tap and switch and capacitor-to-tap (Figs. 5-5(a), 5-5(b)) have the highest voltage gain for the same winding ratio N_1 and duty cycle D, so they are the most suitable inverter candidates for CPT system in terms of voltage gain. Therefore, switch and capacitor-to-tap is the most suitable for analysis in this chapter for CPT system. In this case, the combination of inverter and rectifier can be chosen according to the requirement of to the step-up or step-down voltage at the output voltage conversion ratio. For example, the output-to-tap topology can be used

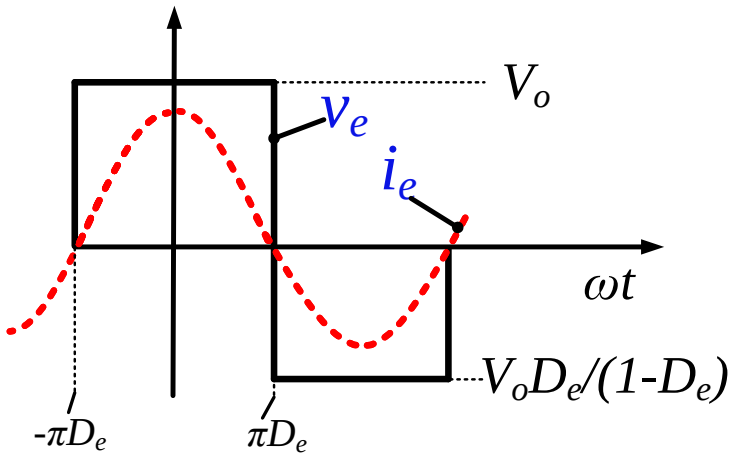


Figure 5-10: Rectifier current and voltage waveforms.

due to the step-up conversion gain for both inverter and rectifier when a high voltage at the output voltage is required, which can can further boost up the output voltage.

5.3.2 Operation Analysis of Rectifier

The voltage gain of rectifiers is a lateral inversion of inverters and thus equal to the reciprocal voltage gain of inverters in Table 5.1, having step down voltage gain, much higher than conventional half-wave rectifier.

The rectifier current and voltage waveform are shown in Fig. 5-10, the voltage applied to the inductor L_{2a}, V_e, is equal to V_o in the positive cycle and is equal to V_{cc2} in the negative cycle. By applying the flux balance condition to the inductor L_{2a}, the voltage in the negative cycle is equal to

$$V_e = \frac{D_e}{1 - D_e} V_o \tag{5.12}$$

where D_e is the effective conduction duty cycle of the rectifier. Therefore, the first harmonic of the rectifier input voltage is given by

$$V_e = \frac{\sqrt{2} \sin \pi D_e}{\pi \left(1 - D_e\right)} V_o. \tag{5.13}$$

Assuming that there is no loss dissipation in the rectifier, the input power of the rectifier should be equal to the output power of the rectifier as

$$\left(\frac{\sqrt{2} \sin \pi D_e}{\pi \left(1 - D_e\right)} V_o \right)^2 \frac{1}{R_e} = \frac{V_o^2}{R_o} \tag{5.14}$$

Thereby, the equivalent resistance is given by

$$R_e = \left(\frac{\sqrt{2} \sin \pi D_e}{\pi \left(1 - D_e\right)} \right)^2 R_o \tag{5.15}$$

To find the value of D_e, the current i_{L2b} is assumed to be sinusoidal as

$$i_{L2b}(\omega t) = -I_{L2b,\max} \cos\left(\omega t + \theta\right) \tag{5.16}$$

where $I_{s,\max}$ and ϕ are the amplitude and phase shift angle in reference to the output voltage of the resonant tank, V_e. The inductor current of inductor L_{2a} is given by
when $-\pi D_e < \omega t \leq \pi D_e$,

$$i_{L2a}\left(\omega t\right) = \int_{-\pi D_e}^{\omega t} -\frac{V_o}{\omega L_{2a}} d\left(\omega t\right) + \int_{-\pi D_e}^{\omega t} \frac{M_2 d(I_{L2b})}{L_{2a} d\left(\omega t\right)} d\left(\omega t\right) + i_{L2a}\left(-\pi D_e\right) \tag{5.17}$$

and where $\pi D_e < \omega t \leq 2\pi - \pi D_e$,

$$i_{L2a}\left(\omega t\right) = \int_{\pi D_e}^{\omega t} \frac{D_e V_o}{\omega L_{2a}\left(1 - D_e\right)} d\left(\omega t\right) + \int_{\pi D_e}^{\omega t} \frac{M_2 d(I_{L2b})}{L_{2a} d\left(\omega t\right)} d\left(\omega t\right) + i_{L2a}\left(\pi D_e\right). \tag{5.18}$$

The input current of the rectifier i_e is calculated by

$$i_e\left(\omega t\right) = i_{L2a}\left(\omega t\right) - i_{L2b}\left(\omega t\right). \tag{5.19}$$

Because $\omega t = \pm \pi D_e$ are defined as the instant of the current zero crossing as shown in Fig. 5-10,

$$\begin{cases} i_e\left(-\pi D_e\right) = 0 \\ i_e\left(\pi D_e\right) = 0. \end{cases} \tag{5.20}$$

From those conditions, the expression of i_{L2a} at $-\pi D_e$ and phase shift angle θ are given by

$$i_{L2a}(-\pi D_e) = -I_{s,\max} \cos(\pi D_e - \theta) \tag{5.21}$$

where

$$\theta = \arcsin\left[-\frac{\pi D_e V_o}{\omega\, I_{s,\max}(M_2+1)\sin(\pi D_e)}\right] \tag{5.22}$$

By applying the charge balance to the capacitor C_{c2}

$$\int_{\pi D_e}^{\pi 2\pi - D_e} i_e\,(\omega t)\,d\,(\omega t) = 0, \tag{5.23}$$

the amplitude $I_{s,max}$ of the current i_{Lb2} can expressed as

$$I_{s,\max} = \frac{\pi^2 D_e V_o (1-D_e)}{\omega\Big[(M_2+L_{2a})\sin(\pi D_e-\theta)+\pi(1-D_e)(M_2+1)\cos(\pi D_e)\Big]}. \tag{5.24}$$

The average current of i_e is equal to the output current I_o

$$I_o = \frac{1}{2\pi D_e}\int_{-\pi D_e}^{\pi D_e} i_e\,(\omega t)\,d\,(\omega t) + \frac{1}{2\pi\,(1-D_e)}\int_{\pi D_e}^{2\pi-\pi D_e} i_e\,(\omega t)\,d\,(\omega t). \tag{5.25}$$

Substituting (5.25) to (5.15), the equivalent resistance R_e is given by

$$R_e = \left(\frac{\sqrt{2}\sin\pi D_e}{\pi(1-D_e)}\right)^2 \frac{\omega L_{2a}}{\pi}\left(1+\pi(1-D_e)[\cot(\pi D_e)-\tan(\theta)]\right) \tag{5.26}$$

5.4 Overall Analysis of Tapped-Inductor CPT Systems for CC-CV Operation

Since, the capacitive coupler of CPT system contains four plates $P_1 - P_4$ resulting in six capacitance as shown in Fig. 5-11(a), it can be represented by two port network model as shown in Fig. 5-11(b), where C_1 and C_2 are equivalent self-capacitance defined as $C_1 = C_{in1}+C_{ex1}$ and $C_2 = C_{in2}+C_{ex2}$ and the capacitive coupling coefficient is $k_c = C_M/(\sqrt{C_1 C_2})$ [31, 139]. The simplified equivalent circuit model of the overall system is shown in Fig. 5-12. Note that every voltage and current is represented in its phasor notation. By KVL, the

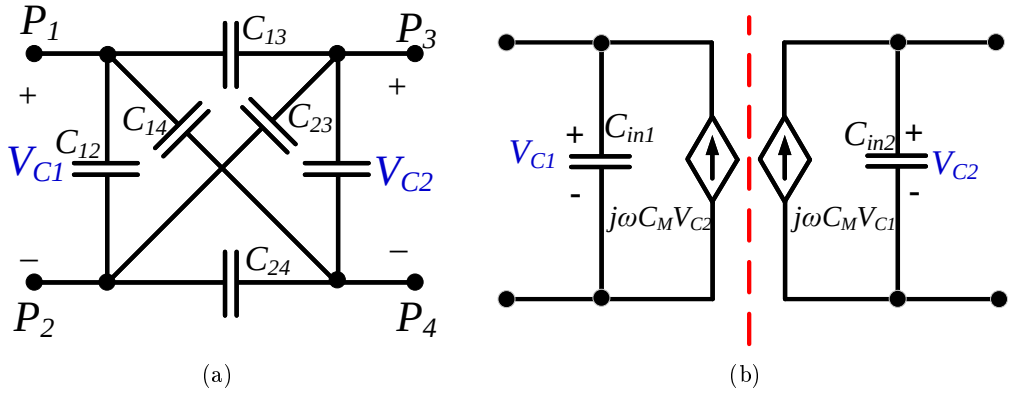


Figure 5-11: Equivalent circuit model of the capacitive coupler (a) circuit model of the coupling capacitors (b) equivalent two-port model.

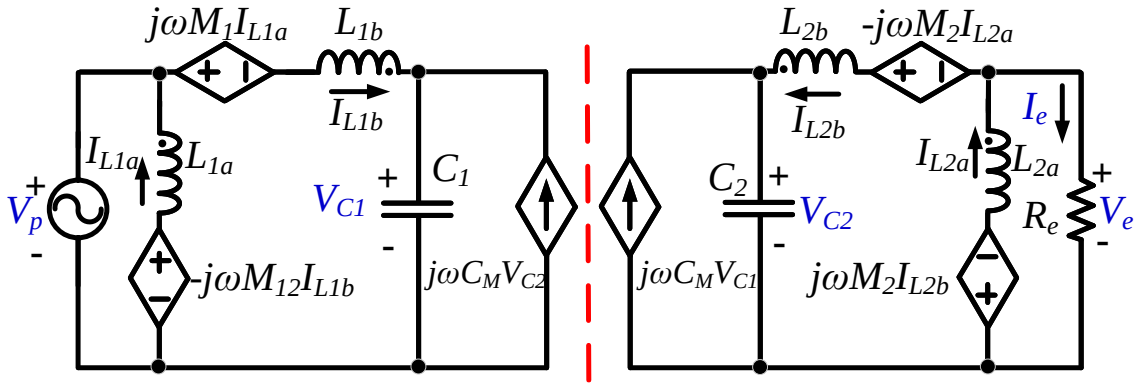


Figure 5-12: Simplified equivalent ac circuit model of the proposed double-side tapped-inductor CPT system.

relationship of current can be expressed as follows:

$$\begin{aligned} I_{L1b} &= Y_{L1}\left(N_1 V_1 - V_{C1}\right) \\ I_{L2b} &= Y_{L2}\left(N_2 V_2 - V_{C2}\right) \\ I_{L2a} &= -\left(N_3\left(N_2 V_2 - V_{C2}\right) + V_e\right) Y_{L2a}. \end{aligned} \tag{5.27}$$

From results of (5.27), KCL is applied to have the relationship of voltage as follows:

$$\begin{aligned} Y_{L1}\left(N_1 V_1 - V_{C1}\right) + Y_M \cdot V_{C2} &= V_{C1} \cdot Y_{C1} \\ Y_{L2}\left(N_2 V_2 - V_{C2}\right) + Y_M \cdot V_{C1} &= V_{C2} \cdot Y_{C2} \\ Y_{L2}\left(N_2 V_2 - V_{C2}\right) + \left(N_3\left(N_2 V_2 - V_{C2}\right) + V_e\right) Y_{L2a} &= -Y_{RL} \cdot V_2 \end{aligned} \tag{5.28}$$

where

$$\begin{aligned}
&Y_{L2\mathrm{a}} = \tfrac{1}{j\omega L_{2\mathrm{a}}}, Y_{L1\mathrm{a}} = \tfrac{1}{j\omega L_{1\mathrm{a}}}, Y_{L2b} = \tfrac{1}{j\omega L_{2b}}, Y_{L1b} = \tfrac{1}{j\omega L_{1\mathrm{b}}},\\
&Y_{\mathrm{C1}} = j\omega C_1, Y_{\mathrm{C2}} = j\omega C_2, Y_M = j\omega C_M,\\
&Y_{L1} = \frac{1}{j\omega\left(L_{1b}-\frac{M_1^2}{L_{1a}}\right)}, Y_{L2} = \frac{1}{j\omega\left(L_{2b}-\frac{M_2^2}{L_{2a}}\right)},\\
&N_1 = \left(1+\tfrac{M_1}{L_{1a}}\right), N_2 = \left(1+\tfrac{M_2}{L_{2a}}\right), N_3 = \frac{M_2}{\left(L_{2b}-\frac{M_2^2}{L_{2a}}\right)},\\
&Y_1 = j\omega C_1 + \frac{1}{j\omega\left(L_{1b}-\frac{M_1^2}{L_{1a}}\right)}, Y_2 = j\omega C_2 + \frac{1}{j\omega\left(L_{2b}-\frac{M_2^2}{L_{2a}}\right)},
\end{aligned} \tag{5.29}$$

The voltage gain $G_v = V_e/V_p$ and the transconductance $G_i = I_e/V_p$ are determined as follows:

$$G_v = \frac{V_e}{V_p} = \frac{Y_M Y_{L1} N_1}{D_0 + \frac{1}{R_e A}\left(Y_1 Y_2 - Y_M^2\right)} \tag{5.30}$$

$$G_i = \frac{I_e}{V_p} = \frac{Y_M Y_{L1} N_1}{R_e D_0 + \frac{1}{A}[Y_1 Y_2 - Y_M^2]}, \tag{5.31}$$

where

$$\begin{aligned}
&D_0 = Y_1\left[Y_2\left(N_2 + \frac{Y_{L2a}}{A}\right) - Y_{L2}N_2\right] - Y_M^2\left(N_2 + \frac{Y_{L2a}}{A}\right),\\
&A = Y_{L2} + N_3 Y_{L2a}.
\end{aligned} \tag{5.32}$$

5.4.1 CV Operation Mode

As shown in (5.30), the voltage gain G_v is independent of the equivalent load resistance R_e when

$$Y_1 Y_2 - Y_M^2 = 0. \tag{5.33}$$

Therefore, the CV frequency that ensure CV mode operation can be given by

$$\omega_{CV1,2} = \sqrt{\frac{\omega_1^2 + \omega_2^2 \pm \sqrt{\left(\omega_1^2+\omega_2^2\right)^2 - 4(1-k_c^2)\omega_1^2\omega_2^2}}{2(1-k_c^2)}} \tag{5.34}$$

where ω_1 and ω_2 are defined as

$$\omega_1 = \frac{1}{\sqrt{C_1\left(L_{1b} - \frac{M_1^2}{L_{1a}}\right)}}, \omega_2 = \frac{1}{\sqrt{C_2\left(L_{2b} - \frac{M_2^2}{L_{2a}}\right)}}. \tag{5.35}$$

By substituting (5.34) to (5.30), the magnitude of G_v in the CV condition is therefore given by

$$G_{CV} = \left|\frac{V_e}{V_p}\right|_{\omega=\omega_{CV1,2}} = \sqrt{\frac{\omega_{1,2}^2 - \omega_1^2}{\omega_{1,2}^2 - \omega_2^2}}\sqrt{\frac{C_1}{C_2}}. \tag{5.36}$$

When the capacitive coupler is designed to be symmetric where $L_{1a} = L_{2a} = L_a$, $L_{1b} = L_{2b} = L_b$, $M_1 = M_2 = M$, and $C_1 = C_2 = C$, the CV frequency and the voltage gain are further simplified as follows:

$$\omega_{CV1,2} = \frac{\omega_0}{\sqrt{1 \mp k_c}}, \tag{5.37}$$

$$|G_{cv}|_{\omega=\omega_{CV1,2}} = \sqrt{\frac{C_1}{C_2}} \tag{5.38}$$

where

$$\omega_0 = \frac{1}{\sqrt{C\left(L_b - \frac{M_1^2}{L_a}\right)}}. \tag{5.39}$$

Therefore, the voltage gain can be designed by changing the capacitive ratio C_1/C_2.

5.4.2 CC Operation Mode

As shown in (5.31), the transconductance gain G_i is independent of equivalent load resistance R_e when

$$Y_1Y_2 - Y_1Y_{L2}\frac{N_2}{\left(N_2 + \frac{Y_{L2a}}{A}\right)} - Y_M^2 = 0. \tag{5.40}$$

Therefore, the CC frequency that ensures CC mode operation can be given by

$$\omega_{CC} = \omega_0\sqrt{\frac{-(F-2) + \sqrt{(F-2)^2 + 4(1-k_c^2)(F-1)}}{2(1-k_c^2)}} \tag{5.41}$$

where

$$F = \frac{L_{2a} + L_{2b} + 2M_2}{L_{2a} + M_2}. \tag{5.42}$$

By substituting (5.41) to (5.31), the magnitude of G_i at the CC condition is therefore given by

$$G_{CC} = \left|\frac{I_e}{V_p}\right|_{\omega=\omega_{CC}} = \frac{N_1N_2\omega_{CC}C_M}{j\omega_o^2\left[k_c^2\left(\frac{\omega_{CC}}{\omega_0}\right)^4 - \left(1 - \left(\frac{\omega_{CC}}{\omega_0}\right)^2\right)^2\right]} \tag{5.43}$$

Table 5.2: Topology Comparisons for CPT system.

Ref.	Driving topology	Compensation type	No. of inverter switches	No. of rectifier diode	No. of compensation inductor and capacitor	Output property	Couper voltage stress	Circuit simplicity
[29]	Full-Bridge	Dual LC	4	4	2 and 2	Step-down CV	Medium	Simple
[109]	Full-Bridge	Dual LC	4	0	4 and 3	Step-down CC,CV	Medium	Simple
[108]	Half Bridge	L	2	4	1 and 0	CV	High	Simple
[135]	Full-Bridge	LCL	4	4	4 and 2	Step-down CC	Medium	Moderate
[94]	Full-Bridge	Dual LCLC	4	4	4 and 4	Step-down CC	Low	Complex
[32]	Half-Bridge	Dual transformer	2	4	1 and 0	Step-down CC	Medium	Moderate
[50]	Full-Bridge	Dual CLC	4	4	4 and 4	Step-down CC	Low	Complex
[30]	Full-Bridge	LCL-LC	4	4	3 and 2	-	Low	Complex
[111]	Class E	L	2	2	3 and 2	-	High	Simple
The proposed topologies	Buck-boost Half-Bridge	Tapped-Inductor	2	2	2 and 2	Step-up and down CC, CV	Medium	Simple

Since the gain is coupling-dependent, gain can be designed by changing the tap ratio of L_1 and L_2 which affects N_1 and N_2 in this formula.

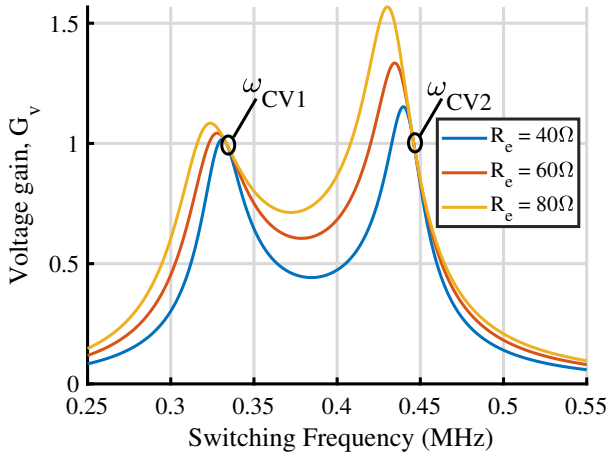
5.4.3 Comparison with the Existing CPT Systems

The comparison between the proposed tapped-inductor inverter/rectifier with integrated matching network and the existing CPT system is shown in Table 5.2. Full-bridge inverter with four switches and full-wave diode rectifier with fours diode is mostly used in the existing CPT system [29, 50, 50, 109, 135]. Moreover,the conventional CPT system support either CV or CC operation [29, 109] but not both. In the proposed system, only two switches and two diodes are required for inverter and rectifier, showing less component count than the existing system. Moreover, step-up and down voltage is possible while still achieving both CC and CV regulation in the proposed system.

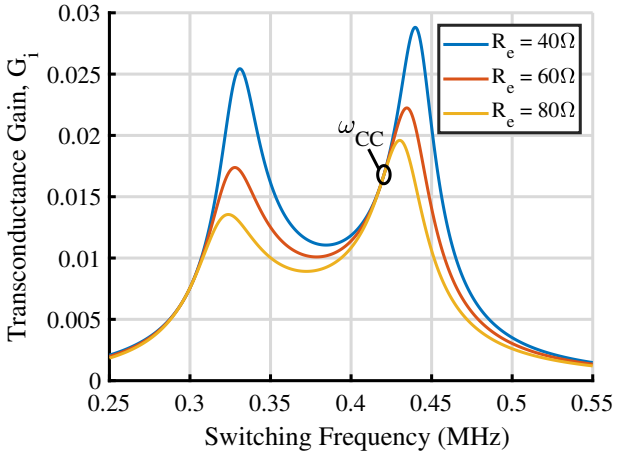
5.5 Prototype Design and Experimental Verification

5.5.1 Prototype Design

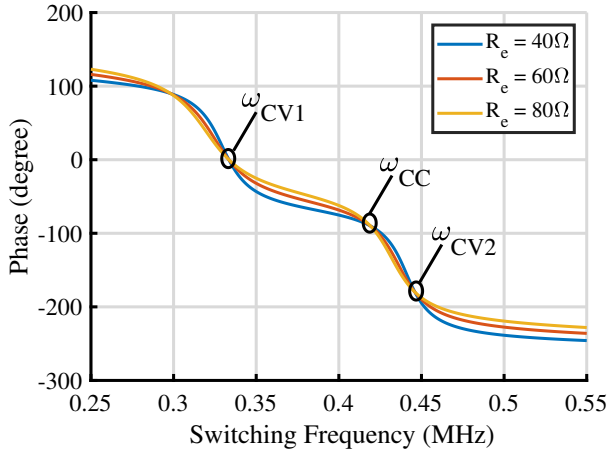
To verify the analysis, a prototype design of the CPT system is given in this section. Four identical (600 mm x 600 mm) aluminum plates are used as the capacitive couplers. The dielectric medium between the two plates is air, and the distance between two plates is 17 mm. Two external capacitor C_{ex1} and C_{ex2} with 500 pF are added to the input and output side of the coupler. The capacitances of C_1, C_2, and C_M are used as 795 pF, 795 pF, and 225 pF, respectively. The system is designed to be symmetric for both input matching network and output matching network as such that $L_{1a} = L_{2a}$, $L_{1b} = L_{2b}$, and $M_1 = M_2$. DC input voltage V_i is set at 50 V and the equivalent load resistance is varied from 40 Ω to 80 Ω. The



(a)



(b)



(c)

Figure 5-13: Gain properties of proposed CPT system (a) magnitude of the voltage gain G_v (b) magnitude of the transconductance gain G_i (c) phase angle of G_v and G_i.

Table 5.3: System parameters of tapped-inductor compensated CPT system.

Symbol	Parameters	Values	Unit
V_i	DC Input Voltage	50	V
V_o	Output Input Voltage	50	V
f_s	Switching frequency	400	kHz
$L_{1a}(L_{2a})$	Parallel inductance	60	μH
$L_{1b}(L_{2b})$	Parallel inductance	230	μH
$M_1(M_2)$	Mutual inductance	18.2	μH
$C_{ex1}(C_{ex2})$	External capacitance	500	pF
$C_1(C_2)$	Link capacitance	700	pF
C_M	Mutual capacitance	200	pF
$C_{c1}(C_{c2})$	Clamp capacitance	50	μF
R_o	Load resistance	40	Ω
C_f	Output filter capacitance	200	μF

system parameters are designed as shown in Table 5.3.

According to the analysis in Section IV, the gain properties of the system for different load conditions are shown in Fig. 5-13. It is shown that there are two CV operation points $f_{CV} = 335$ kHz and $f_{CV} = 440$ kHz and only one CC operation point at $f_{CC} = 420$ kHz which matches well with calculated value from (5.34) and (5.41). Moreover, since the system is designed to be symmetric, the voltage gain G_v is unity at CV operation. Because the only resistivity load R_e is considered in the analysis, the voltage V_e and the current I_e have the same phase angle. As shown in Fig. 5-13(c), the phase angle of the voltage V_e at CV operation and current I_e at CC operation are $\theta_{CV1} = 0^o$, $\theta_{CV2} = 180^o$, and $\theta_{CC} = 90^o$, respectively, where V_p is used as the reference phase.

5.5.2 Coupler Voltage Stress Comparison

Coupler voltage stress comparison with the traditional LC compensation of CPT system is given by simulation results. To form a resonant circuit with the capacitive coupler, inductors L_1 and L_2 of value 222 μH are connected on both sides of the capacitive coupler as shown in Fig. 5-2. The dc output voltage are fixed at 50 V. The transferred power is adjusted by the input voltage to deliver 50 W output power. The stress voltage V_1 and V_2 of the proposed topology is just 0.8 kV while the voltages tress of LC compensation is as high as 1.34 kV. Due to the inherent high voltage gain, the proposed CPT system can reduce the voltage stress by about 1.7 times compared with conventional LC compensation at the same

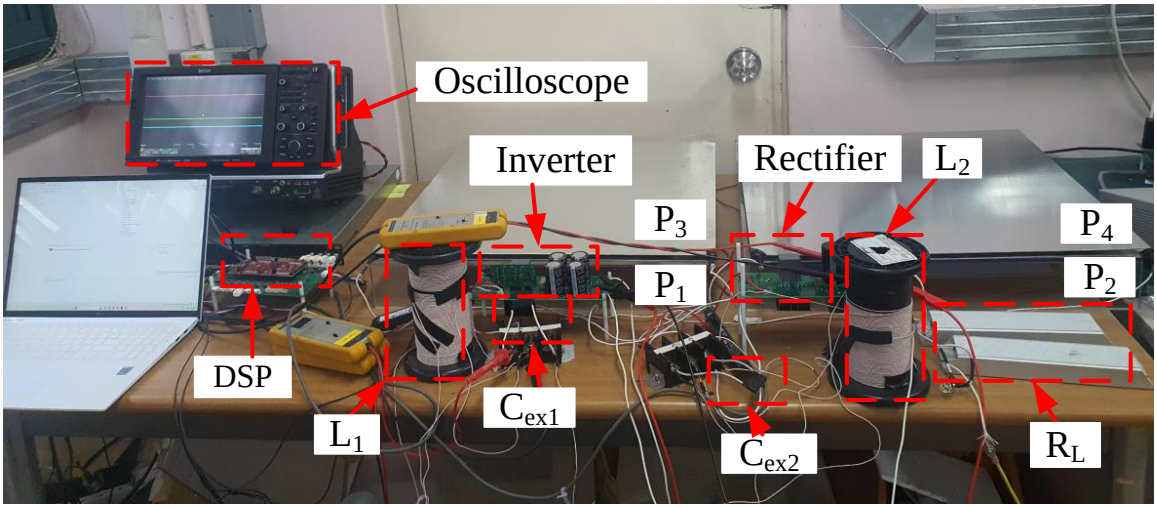


Figure 5-14: Experimental setup of the proposed CPT system.

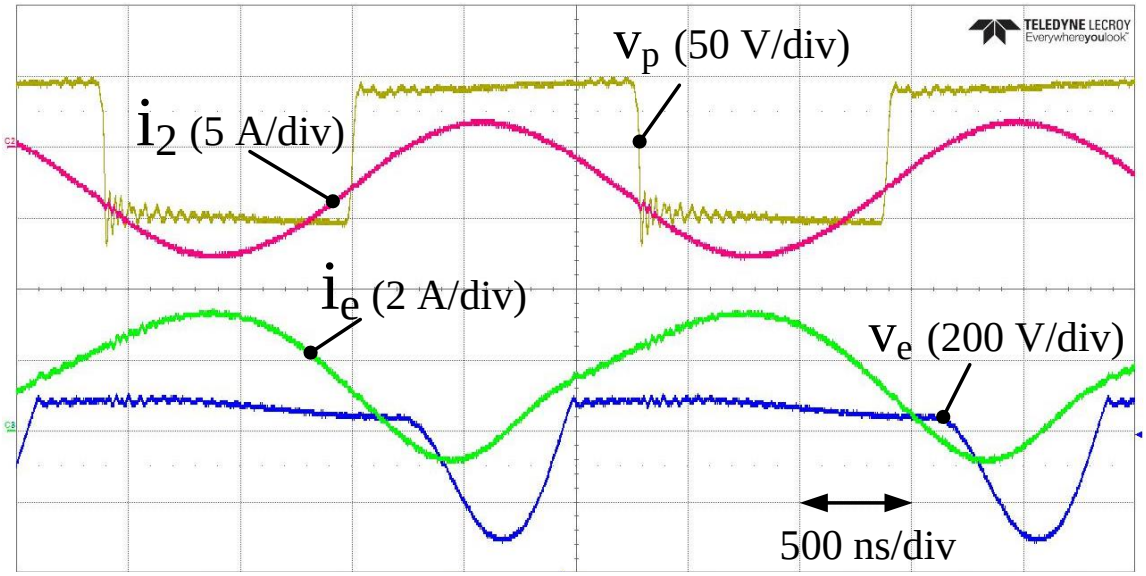


Figure 5-15: Experimental waveforms in the CV operation mode.

transferred power.

5.5.3 Experimental Verification

The experiment is conducted with the hardware setup shown in Fig. 5-14. Silicon carbide MOSFETs (CREE C3M0065090) with on resistance of 78 $m\Omega$ are used as the switches of the HF inverter and silicon carbide schottky diodes with 1 V forward voltage (CREE C3D16060D) are used for the rectifier. The DSP (TI TMS320F28379D) is used as PWM generator for switches. Air core is used for two tapped-inductors with AWG 40 Litz-wire. The experiment was conducted for both CV and CC operation conditions.

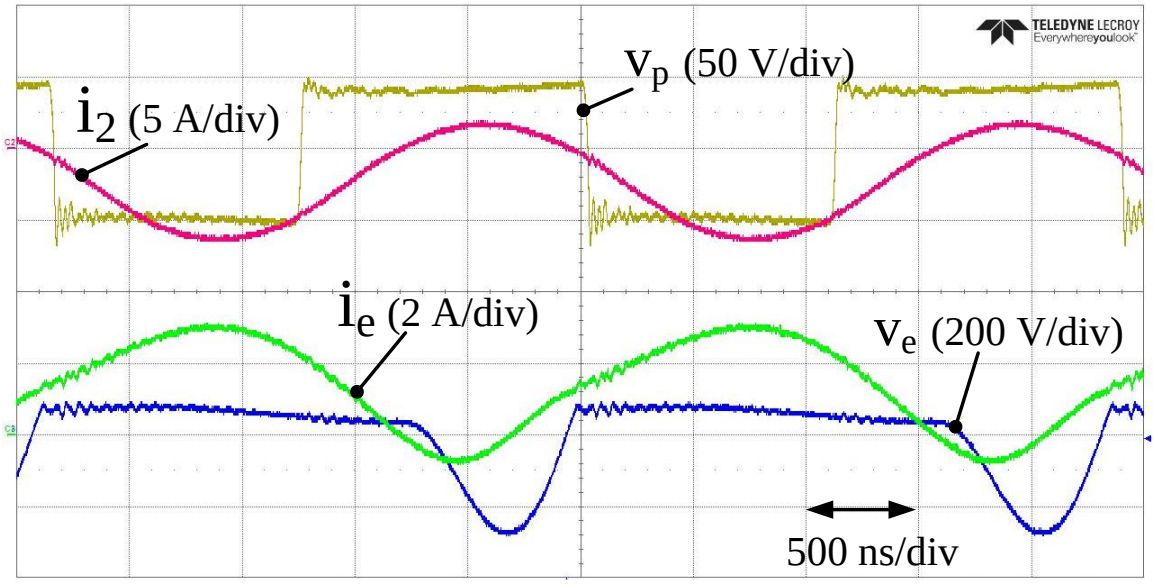


Figure 5-16: Experimental waveforms in the CC operation mode.

CV operation results

For CV operation condition, switching frequency f_s is set at $f_{CV} = 440$ kHz. The experimental results of the CV working mode are shown in Fig. 5-15 for a load resistance $R_o = 40$ Ω. As shown in Fig. 5-15, V_p is lagging V_e by 180^o at the CV frequency ω_{CV2}, which agrees with Fig. 5-13(c).

The power loss distribution among the circuit components is shown in Fig. 5-17(a). The power loss in the compensation inductors and capacitors is calculated by their internal resistances and measured by LCR Meter (Agilent 4263B). MOSFETs and diodes losses are calculated by their drain-to-source resistance and the forward voltage information from datasheets. Accurately measuring power losses in capacitors, especially those with very low dissipation factors, is challenging [141]. Therefore, the losses in the capacitive coupler are estimated by subtracting them from the total losses of the system. The coupler losses are categorized into two types: innate loss and region loss. The innate losses in the coupler structure include metal conduction losses and polarization loss (dielectric losses) [142]. The region loss caused by the air and the leakage current loss between the CPT couplers and the surrounding objects [143]. Coupler loss percentages reported in existing works are summarized in Table 5.4. The coupler loss percentage achieved in this thesis is comparable to that of existing works. To reduce the coupler's power loss, its innate loss can be minimized by improving the conductivity of the metal plates, which lowers the coupler's equivalent series resistance (ESR).

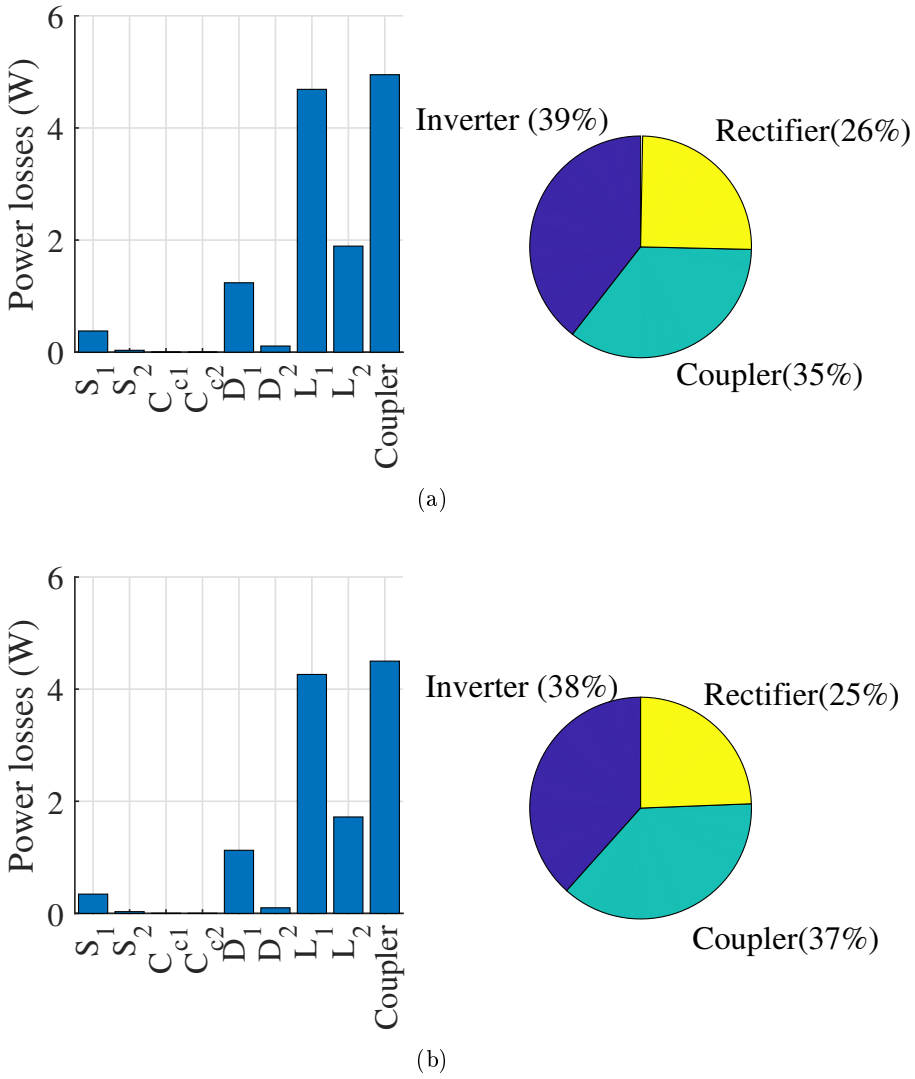


Figure 5-17: Loss-breakdown (a) CV operation (b) CC operation.

The dc-dc system efficiency is 81.5 % and its loss-breakdown is shown in Fig. 5-17(a). In future designs, thicker wire and low loss external capacitors with a lower dissipation factor can be used to reduce the system loss and improve its efficiency [143].

Table 5.4: Coupler Loss Percentage in Existing Works

Reference	Power Rating	Frequency	Efficiency	Coupler Loss
[50]	1.8 kW	1 MHz	85.6%	36%
[29]	150 kW	1.5 MHz	74.8%	26%
[144]	3.75 kW	13.55 MHz	94.7%	5.3%
This thesis	50 W	400 kHz	80.1%	35%

CC operation results

For CV operation condition, the switching frequency f_s is set at 420 kHz. Experimental results of the CC mode are shown in Fig. 5-16 for a load resistance R_o = 40 Ω, which shows the output voltage V_e lags the input voltage V_p by 90^o. This agrees with theoretical expected Fig. 5-13(c). The dc–dc system efficiency is 78.8% and loss-breakdown is shown in Fig. 5-17(b).

5.6 Conclusion

This chapter proposes a family of tapped-inductor inverter/rectifier with integrated matching network structure for CPT system. The tapped-inductor and buck-boost inverter are combined to reduce the voltage stress of the CPT system by providing high voltage conversion ratio. The proposed topology also has the advantage of wide voltage gain to eliminate the additional dc-dc converter resulting in fewer components. The proposed topology can operate in CC and CV modes which are clearly advantageous for the CPT's most popular battery charging applications. The experimental results agree well with the theoretical analysis. The proposed CPT system can reduce the voltage stress by 1.7 times compared with conventional double-side LC at the same transferred power.

Chapter 6

Conclusions and Future Works

6.1 Conclusions

The effectiveness and practicality of capacitive power transfer systems are significantly enhanced thanks to the implementation of advanced topology design and control for this system with reduced voltage stress and misalignment compensation, which serve as critical factors in optimizing performance and ensuring seamless functionality of the CPT system. From current research, this thesis contributes significantly to CPT system development as a new approach to solving high voltage stress and misalignment compensation issues, leading to reduce voltage stress of the capacitive coupler. In addition, the primary side of the CPT system has been proposed to reduce the complexity, volume, and cost of the system.

The central theme of this thesis emphasizes the following important aspects. Firstly, because of simple model designs, it helps to reduce long-term maintenance and replacement expenses, and the creation of the CPT coupler allows safety control and prevents the risk of electrical devices, ensuring no harm to humans even when the system faces high voltage stress. Secondly, from an environmental perspective, simplifying the system not only contributes to cost-effectiveness but also helps reduce carbon emissions and non-recyclable waste, minimizing environmental impact. To exploit the full potential of wireless power transfer, designing and enhancing output performance are crucial factors. Lastly, the complexity of different methods were simplified and handled through duty cycle control, which paves the way for the long-term development strategy in the simplicity and low cost of the CPT systems in the future.

The key core of this thesis on advanced topology and control for capacitive power transfer systems with reduced voltage stress and misalignment compensation systems are summarized

as follows:

- In Chapter 1, a thorough review of the CPT systems on their applications and control. Additionally, the thesis outlined the background, challenges, and objectives; from that, the proposed solutions aimed at enhancing the voltage stress, and misalignment capability of capacitive couplers.

- In Chapter 2, the modeling of capacitive coupler misalignment was presented. Simulations and experiment were carried out to validate the reliability and effectiveness of the analysis.

- In Chapter 3, a parameter estimation technique capable of estimating the load voltage without secondary-side physical quantity measurement was presented. Simulations were carried out to validate the reliability and effectiveness of this method.

- In Chapter 4, an asymmetric half-bridge CPT inverter topology as a single power stage inverter circuit structure with high voltage gain was presented, applicable to application circuits with a very wide input voltage range, such as those for universal AC input. Both simulations and experiment confirmed the effectiveness of proposed topology.

- In Chapter 5 was presented a family of tapped-inductor based inverter and rectifier topologies. Through this, the actual current flowing through the CPT coupler can be reduced, thereby decreasing the voltage stress on the CPT coupler, and an additional advantage of simplifying the complex networks typically required in conventional matching circuits was obtained. The effectiveness of this approach is confirmed through both simulations and experiments. Experimental evidence highlighted the accuracy and robustness of the proposed solution.

This thesis provides new methods that remedies many critical challenges head-on such as voltage stress and misalignment compensation. Alongside the advances in science and new potential capabilities, it establishes of rigorous safety and efficient energy transfer approaches while ensuring the CPT systems are simpler and easier to control in the innovative CPT solutions. As the demand for the WPT engineering field grows, the effective voltage output without any energy losses was also taken into account . By applying new approaches, this research eliminates the need for a complex compensation network and the additional DC-

DC converter, which greatly contributes to a mitigated risk of electrical arcing and dielectric breakdown, bringing in a longer lifespan benefit for the coupler.

In essence, capacitive power transfer harbors huge potential to enhance the WPT systems, yet it still holds some certain limitations. This presents challenges not only related to voltage stress and misaligned coupling, but also concerning safety and the efficiency of power transfer. In the journey toward safety, effective expenses, and environmental sustainability, capacitive wireless power transfer could be everywhere, therefore must meet essential requirements such as design quality, safety, energy efficiency, and electrical distribution capability. In parallel, through this solution, it provides a new direction as a guideline to popularize the CPT application by reducing voltage stress and misalignment compensation.

Overall, this thesis introduces innovative methods that significantly improve the performance, efficiency, and safety of CPT systems, addressing the challenges of high voltage stress of couplers, misalignment, and primary side control.

6.2 Future Works

The CPT systems are a new trend that can be considered as the traditional alternative for IPT and should be applied commonly nowadays. Although this thesis has solved some fundamental issues of the CPT system, there are several extensions for future research that could further be developed based on the results of this thesis. In the future, the following research directions can be identified from this study:

- First, one such area is the enhancement of power density through high-frequency operation. Operating at higher frequencies can significantly reduce the size of passive components and improve overall system efficiency

- Second, bidirectional capability is especially important in applications such as electric vehicles, energy storage systems, and grid-connected devices, where power may need to flow in both directions. Implementing this functionality in CPT systems involves designing appropriate control algorithms, optimizing coupling structures, and ensuring system stability under varying operating conditions.

- Third, dynamic charging, where power is transferred while the load is in motion, requires real-time alignment compensation and robust control under constantly changing coupling conditions. Research in these areas would significantly broaden the practical

applicability and versatility of CPT technology.

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Appendix A: The parallel inductor rms currents calculation

In stage 1 ($-\pi D < \omega t \leq \pi D$), the inductor current is linearly increasing as given by

$$i_{L_p}(\omega t) = \frac{V_s}{\omega L_p}(\omega t + \pi D) + i_{L_p}(-\pi D). \tag{1}$$

At the end of stage 1 when $\omega t = \pi D$,

$$i_{L_p}(\pi D) = \frac{2\pi D V_s}{\omega L_p} + i_{L_p}(-\pi D). \tag{2}$$

If current change is ignored during the dead time angle, for the remaining stages ($\pi D < \omega t \leq 2\pi - \pi D$), the inductor current linearly decreases as given by

$$i_{L_p}(\omega t) = -\frac{D}{\omega L_p (1-D)} V_s (\omega t - \pi D) + i_{L_p}(\pi D) \tag{3}$$

Substituting (2) into (3) we have

$$i_{L_p}(\omega t) = \frac{D V_s}{\omega L_p}\left(2\pi - \frac{\omega t - \pi D}{1-D}\right) + i_{L_p}(-\pi D). \tag{4}$$

Applying charge balance for the capacitor C_c, we have

$$\int_{\pi D}^{2\pi - \pi D} i_{L_p}(\omega t) + i_{tank}(\omega t)\, d(\omega t) = 0 \tag{5}$$

where i_{tank} is the tank current in (4.12), when the resonant tank is driven at the resonant frequency, the phase-shift between primary voltage and tank current, ϕ, equals zero, and

the current in L_p at $-\pi D$ is given by

$$i_{L_p}(-\pi D) = V_s\left(\frac{-\pi D}{\omega L_p} + K\right) \tag{6}$$

where

$$K = \frac{2\sin^2 \pi D}{R_e\left(\pi\left(1-D\right)\right)^2} \tag{7}$$

Finally, by substituting (6) into (1) and (3), the current in inductor L_p can be expressed as follows: for $-\pi D < \omega t \leq \pi D$,

$$i_{L_p}(\omega t) = V_s\left(\frac{1}{\omega L_p}\omega t + K\right) \tag{8}$$

and for $\pi D < \omega t \leq 2\pi - \pi D$,

$$i_{L_p}(\omega t) = V_s\left(\frac{D\left(\pi - \omega t\right)}{\omega L_p\left(1-D\right)} + K\right) \tag{9}$$

which gives (4.14) and (4.15).

From (8) the DC offset of current in inductor L_p can be calculated as

$$\begin{aligned}\Delta I_{L_p} &= \frac{I(\pi D) + I(-\pi D)}{2} \\ &= V_s K\end{aligned} \tag{10}$$

With DC offset and peak-to-peck value of i_{L_p} in (4.7), the rms current of i_{Lp} can be given by

$$I_{rms,L_p} = V_s\sqrt{K^2 + \frac{1}{3}\left(\frac{D}{2L_p f_0}\right)^2}. \tag{11}$$

초록

전계결합형 무선전력전송(CPT)은 금속판 사이의 전기장을 활용하여 에너지를 전송하는 새로운 무선전력전송(WPT) 기술이다. 기존의 자기유도형 무선전력전송(IPT) 시스템과 비교하여 CPT는 주변 금속 구조물에서의 와전류 손실 제거, 가볍고 저렴한 시스템 등 여러 장점을 제공한다. 그러나 공기 또는 진공에서의 낮은 유전율로 인해 전극 혹은 CPT 커플러 사이의 높은 전압 스트레스, 제한된 전력 전송 능력, 좁은 제어 범위 등의 문제점을 겪으며, 이는 실제 응용 분야에서의 채택에 걸림돌이 되고 있다.

본 학위논문은 이러한 기술적인 단점들을 해결하고 CPT 시스템의 구현 가능성을 향상시키는 회로 토폴로지 및 제어 전략들을 제안한다. 논문의 주요 기여 내용으로는 첫째, CPT 커플러의 오정렬에 강인한 회로 매칭 회로 기법, 둘째, 2차측의 전압정보를 추정하여 커플러의 오정렬을 보상하고 광범위한 부하 조건에서 출력 전압을 조절할 수 있는 1차측 제어 전략, 셋째, 고주파 인버터의 전압 이득을 확장하여 광범위한 입력전압과 부하변화를 제어하고 영전압 스위칭을 달성하는 제어방법, 넷째, 탭 인덕터 기반 비대칭 하프 브리지 구조를 통해 CPT 커플러의 전압 스트레스를 줄이는 방법이다.

본 논문은 크게 오정렬에 대한 모델링과 이를 극복하기 위한 제어전략을 다룬 2장 및 3장의 제어 기술부분과 넓은 입출력 제어범위 및 영전압 스위칭을 제공하는 인버터 토폴로지를 제안하고, CPT 커플러에 가해지는 전압스트레스를 저감할 수있는 방법을 제시한 4장 및 5장의 토폴로지 기술 부분으로 구성된다.

먼저, 2장에서는 전극의 오정렬에 대한 모델링을 통해 최적의 인버터 및 커플러 설계를 위한 지침을 제시하였다. IPT와 CPT기술의 쌍대성관계를 활용하여 등가모델의 유사성을 도출하고, 4단자망 해석을 통해 직렬-직렬/직렬-병렬/병렬-직렬/병렬-병렬 구조에서의 오정렬 보상방법을 도출하였다. 한편 3장에서는 2장에서 도출한 등가모델을 활용하여, 오정렬이 발생하였을 때에 2차측 물리량 측정이 없이도 부하전압을 추정할 수 있는 파라메터 추정기법 및 이를 이용한 1차측 제어방법을 제시하였다. 이 방법은 결합 커패시턴스 및 부하 임피던스와 같은 주요 시스템 파라미터를 실시간으로 추정하여,커플러 간 정렬 불량이나 가변 부하 조건에서도 인버터의 작동 조건을 동적으로 조정하여 최적의 전력 전송을 유지할 수 있다. 제안된 제어 방법을 통해 시스템 적응성을 크게 향상시켜, CPT 시스템이 20% 이상의 측면 또는 각도 정렬 불량에서도 안정적인 전력 전송과 효율을 유지할 수 있음을 시뮬레이션으로 검증하였다. 따라서, 제안된 알고리즘을 통해 1-2차간 피드백 제어에 필요한 추가적인 통신 선로를 제거할 수 있으며, 정렬불량 정도를 나타내는 결합 캐패시턴스 값도 추정이 가능하여 커플러의 오정렬에 강인한 CPT시스템 설계가 가능해진다.

한편, 4장에서는 유니버설 AC전압과 같이 입력전압범위가 매우 큰 응용회로에 적용할 수

있는 고전압 이득을 가지는 단일 전력단 인버터회로 구조로서 비대칭 하프브릿지 구조의 CPT 용 인버터 토폴로지가 제안되었다. 특히 5장에서는 이를 더욱 발전시켜 탭 인덕터 기반 인버터 및 정류기 토폴로지 군들을 제시하였는데, 이를 통해 CPT 커플러에 실제 흐르는 전류를 감소시켜 CPT커플러에 걸리는 전압 스트레스를 감소시킬 수 있으며, 기존의 매칭회로에서 일반적으로 요구되는 복잡한 회로망을 단순화시키는 추가적인 장점을 얻었다. 하드웨어 실험을 통해, 제안한 토폴로지가 100mm의 공극에 걸쳐 50W를 전달하고, 80% 이상의 시스템 효율을 달성하며, 넓은 부하 범위에서 소프트 스위칭(ZVS)을 유지함을 검증하였다.

결론적으로, 본 논문에 제시된 일련의 기법을 통해, 오정렬에 더욱 강인하고 좀 더 안전한 CPT 시스템 구성할 수 있다. 또한, 파라메터 추정을 통한 1차측 제어를 통해 추가적인DC-DC 변환회로를 제거하고 및 복잡한 보상 회로망을 단순화 함으로써, CPT기술의 적용범위를 더욱 확대시킬 수 있으며, 이를 통해 경쟁기술인 유선충전이나 IPT 시스템과 비교하여 CPT 기술의 경쟁력을 더욱 강화할 것으로 기대한다. 본 연구에서는 다루지 못하였지만, 향후 연구로서는 고주파 구동을 통한 CPT시스템의 전력 밀도 증가, 양방향 무선전력전달, 그리고 동적 무선충전 및 다중 커플러 활용 기술 등이 유망한 연구주제가 될 수 있을 것이다.